**MOSPEC**

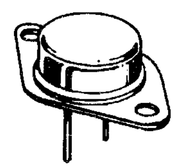
## COMPLEMENTARY SILICON POWER DARLINGTON TRANSISTORS

..designed for use as general purpose amplifiers,low frequency switching and motor control applications.

FEATURES:
* High Gain Darlington Performance
* High DC Current Gain hFE = 400(Min) @ $I_C$ = 10 A
* Monolithic Construction

| PNP | NPN |
|---|---|
| MJ11017 | MJ11018 |
| MJ11019 | MJ11020 |
| MJ11021 | MJ11022 |

15 AMPERE
COMPLEMENTARY
SILICON POWER
DARLINGTON TRANSISTOR
150-250 VOLTS
175 WATTS



TO-3

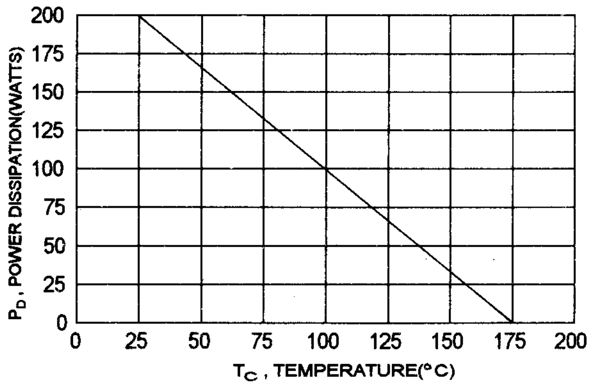
### MAXIMUM RATINGS

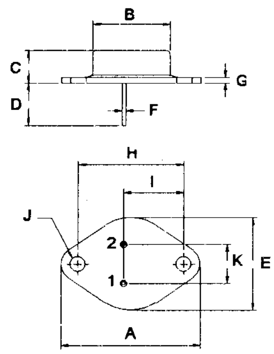
| Characteristic | Symbol | MJ11017 MJ11018 | MJ11019 MJ11020 | MJ11021 MJ11022 | Unit |
|---|---|---|---|---|---|
| Collector-Emitter Voltage | $V_{CEO}$ | 150 | 200 | 250 | V |
| COllector-Base Voltage | $V_{CBO}$ | 150 | 200 | 250 | V |
| Emitter-Base Voltage | $V_{EBO}$ | 5.0 | | | V |
| Collector Current-Continuous<br>-Peak | $I_C$<br>$I_{CM}$ | 15<br>30 | | | A |
| Base Current | $I_B$ | 0.5 | | | A |
| Total Power Dissipation @$T_C$= 25°C<br>Derate above 25°C | $P_D$ | 175<br>1.16 | | | W<br>W/°C |
| Operating and Storage Junction Temperature Range | $T_J$ ,$T_{STG}$ | - 65 to +175 | | | °C |

### THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Thermal Resistance Junction to Case | Rθjc | 0.86 | °C/W |

FIGURE -1 POWER DERATING




PIN 1.BASE
2.EMITTER
COLLECTOR(CASE)

| DIM | MILLIMETERS | |
|---|---|---|
| | MIN | MAX |
| A | 38.75 | 39.96 |
| B | 19.28 | 22.23 |
| C | 7.96 | 9.28 |
| D | 11.18 | 12.19 |
| E | 25.20 | 26.67 |
| F | 0.92 | 1.09 |
| G | 1.38 | 1.62 |
| H | 29.90 | 30.40 |
| I | 16.64 | 17.30 |
| J | 3.88 | 4.36 |
| K | 10.67 | 11.18 |

**ELECTRICAL CHARACTERISTICS** ( $T_C$ = 25°C unless otherwise noted )

| Characteristic | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Collector - Emitter Sustaining Voltage (1) ( $I_C$ = 100 mA, $I_B$ = 0 ) | MJ11017,MJ11018<br>MJ11019,MJ11020<br>MJ11021,MJ11022 | $V_{CEO(sus)}$ | 150<br>200<br>250 | | V |
| Collector Cutoff Current<br>( $V_{CE}$ = 75 V, $I_B$ = 0 )<br>( $V_{CE}$ = 100 V, $I_B$ = 0 )<br>( $V_{CE}$ = 125 V, $I_B$ = 0 ) | | $I_{CEO}$ | | 1.0<br>1.0<br>1.0 | mA |
| Collector Cutoff Current<br>( $V_{CE}$ = Rated $V_{CB}$, $V_{BE(off)}$= 1.5V )<br>( $V_{CE}$ = Rated $V_{CB}$, $V_{BE(off)}$= 1.5V , $T_J$=150 °C) | | $I_{CEV}$ | | 0.5<br>5.0 | mA |
| Emitter Cutoff Current<br>( $V_{EB}$ = 5.0 V, $I_C$= 0 ) | | $I_{EBO}$ | | 2.0 | mA |
| **ON CHARACTERISTICS (1)** | | | | | |
| DC Current Gain<br>( $I_C$ = 10 A, $V_{CE}$ = 5.0 V )<br>( $I_C$ = 15 A, $V_{CE}$ = 5.0 V ) | | hFE | 400<br>100 | 15000 | |
| Collector-Emitter Saturation Voltage<br>( $I_C$ = 10 A, $I_B$ = 100 mA )<br>( $I_C$ = 15 A, $I_B$ = 150 mA ) | | $V_{CE(sat)}$ | | 2.0<br>3.4 | V |
| Base-Emitter Saturation Voltage<br>( $I_C$ = 15 A, $I_B$ = 150 mA ) ) | | $V_{BE(sat)}$ | | 3.8 | V |
| Base-Emitter On Voltage<br>( $I_C$ = 10 A, $V_{CE}$ = 5.0 V ) | | $V_{BE(on)}$ | | 2.8 | V |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Small-Signal Current Gain<br>( $I_C$ = 10 A, $V_{CE}$ = 3.0 V, f = 1.0 MHz ) | | $\lvert h_{fe} \rvert$ | 3.0 | | |

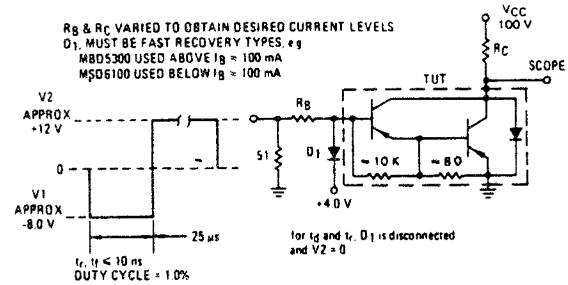
**SWITCHING CHARACTERISTICS**

| Characteristic | | Symbol | Typical NPN | Typical PNP | Unit |
|---|---|---|---|---|---|
| Delay Time | $V_{CC}$ = 100 V, $I_C$ = 10 A<br>$I_{B1}$ = 100mA, $V_{BE(off)}$=5.0V<br>tp = 25us, Duty Cycle ≦ 10% | $t_d$ | 0.2 | 0.1 | us |
| Rise Time | | $t_r$ | 1.3 | 0.6 | us |
| Storage Time | | $t_s$ | 4.5 | 2.7 | us |
| Fall Time | | $t_f$ | 10 | 2.6 | us |

(1) Pulse Test: Pulse width = 300 us , Duty Cycle ≦ 2.0%

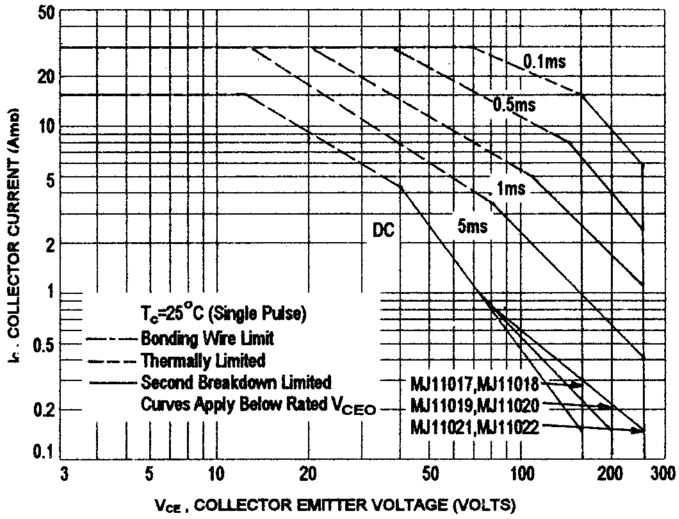
(2) $f_T = \lvert h_{fe} \rvert \circ f_{test}$

**FIGURE 2 — SWITCHING TIMES TEST CIRCUIT**




For NPN test circuit reverse diode and voltage polarities.

FIG-3 FORWARD BIAS SAFE OPERATING AREA

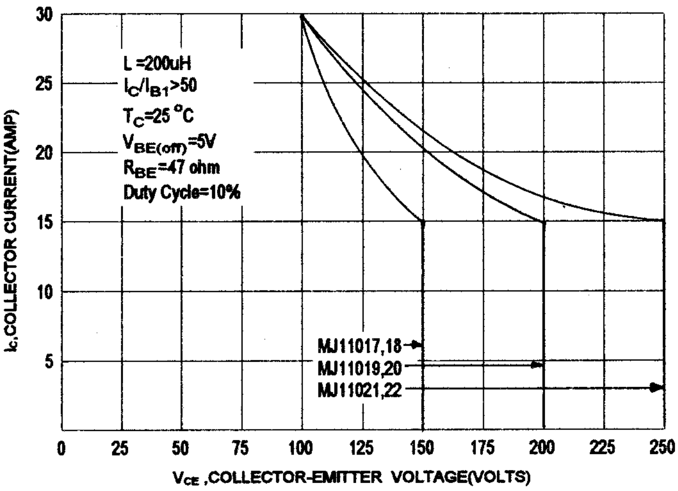



## FORWARD BIAS

There are two limitation on the power handling ability of a transistor:average junction temperature and second breakdown safe operating area curves indicate $I_C$-$V_{CE}$ limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than curves indicate.

The data of FIG-3 is base on $T_{J(PK)}$=200 °C;$T_C$ is variable depending on conditions.At high case temperatures , thermal limitation will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIG-4 REVERSE BIAS SAFE OPERATING AREA

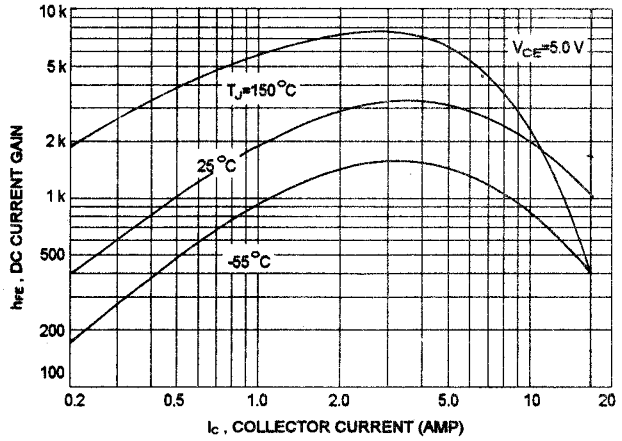



## REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off,in most cases, with the base-to-emitter junction reverse biased Under these conditions the collector voltage must be held to a safe level at or below a specfic value of collector current.This can be accomplished by several mean such as active clamping, RC snubbing, load line shaping, etc. the safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. FIG-4 gives the RBSOA characteristics.

FIG-5 DC CURRENT GAIN

PNP




NPN

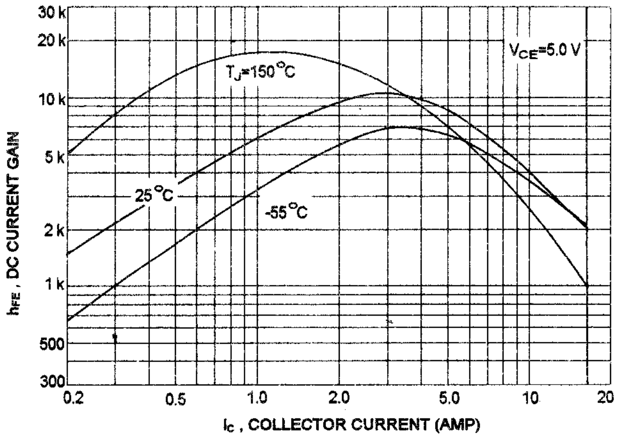
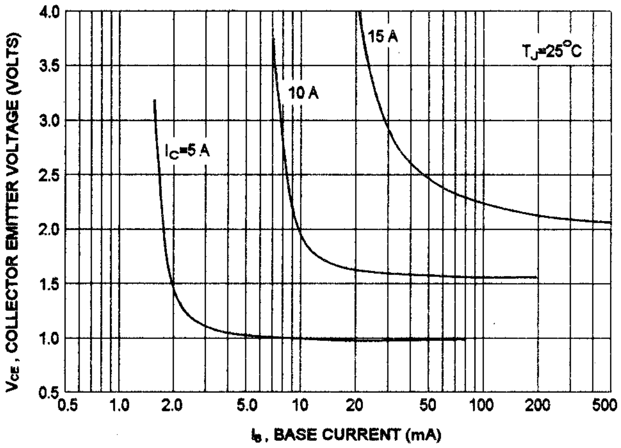



FIG-6 COLLECTOR SATURATION

PNP




NPN

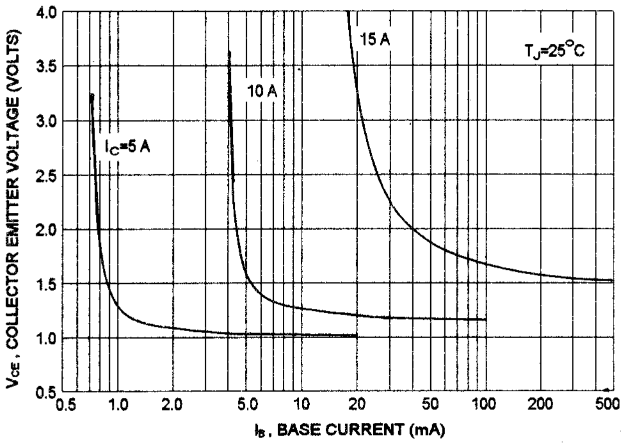
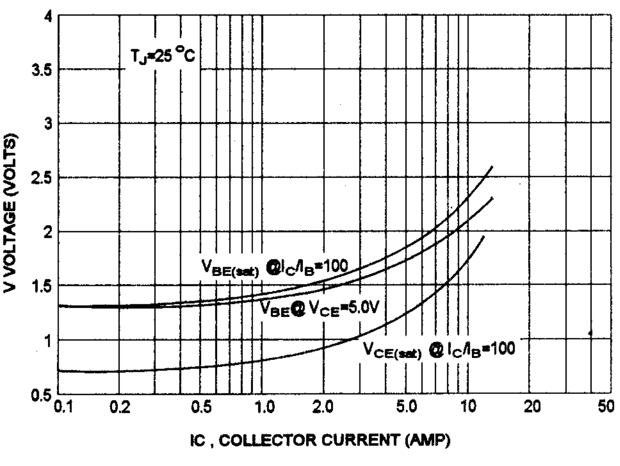



FIG-7 "ON" VOLTAGE

PNP




NPN