



High Speed Flow-through 1-Mbit (16Kx64) Standard 1T-SRAM[®] Embedded Memory Macro

M1T1HT18FL64E

• High Speed 1T-SRAM Standard Macro

- 100 MHz operation
- 1-Clock cycle time
- Flow-through read access timing
- Late write mode timing
- 64-Bit wide data buses
- Byte Write Enables
- Simple standard SRAM interface
- Fast delivery

• Ultra-Dense Memory

- 3.6mm² size per macro instance
- Redundancy & fuses included in macro area

• Silicon-Proven 1T-SRAM Technology

- Qualification programs completed
- Products in volume production

• High Yield and Reliability

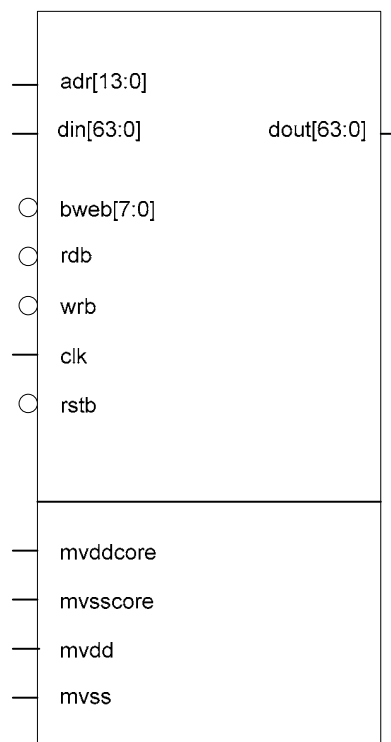
- Built-in redundancy for enhanced yield

• Standard Logic Process

- TSMC 0.18µm CL018G process
- Logic design rules
- Uses 4 metal layers
- Routing over macro possible in layers 5+

• Power

- Single voltage 1.8V Supply
- Low power consumption



General Description

The M1T1HT18FL64E is a 1Mbit (1,084,576 bits), high speed, embedded 1T-SRAM macro. The M1T1HT18FL64E is organized as 16K(16,384) words of 64 bits. The macro employs a flowthrough read timing interface with late write timing. Write control over individual bytes in the input data is achieved through the use of the byte write enable (bweb) input signals. The M1T1HT18FL64E macro is implemented using MoSys 1T-SRAM technology, resulting in extremely high density and performance.



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Memory Interface Signal List

| Signal Name | Valid | Logic | Direction | Description |
|-------------|-------------------|----------|-----------|---|
| adr[13:0] | Positive clk edge | Positive | Input | Memory address |
| bweb[7:0] | Positive clk edge | Negative | Input | Memory byte write enables bweb[n] = 0 enables data write bweb[n] = 1 disables data write bweb[7] controls writing of din[63:56] bweb[6] controls writing of din[55:48] bweb[5] controls writing of din[47:40] ... bweb[0] controls writing of din[7:0] |
| rdb | Positive clk edge | Negative | Input | Memory read |
| wrb | Positive clk edge | Negative | Input | Memory write |
| din[63:0] | Positive clk edge | Positive | Input | Memory data in bus |
| dout[63:0] | Positive clk edge | Positive | Output | Memory data out bus |
| rstb | Positive clk edge | Negative | Input | Memory initialization reset |
| clk | Clock | Positive | Input | Memory Clock |
| mvddcore | | | | Memory core supply voltage |
| mvsscore | | | | Memory core ground |
| mvdd | | | | Memory interface supply voltage |
| mvss | | | | Memory interface ground |

Operating Conditions

| Symbol | Parameter | Condition | Min | Max | Units |
|------------------|----------------------------------|----------------------------|-----------------------|-----------------------|-------|
| V _{DD} | Supply Voltage Range (1.8V ±10%) | Operating | 1.62 | 1.98 | V |
| T _J | Junction Temperature | Nominal V _{DD} | 0 | 125 | °C |
| t _{CYC} | Cycle Time | Operating | 5.0 | 33.3* | ns. |
| t _{CKH} | Clock High | Operating | 0.45*t _{CYC} | 0.55*t _{CYC} | ns. |
| t _{CKL} | Clock Low | Operating | 0.45*t _{CYC} | 0.55*t _{CYC} | ns. |

Note: Minimum clock frequency limit adjustable to meet system timing requirements

Power Requirements

| Symbol | Condition | Current per Instance | Units |
|------------------|--|----------------------|--------|
| I _{DD1} | Operating current, V _{DD} =1.8V, clock frequency = 100MHz, output not loaded, memory accessed every clock | 0.7 | mA/MHz |
| I _{DD2} | Standby current, V _{DD} =1.8V, clock frequency =100MHz, memory not accessed | 0.3 | mA/MHz |

Input Loading

| Symbol | Condition | Load Capacitance | Units |
|------------------|--|------------------|-------|
| C _{DIN} | din signal input loading | 0.1 | pF |
| C _{ADR} | adr signal input loading | 0.1 | pF |
| C _{CTL} | rdb, wrb and bweb signal input loading | 0.1 | pF |
| C _{CLK} | clk signal input loading | 1.0 | pF |



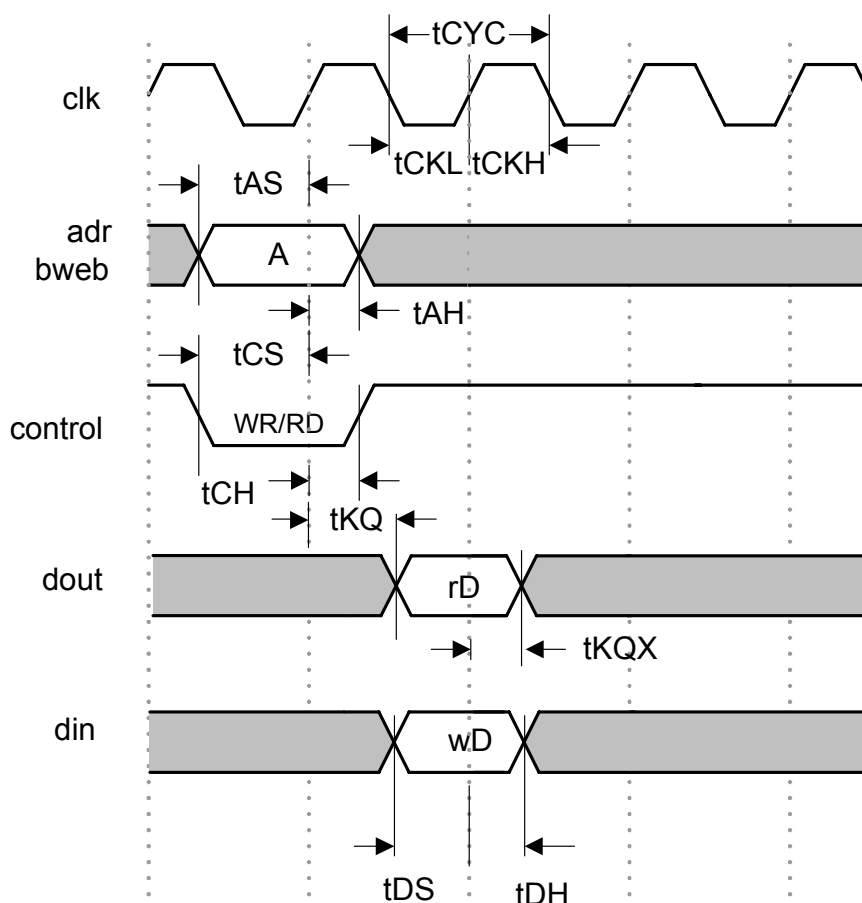
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AC Timing Characteristics

All times in nanoseconds

Bolded numbers reflect worst case design parameters

| Parameter | Description | Condition | Slow | Typical | Fast |
|-----------|-----------------------------------|-----------|------------|---------|------------|
| tAS | Address Setup | Min. | 1.0 | 0.8 | 0.6 |
| tAH | Address Hold | Min. | 0.5 | 0.4 | 0.3 |
| tCS | Control Setup | Min. | 1.0 | 0.8 | 0.6 |
| tCH | Control Hold | Min. | 0.5 | 0.4 | 0.3 |
| tDS | Write Data Setup | Min. | 1.0 | 0.8 | 0.6 |
| tDH | Write Data Hold | Min. | 0.5 | 0.4 | 0.3 |
| tKQ | Clock to Data Valid | Max. | 7.0 | 6.0 | 5.0 |
| tKQE | Data valid extrinsic delay per pF | Max. | 0.8 | 0.6 | 0.4 |
| tKQX | Clock to Data not valid | Min. | 0.8 | 0.6 | 0.5 |



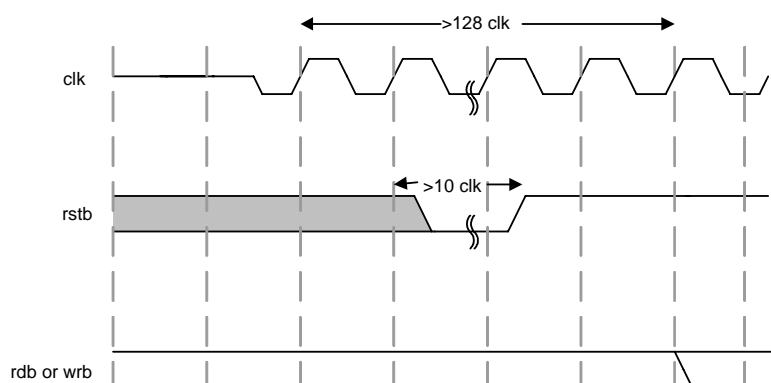
General AC Timing



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Memory macro implements a synchronous reset to force state machines into a known state after power-up. This reset does not clear the memory contents. The clock must be running for at least two cycles before the Reset (rstb) signal will be correctly sampled as shown above. The Reset (rstb) signal must be active for at least ten (10) clock periods to initialize all internal circuitry. Independent of the Reset (rstb) signal, after power has stabilized to a voltage within the operating specification and the clock is operating within its timing specifications, there must be at least 128 clock cycles before any read or write access.



Initialization Timing



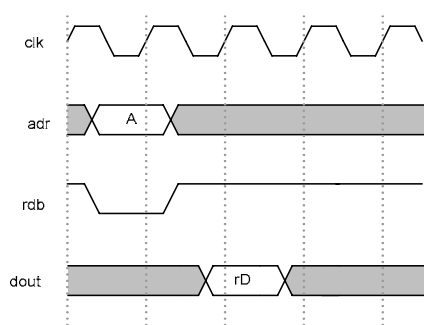
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OPERATION TRUTH TABLE

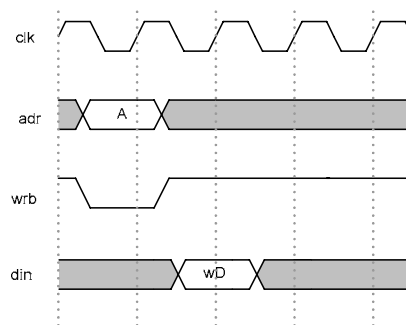
| rdb | wrb | Operation |
|-----|-----|-----------|
| 0 | 0 | Illegal |
| 0 | 1 | Read |
| 1 | 0 | Write |
| 1 | 1 | Nop |

FUNCTIONAL OPERATION

Address and command clocked in by rising clock edge. Both read and write data transfer occur in the same clock cycle. This particular standard macro uses user-managed refresh hiding. Consult factory for options.



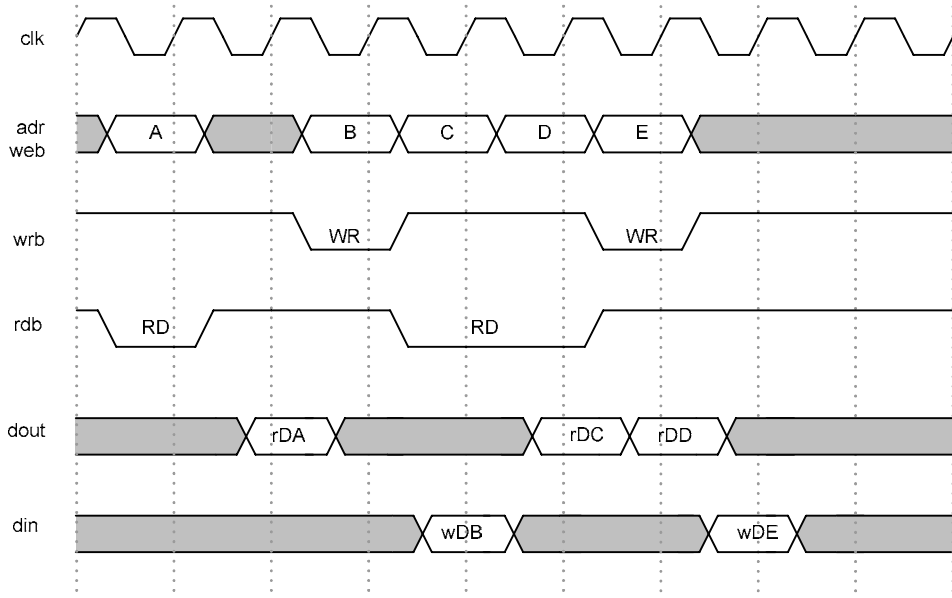
Single Cycle Read Timing



Single Cycle Write Timing

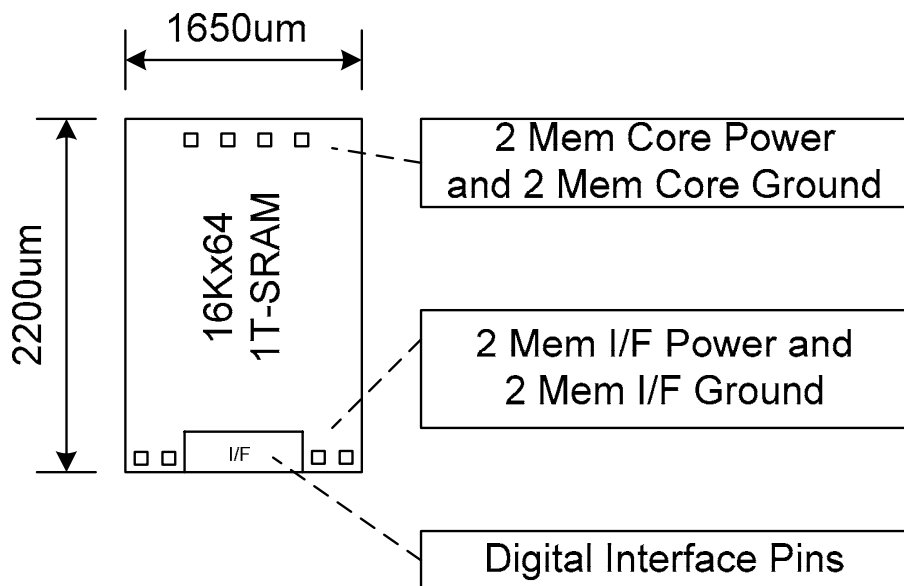


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Multiple Cycle Timing

MEMORY BLOCK ESTIMATES*



*Note: Approximate dimensions. Exact dimensions appear on place and route phantom

Physical Layout