# Octal 3-State Inverting Bus Transceiver

High–Performance Silicon–Gate CMOS

The MC54/74HC640A is identical in pinout to the LS640. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC640A is a 3–state transceiver that is used for 2–way asynchronous communication between data buses. The device has an active–low Output Enable pin, which is used to place the I/O ports into high–impedance states. The Direction control determines whether data flows from A to B or from B to A.
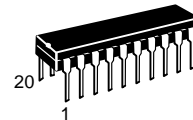
- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 276 FETs or 69 Equivalent Gates
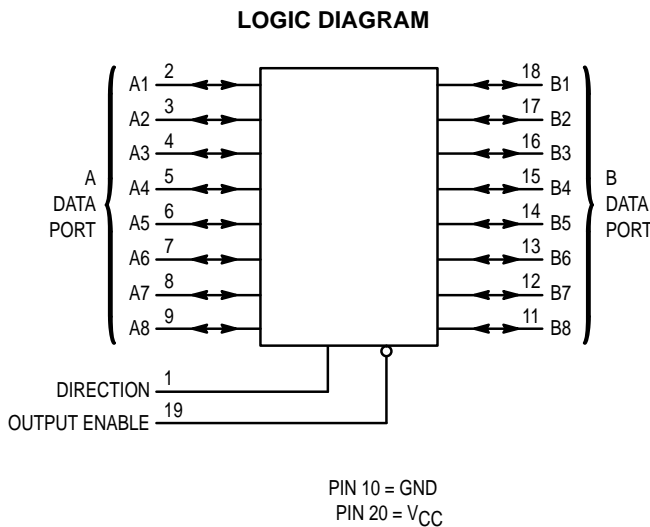
MC54/74HC640A
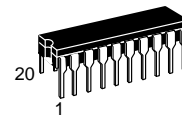
J SUFFIX
CERAMIC PACKAGE
CASE 732–03

N SUFFIX
PLASTIC PACKAGE
CASE 738–03

DW SUFFIX
SOIC PACKAGE
CASE 751D–04

ORDERING INFORMATION

MC54HCXXXAJ	Ceramic
MC74HCXXXAN	Plastic
MC74HCXXXADW	SOIC

LOGIC DIAGRAM

A DATA PORT: A1 (2), A2 (3), A3 (4), A4 (5), A5 (6), A6 (7), A7 (8), A8 (9)

B DATA PORT: B1 (18), B2 (17), B3 (16), B4 (15), B5 (14), B6 (13), B7 (12), B8 (11)

DIRECTION 1

OUTPUT ENABLE 19

PIN 10 = GND
PIN 20 = V$_{CC}$

PIN ASSIGNMENT

DIRECTION	1●	20	V$_{CC}$
A1	2	19	OUTPUT ENABLE
A2	3	18	B1
A3	4	17	B2
A4	5	16	B3
A5	6	15	B4
A6	7	14	B5
A7	8	13	B6
A8	9	12	B7
GND	10	11	B8

FUNCTION TABLE

Control Inputs		Operation
Output Enable	Direction	
L	L	Data Transmitted from Bus B to Bus A (Inverted)
L	H	Data Transmitted from Bus A to Bus B (Inverted)
H	X	Buses Isolated (High–Impedance State)

X = don't care

REV 7

MOTOROLA

MC54/74HC640A

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND), Pin 1 or 19	– 0.5 to V_{CC} + 0.5	V
$V_{I/O}$	DC I/O Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
$I_{I/O}$	DC I/O Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	 260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND $\leq$ (V_{in} or V_{out}) $\leq$ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus.

* Maximum Ratings are those values beyond which damage to the device may occur.
  Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
  Ceramic DIP: – 10 mW/°C from 100° to 125°C
  SOIC Package: – 7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions		V_{CC} V	Guaranteed Limit			Unit
					– 55 to 25°C	$\leq$ 85°C	$\leq$ 125°C	
V_{IH}	Minimum High–Level Input Voltage	$V_{out} = V_{CC}$ – 0.1 V $|I_{out}| \leq 20\,\mu A$		2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V $|I_{out}| \leq 20\,\mu A$		2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High–Level Output Voltage	$V_{in} = V_{IH}$ $|I_{out}| \leq 20\,\mu A$		2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$	$|I_{out}| \leq 2.4$ mA $|I_{out}| \leq 6.0$ mA $|I_{out}| \leq 7.8$ mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.2 3.7 5.2	
V_{OL}	Maximum Low–Level Output Voltage	$V_{in} = V_{IL}$ $|I_{out}| \leq 20\,\mu A$		2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IL}$	$|I_{out}| \leq 2.4$ mA $|I_{out}| \leq 6.0$ mA $|I_{out}| \leq 7.8$ mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.4 0.4 0.4	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	µA
I_{OZ}	Maximum Three–State Leakage Current	Output in High–Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	± 0.5	± 5.0	± 10	µA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0$ µA	6.0	4.0	40	160	µA

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to B, B to A (Figures 1 and 3)	2.0 3.0 4.5 6.0	75 55 15 13	95 70 19 16	110 80 22 19	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Direction or Output Enable to A or B (Figures 2 and 4)	2.0 3.0 4.5 6.0	110 90 22 19	140 110 28 24	165 130 33 28	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Output Enable to A or B (Figures 2 and 4)	2.0 3.0 4.5 6.0	110 90 22 19	140 110 28 24	165 130 33 25	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 3.0 4.5 6.0	60 23 12 10	75 27 15 13	90 32 18 15	ns
C_{in}	Maximum Input Capacitance, Pin 1 or 19	—	10	10	10	pF
C_{out}	Maximum Three–State I/O Capacitance (Output in High–Impedance State)	—	15	15	15	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Transceiver Channel)*	40	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).
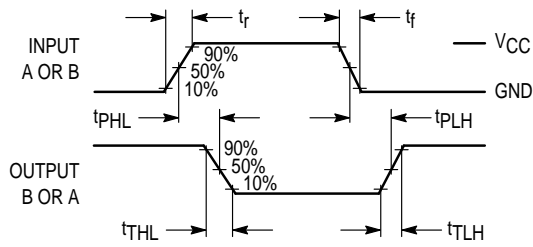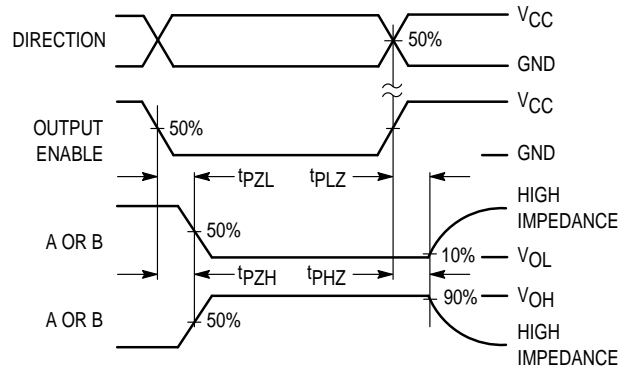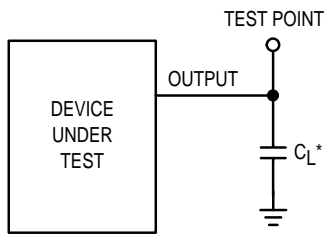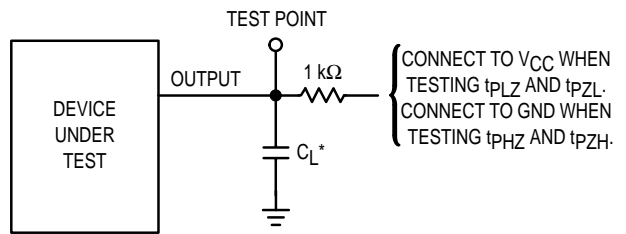
SWITCHING WAVEFORMS

Figure 1.

Figure 2.

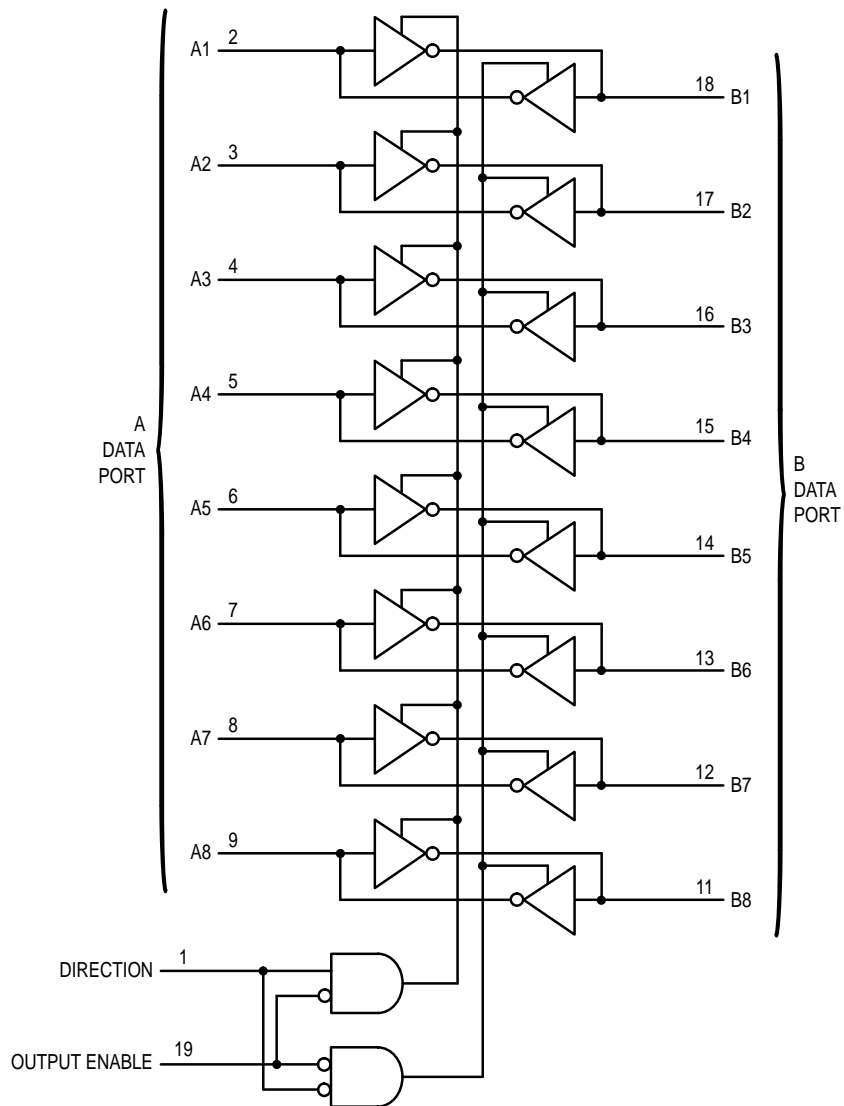## tTEST CIRCUITS

* Includes all probe and jig capacitance

Figure 3.

CONNECT TO V_{CC} WHEN TESTING t_{PLZ} AND t_{PZL}.
CONNECT TO GND WHEN TESTING t_{PHZ} AND t_{PZH}.

* Includes all probe and jig capacitance

Figure 4.

EXPANDED LOGIC DIAGRAM

A DATA PORT

B DATA PORT

A1	2		18	B1
A2	3		17	B2
A3	4		16	B3
A4	5		15	B4
A5	6		14	B5
A6	7		13	B6
A7	8		12	B7
A8	9		11	B8

DIRECTION 1

OUTPUT ENABLE 19

MC54/74HC640A

OUTLINE DIMENSIONS

J SUFFIX
CERAMIC PACKAGE
CASE 732–03
ISSUE E
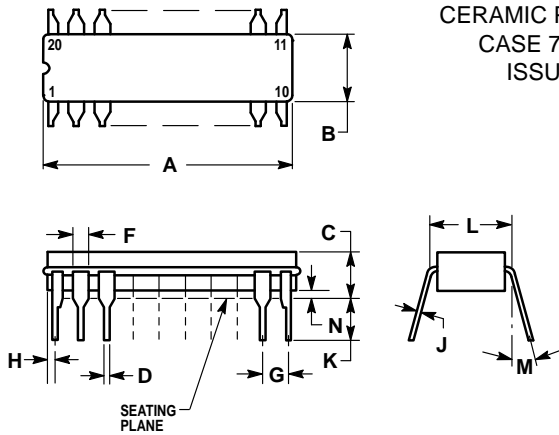
NOTES:
1. LEADS WITHIN 0.25 (0.010) DIAMETER, TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONS A AND B INCLUDE MENISCUS.

DIM	MILLIMETERS		INCHES	
---	MIN	MAX	MIN	MAX
A	23.88	25.15	0.940	0.990
B	6.60	7.49	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.040

N SUFFIX
PLASTIC PACKAGE
CASE 738–03
ISSUE E
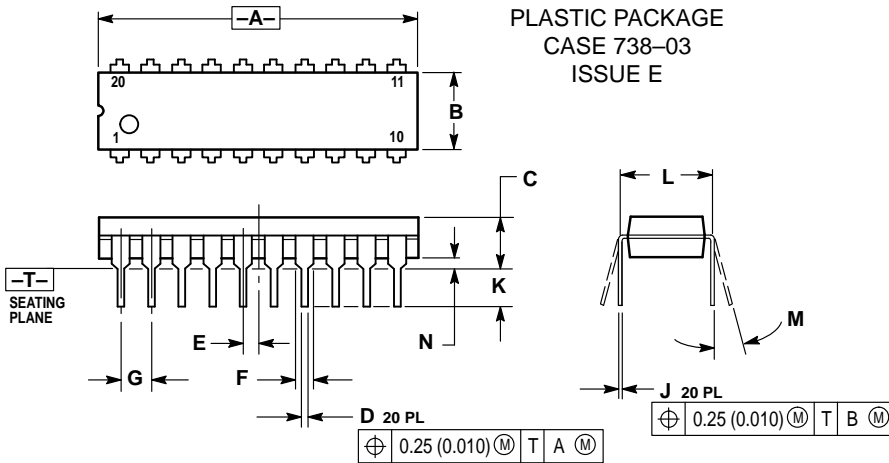
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

⊕ 0.25 (0.010) Ⓜ T A Ⓜ

⊕ 0.25 (0.010) Ⓜ T B Ⓜ

DIM	INCHES		MILLIMETERS	
---	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D–04
ISSUE E
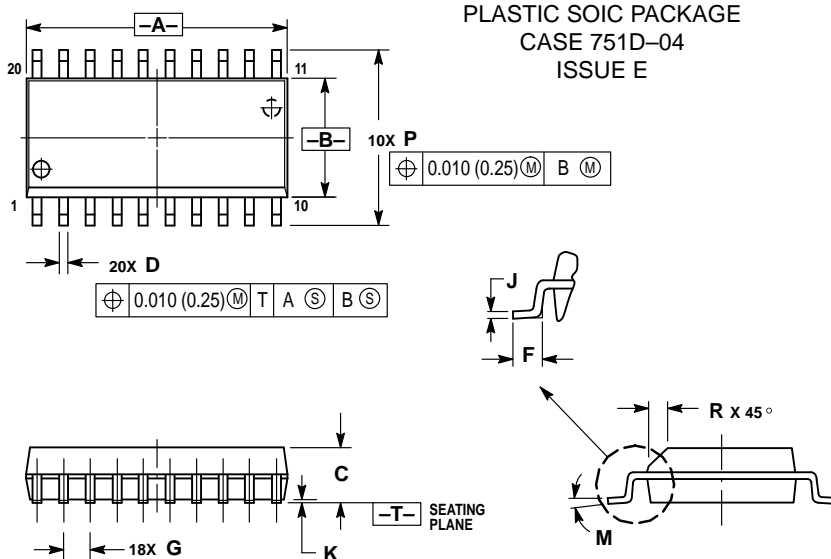
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

⊕ 0.010 (0.25) Ⓜ B Ⓜ

⊕ 0.010 (0.25) Ⓜ T A Ⓢ B Ⓢ

DIM	MILLIMETERS		INCHES	
---	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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