

Advance Information
Low-Voltage CMOS 16-Bit Latching Transceiver
With 5V-Tolerant Inputs and Outputs
(3-State, Non-Inverting)

The MC74LCX16543 is a high performance, non-inverting 16-bit latching transceiver operating from a 2.7 to 3.6V supply. The device is byte controlled. Each byte has separate control inputs which can be tied together for full 16-bit operation. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX16543 inputs to be safely driven from 5V devices. The MC74LCX16543 is suitable for memory address driving and all TTL level bus oriented transceiver applications.

For data flow from A to B with the EAB LOW, the A-to-B Output Enable (OEAB) must be LOW in order to enable data to the B bus, as indicated in the Function Table. With EAB LOW, a LOW signal on the A-to-B Latch Enable (LEAB) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the LEAB signal will latch the A latches, and the outputs no longer change with the A inputs. With EAB and OEAB both LOW, the 3-State B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is symmetric to that above, but uses the EBA, LEBA, and OEBA inputs.

- Designed for 2.7 to 3.6V V_{CC} Operation
- 5.2ns Maximum t_{pd}
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When $V_{CC} = 0V$
- LVTTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (20 μ A) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V

MC74LCX16543

LCX

LOW-VOLTAGE CMOS
16-BIT LATCHING
TRANSCEIVER



DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 1202-01

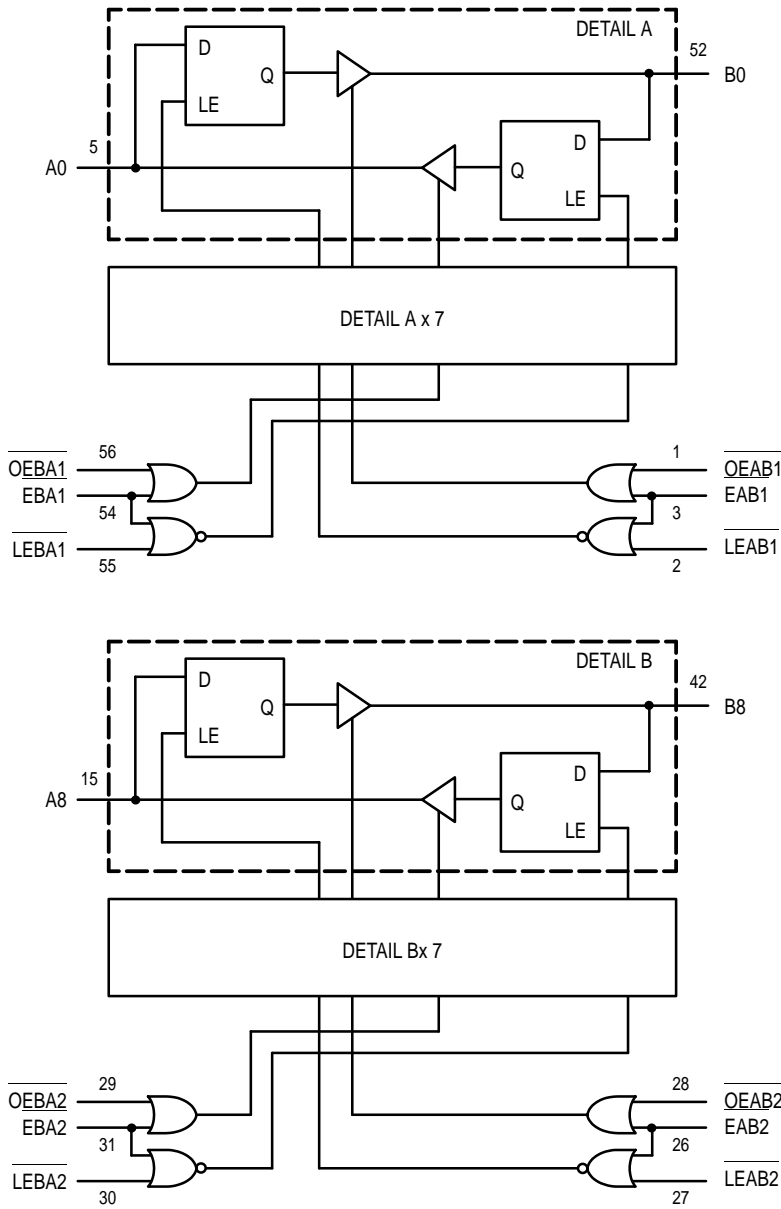
PIN NAMES

| Pins | Function |
|--------------------------|------------------------|
| <u>OE</u> _{xxn} | Output Enable Inputs |
| <u>E</u> _{xxn} | Enable Inputs |
| <u>LE</u> _{xxn} | Latch Enable Inputs |
| A0-A15 | 3-State Inputs/Outputs |
| B0-B15 | 3-State Inputs/Outputs |

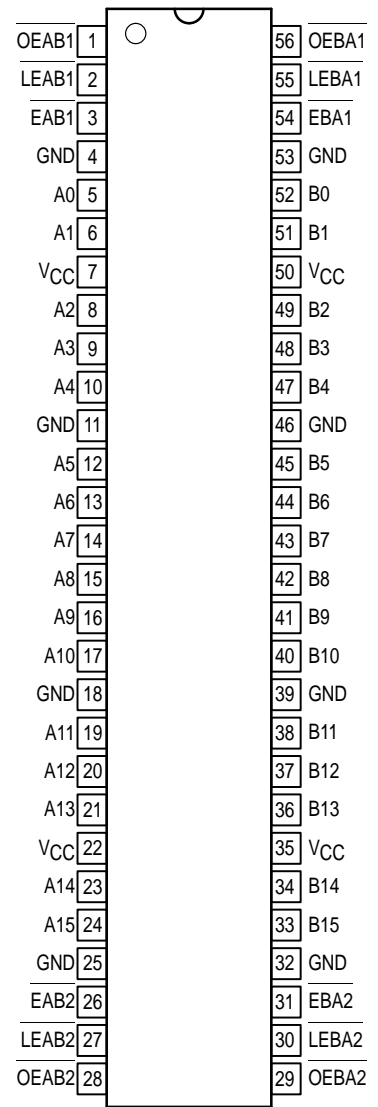
This document contains information on a new product. Specifications and information herein are subject to change without notice.



LOGIC DIAGRAM



Pinout: 56-Lead TSSOP
(Top View)



FUNCTION TABLE

| Inputs | | | | | | Data Ports | | Operating Mode | |
|--------|-------|------|-------|-------|--------|------------|--------|-----------------------------|-----------------------------|
| OEABn | OEBAn | EABn | EBAAn | LEABn | LEBAAn | An | Bn | | |
| H | H | | | | | Input | Input | | |
| | | X | X | X | X | X | X | Disable Outputs | |
| | | L | L | L | L | L | L | X | X |
| H | H | | | l | h | l | h | Latch and Outputs Disabled | |
| L | H | | | | | Input | Output | | |
| | | H | X* | L | X | l | Z | Z | Load and B Outputs Disabled |
| | | | | H | X | X | X | Z | Hold; B Outputs Disabled |
| | | L | X* | L | X | L | H | L | H |
| H | X | | | l | h | L | H | Latch and Display B Outputs | |
| H | L | | | | | Output | Input | | |
| | | X* | H | X | L | Z | l | h | Load and A Outputs Disabled |
| | | | | X | H | Z | X | X | Hold; A Outputs Disabled |
| | | X* | L | X | L | L | H | L | H |
| X | H | | | L | h | l | h | Latch and Display A Outputs | |

H = High Voltage Level; h = High Voltage Level One Setup Time Prior to the Latch Enable or Enable Low-to-High Transition; L = Low Voltage Level; l = Low Voltage Level One Setup Time Prior to the Latch Enable or Enable Low-to-High Transition; X = Don't Care; * = The latches are not internally gated with the Output Enables. Therefore, data at the A or B ports may enter the latches at any time, provided that the LExx and Exx pins are set accordingly. For I_{CC} reasons, Do Not Float Inputs.

ABSOLUTE MAXIMUM RATINGS*

| Symbol | Parameter | Value | Condition | Unit |
|------------------|----------------------------------|---|----------------------------------|------|
| V _{CC} | DC Supply Voltage | -0.5 to +7.0 | | V |
| V _I | DC Input Voltage | -0.5 ≤ V _I ≤ +7.0 | | V |
| V _O | DC Output Voltage | -0.5 ≤ V _O ≤ +7.0 | Output in 3-State | V |
| | | -0.5 ≤ V _O ≤ V _{CC} + 0.5 | Note 1. | V |
| I _{IK} | DC Input Diode Current | -50 | V _I < GND | mA |
| I _{OK} | DC Output Diode Current | -50 | V _O < GND | mA |
| | | +50 | V _O > V _{CC} | mA |
| I _O | DC Output Source/Sink Current | ±50 | | mA |
| I _{CC} | DC Supply Current Per Supply Pin | ±100 | | mA |
| I _{GND} | DC Ground Current Per Ground Pin | ±100 | | mA |
| T _{STG} | Storage Temperature Range | -65 to +150 | | °C |

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

1. Output in HIGH or LOW State. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Typ | Max | Unit | |
|-----------------|--|---------------------|-----|------------------------|------|---|
| V _{CC} | Supply Voltage | Operating | 2.0 | 3.3 | 3.6 | V |
| | | Data Retention Only | 1.5 | 3.3 | 3.6 | |
| V _I | Input Voltage | 0 | | 5.5 | V | |
| V _O | Output Voltage (HIGH or LOW State) (3-State) | 0 | | V _{CC} 5.5 | V | |
| I _{OH} | HIGH Level Output Current, V _{CC} = 3.0V – 3.6V | | | –24 | mA | |
| I _{OL} | LOW Level Output Current, V _{CC} = 3.0V – 3.6V | | | 24 | mA | |
| I _{OH} | HIGH Level Output Current, V _{CC} = 2.7V – 3.0V | | | –12 | mA | |
| I _{OL} | LOW Level Output Current, V _{CC} = 2.7V – 3.0V | | | 12 | mA | |
| T _A | Operating Free–Air Temperature | –40 | | +85 | °C | |
| Δt/ΔV | Input Transition Rise or Fall Rate, V _{IN} from 0.8V to 2.0V, V _{CC} = 3.0V | 0 | | 10 | ns/V | |

DC ELECTRICAL CHARACTERISTICS

| Symbol | Characteristic | Condition | T _A = –40°C to +85°C | | Unit |
|------------------|---------------------------------------|--|---------------------------------|------|------|
| | | | Min | Max | |
| V _{IH} | HIGH Level Input Voltage (Note 2.) | 2.7V ≤ V _{CC} ≤ 3.6V | 2.0 | | V |
| V _{IL} | LOW Level Input Voltage (Note 2.) | 2.7V ≤ V _{CC} ≤ 3.6V | | 0.8 | V |
| V _{OH} | HIGH Level Output Voltage | 2.7V ≤ V _{CC} ≤ 3.6V; I _{OH} = –100μA | V _{CC} – 0.2 | | V |
| | | V _{CC} = 2.7V; I _{OH} = –12mA | 2.2 | | |
| | | V _{CC} = 3.0V; I _{OH} = –18mA | 2.4 | | |
| | | V _{CC} = 3.0V; I _{OH} = –24mA | 2.2 | | |
| V _{OL} | LOW Level Output Voltage | 2.7V ≤ V _{CC} ≤ 3.6V; I _{OL} = 100μA | | 0.2 | V |
| | | V _{CC} = 2.7V; I _{OL} = 12mA | | 0.4 | |
| | | V _{CC} = 3.0V; I _{OL} = 16mA | | 0.4 | |
| | | V _{CC} = 3.0V; I _{OL} = 24mA | | 0.55 | |
| I _I | Input Leakage Current | 2.7V ≤ V _{CC} ≤ 3.6V; 0V ≤ V _I ≤ 5.5V | | ±5.0 | μA |
| I _{OZ} | 3–State Output Current | 2.7 ≤ V _{CC} ≤ 3.6V; 0V ≤ V _O ≤ 5.5V; V _I = V _{IH} or V _{IL} | | ±5.0 | μA |
| I _{OFF} | Power–Off Leakage Current | V _{CC} = 0V; V _I or V _O = 5.5V | | 10 | μA |
| I _{CC} | Quiescent Supply Current | 2.7 ≤ V _{CC} ≤ 3.6V; V _I = GND or V _{CC} | | 20 | μA |
| | | 2.7 ≤ V _{CC} ≤ 3.6V; 3.6 ≤ V _I or V _O ≤ 5.5V | | ±20 | μA |
| ΔI _{CC} | Increase in I _{CC} per Input | 2.7 ≤ V _{CC} ≤ 3.6V; V _{IH} = V _{CC} – 0.6V | | 500 | μA |

2. These values of V_I are used to test DC electrical characteristics only.

AC CHARACTERISTICS (Note 3.; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$)

| Symbol | Parameter | Waveform | Limits | | | | Unit |
|--------------------------|--|----------|---|-----|------------------------|-----|------|
| | | | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ | | | | |
| | | | $V_{CC} = 3.0\text{V to } 3.6\text{V}$ | | $V_{CC} = 2.7\text{V}$ | | |
| | | | Min | Max | Min | Max | |
| t_{PLH} t_{PHL} | Propagation Delay An to Bn or Bn to An | 1 | 1.5 | 5.2 | 1.5 | 6.0 | ns |
| t_{PLH} t_{PHL} | Propagation Delay LEBAn to An or LEABn to Bn | 4 | 1.5 | 6.5 | 1.5 | 7.5 | ns |
| t_{PZH} t_{PZL} | Output Enable Time OEBAAn to An or OEABn to Bn | 2 | 1.5 | 6.5 | 1.5 | 7.0 | ns |
| t_{PHZ} t_{PLZ} | Output Disable Time OEBAAn to An or OEABn to Bn | 2 | 1.5 | 6.5 | 1.5 | 7.0 | ns |
| t_{PZH} t_{PZL} | Output Enable Time EBAAn to An or EABn to Bn | 2 | 1.5 | 6.5 | 1.5 | 7.0 | ns |
| t_{PHZ} t_{PLZ} | Output Disable Time EBAAn to An or EABn to Bn | 2 | 1.5 | 6.5 | 1.5 | 7.0 | ns |
| t_s | Setup Time, HIGH to LOW Data to LE $_{xxn}$ | 4 | 2.5 | | 2.5 | | ns |
| t_h | Hold Time, HIGH to LOW Data to LE $_{xxn}$ | 4 | 1.5 | | 1.5 | | ns |
| t_s | Setup Time, HIGH to LOW Data to E $_{xxn}$ | 4 | 2.5 | | 2.5 | | ns |
| t_h | Hold Time, HIGH to LOW Data to E $_{xxn}$ | 4 | 1.5 | | 1.5 | | ns |
| t_w | Latch Enable or Enable Pulse Width, LOW | 4 | 3.0 | | 3.0 | | ns |
| t_{OSHL} t_{OSLH} | Output-to-Output Skew (Note 4.) | | | 1.0 | | | ns |

3. These AC parameters are preliminary and may be modified prior to release. The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.
4. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

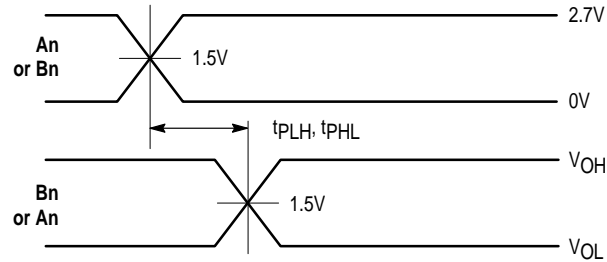
DYNAMIC SWITCHING CHARACTERISTICS

| Symbol | Characteristic | Condition | $T_A = +25^\circ\text{C}$ | | | Unit |
|-----------|--------------------------------------|--|---------------------------|-----|-----|------|
| | | | Min | Typ | Max | |
| V_{OLP} | Dynamic LOW Peak Voltage (Note 5.) | $V_{CC} = 3.3\text{V}$, $C_L = 50\text{pF}$, $V_{IH} = 3.3\text{V}$, $V_{IL} = 0\text{V}$ | | 0.8 | | V |
| V_{OLV} | Dynamic LOW Valley Voltage (Note 5.) | $V_{CC} = 3.3\text{V}$, $C_L = 50\text{pF}$, $V_{IH} = 3.3\text{V}$, $V_{IL} = 0\text{V}$ | | 0.8 | | V |

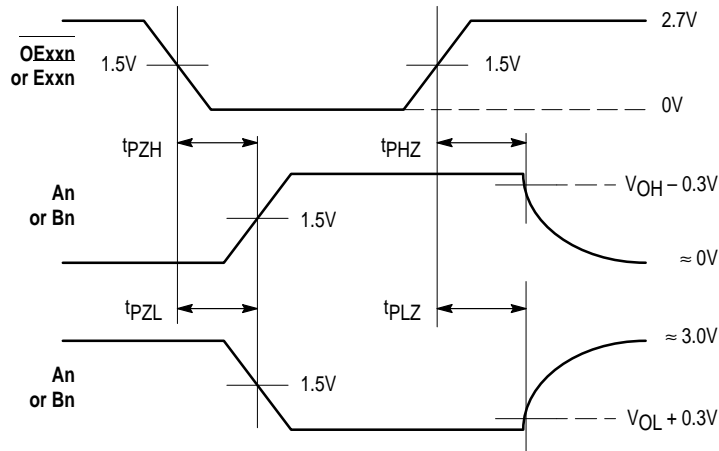
5. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

| Symbol | Parameter | Condition | Typical | Unit |
|-----------|-------------------------------|---|---------|------|
| C_{IN} | Input Capacitance | $V_{CC} = 3.3\text{V}$, $V_I = 0\text{V}$ or V_{CC} | 7 | pF |
| $C_{I/O}$ | Input/Output Capacitance | $V_{CC} = 3.3\text{V}$, $V_I = 0\text{V}$ or V_{CC} | 8 | pF |
| CPD | Power Dissipation Capacitance | 10MHz, $V_{CC} = 3.3\text{V}$, $V_I = 0\text{V}$ or V_{CC} | 20 | pF |

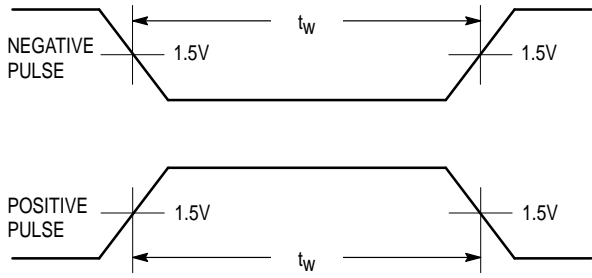


WAVEFORM 1 – A/B to B/A PROPAGATION DELAYS
 $t_R = t_F = 2.5\text{ns}$, 10% to 90%; $f = 1\text{MHz}$; $t_W = 500\text{ns}$

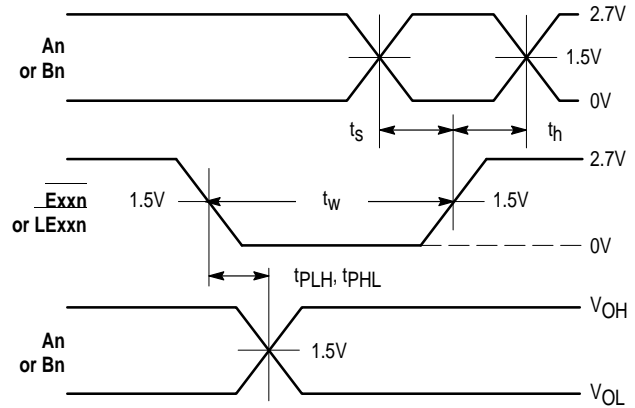


WAVEFORM 2 – OE_x/E_x to A or B OUTPUT ENABLE AND DISABLE TIMES
 $t_R = t_F = 2.5\text{ns}$, 10% to 90%; $f = 1\text{MHz}$; $t_W = 500\text{ns}$

Figure 1. AC Waveforms

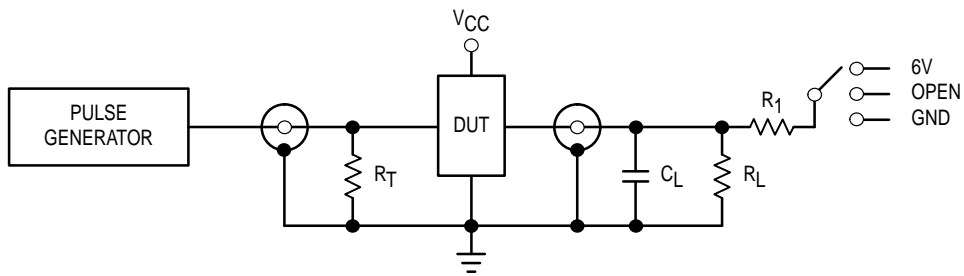


WAVEFORM 3 – INPUT PULSE DEFINITION
 $t_R = t_F = 2.5\text{ns}$, 10% to 90% of 0V to 2.7V



WAVEFORM 4 – Enable to A or B PROPAGATION DELAYS, Enable MINIMUM PULSE WIDTH, A or B to Enable SETUP AND HOLD TIMES
 $t_R = t_F = 2.5\text{ns}$, 10% to 90%; $f = 1\text{MHz}$; $t_W = 500\text{ns}$ except when noted

Figure 2. AC Waveforms (continued)



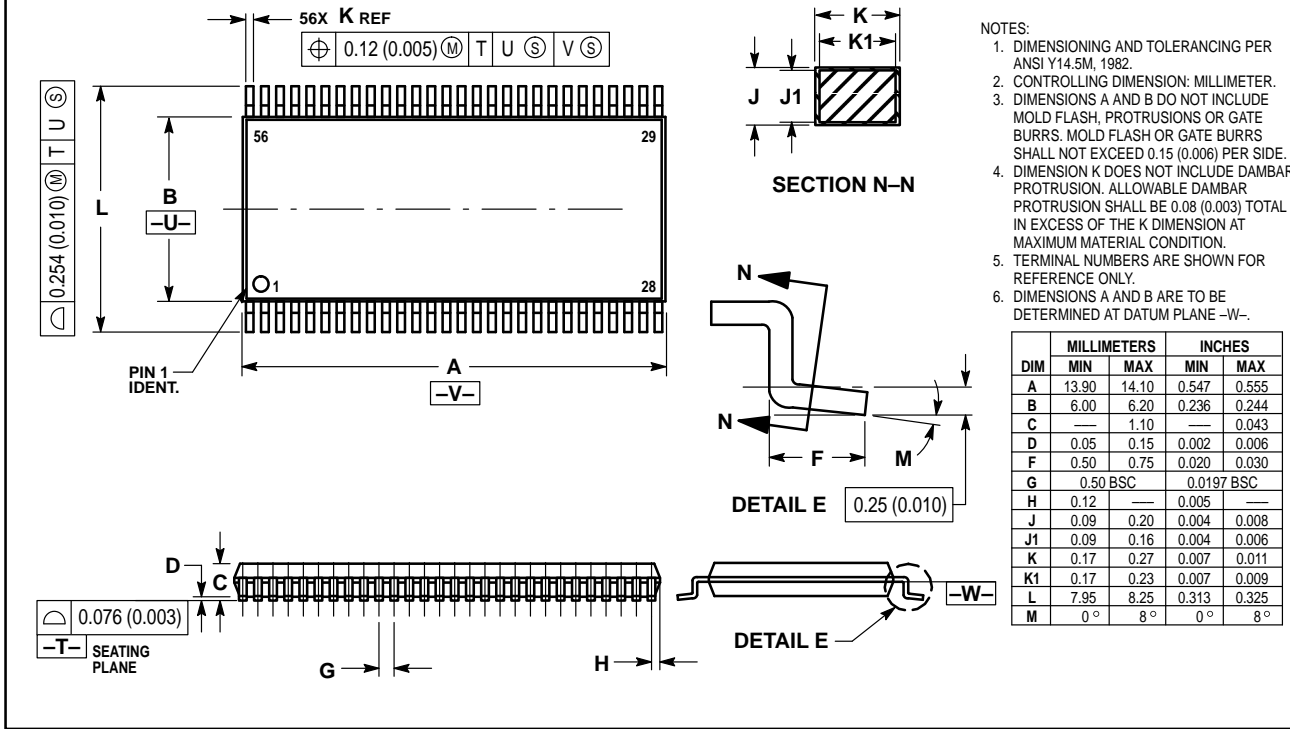
| TEST | SWITCH |
|--|--------|
| t_{PLH} , t_{PHL} | Open |
| t_{PZL} , t_{PLZ} | 6V |
| Open Collector/Drain t_{PLH} and t_{PHL} | 6V |
| t_{PZH} , t_{PHZ} | GND |

$C_L = 50\text{pF}$ or equivalent (Includes jig and probe capacitance)
 $R_L = R_1 = 500\Omega$ or equivalent
 $R_T = Z_{OUT}$ of pulse generator (typically 50 Ω)

Figure 3. Test Circuit

OUTLINE DIMENSIONS

DT SUFFIX
 PLASTIC TSSOP PACKAGE
 CASE 1202-01
 ISSUE A



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USA/EUROPE/Locations Not Listed: Motorola Literature Distribution;
 P.O. Box 5405, Denver, Colorado 80217. 1-800-441-2447

Mfax™: RMFAX0@email.sps.mot.com – TOUCHTONE 602-244-6609
INTERNET: http://Design-NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, 6F Seibu-Butsuryu-Center,
 3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-81-3521-8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

