

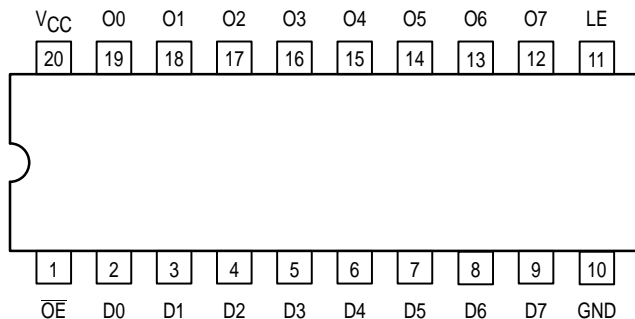
# Low-Voltage Quiet CMOS Octal Transparent Latch Flow Through Pinout (3-State, Non-Inverting)

The MC74LVQ573 is a high performance, non-inverting octal transparent latch operating from a 2.7 to 3.6V supply. The MC74LVQ573 is suitable for TTL level bus oriented applications where a memory element is required.

The MC74LVQ573 contains 8 D-type latches with 3-state standard outputs. When the Latch Enable (LE) input is HIGH, data on the Dn inputs enters the latches. In this condition, the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state standard outputs are controlled by the Output Enable ( $\overline{OE}$ ) input. When  $\overline{OE}$  is LOW, the standard outputs are enabled. When  $\overline{OE}$  is HIGH, the standard outputs are in the high impedance state, but this does not interfere with new data entering into the latches. The LVQ573 flow through design facilitates easy PC board layout.

- Designed for 2.7 to 3.6V  $V_{CC}$  Operation – Ideal for Low Power/Low Noise Applications
- Guaranteed Simultaneous Switching Noise Level and Dynamic Threshold Performance
- Guaranteed Skew Specifications
- Guaranteed Incident Wave Switching into 75Ω
- Low Static Supply Current (10μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V

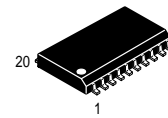
Pinout: 20-Lead (Top View)



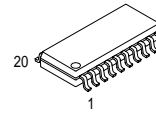
**MC74LVQ573**

**LVQ**

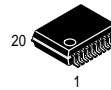
**LOW-VOLTAGE  
CMOS OCTAL  
TRANSPARENT LATCH**



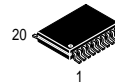
**DW SUFFIX**  
PLASTIC SOIC  
CASE 751D-04



**M SUFFIX**  
PLASTIC SOIC EIAJ  
CASE 967-01



**SD SUFFIX**  
PLASTIC SSOP  
CASE 940C-03

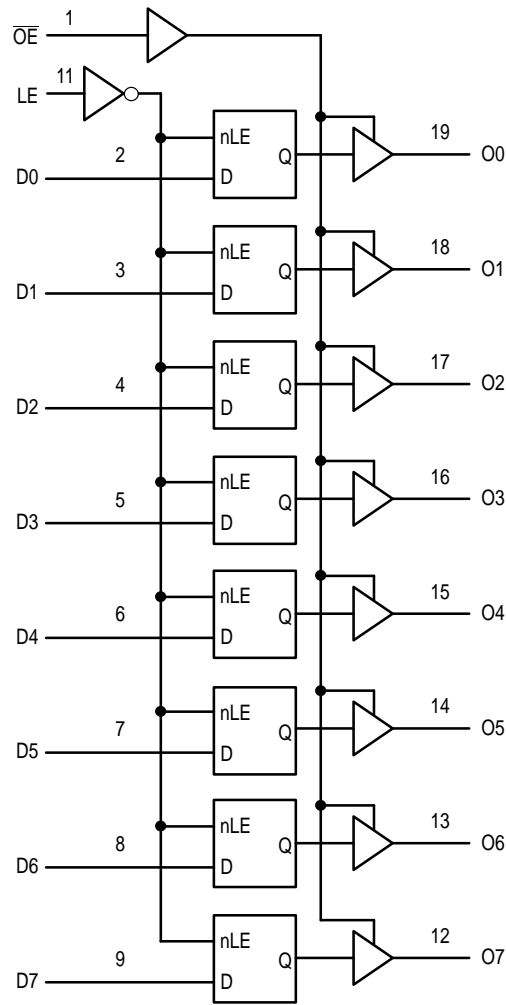


**DT SUFFIX**  
PLASTIC TSSOP  
CASE 948E-02

**PIN NAMES**

Pins	Function
$\overline{OE}$	Output Enable Input
LE	Latch Enable Input
D0–D7	Data Inputs
O0–O7	3-State Latch Outputs

LOGIC DIAGRAM



INPUTS			INTERNAL LATCHES	OUTPUTS	OPERATING MODE
$\overline{OE}$	LE	Dn	Q	On	
L L	H H	H L	H L	H L	Transparent (Latch Disabled); Read Latch
L L	L L	h l	H L	H L	Latched (Latch Enabled) Read Latch
L	L	X	NC	NC	Hold; Read Latch
H	L	X	NC	Z	Hold; Disabled Outputs
H H	H H	H L	H L	Z Z	Transparent (Latch Disabled); Disabled Outputs
H H	L L	h l	H L	Z Z	Latched (Latch Enabled); Disabled Outputs

H = High Voltage Level; h = High Voltage Level One Setup Time Prior to the Latch Enable High-to-Low Transition; L = Low Voltage Level; l = Low Voltage Level One Setup Time Prior to the Latch Enable High-to-Low Transition; NC = No Change; X = High or Low Voltage Level and Transitions are Acceptable; Z = High Impedance State; For I<sub>CC</sub> Reasons DO NOT FLOAT Inputs

**ABSOLUTE MAXIMUM RATINGS\***

Symbol	Parameter	Value	Condition	Unit
V <sub>CC</sub>	DC Supply Voltage	-0.5 to +7.0		V
V <sub>I</sub>	DC Input Voltage	-0.5 ≤ V <sub>I</sub> ≤ V <sub>CC</sub> + 0.5V		V
V <sub>O</sub>	DC Output Voltage	-0.5 ≤ V <sub>O</sub> ≤ V <sub>CC</sub> + 0.5	Output in HIGH or LOW State	V
I <sub>IK</sub>	DC Input Diode Current	-20	V <sub>I</sub> = -0.5V	mA
		+20	V <sub>I</sub> = V <sub>CC</sub> + 0.5V	mA
I <sub>OK</sub>	DC Output Diode Current	-20	V <sub>O</sub> = -0.5V	mA
		+20	V <sub>I</sub> = V <sub>CC</sub> + 0.5V	mA
I <sub>O</sub>	DC Output Source/Sink Current	±50		mA
I <sub>CC</sub>	DC Supply Current	±400		mA
I <sub>GND</sub>	DC Ground Current	±400		mA
T <sub>STG</sub>	Storage Temperature Range	-65 to +150		°C

\* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	2.0	3.3	3.6	V
V <sub>I</sub>	Input Voltage	0		V <sub>CC</sub>	V
V <sub>O</sub>	Output Voltage	0		V <sub>CC</sub>	V
T <sub>A</sub>	Operating Free-Air Temperature	-40		+85	°C
ΔV/Δt	Input Transition Rise or Fall Rate, V <sub>IN</sub> from 0.8V to 2.0V, V <sub>CC</sub> = 3.0V	0		125	mV/ns

**DC ELECTRICAL CHARACTERISTICS**

Symbol	Characteristic	Condition	T <sub>A</sub> = -40°C to +85°C		Unit
			Min	Max	
V <sub>IH</sub>	HIGH Level Input Voltage (Note 1)	2.7V ≤ V <sub>CC</sub> ≤ 3.6V, V <sub>O</sub> = 0.1V or V <sub>CC</sub> - 0.1V	2.0		V
V <sub>IL</sub>	LOW Level Input Voltage (Note 1)	2.7V ≤ V <sub>CC</sub> ≤ 3.6V, V <sub>O</sub> = 0.1V or V <sub>CC</sub> - 0.1V		0.8	V
V <sub>OH</sub>	HIGH Level Output Voltage	2.7V ≤ V <sub>CC</sub> ≤ 3.6V; I <sub>OH</sub> = -50μA	V <sub>CC</sub> - 0.1		V
		V <sub>CC</sub> = 2.7V; I <sub>OH</sub> = -12mA	2.2		
		V <sub>CC</sub> = 3.0V; I <sub>OH</sub> = -12mA	2.48		
V <sub>OL</sub>	LOW Level Output Voltage	2.7V ≤ V <sub>CC</sub> ≤ 3.6V; I <sub>OL</sub> = 50μA		0.1	V
		2.7V ≤ V <sub>CC</sub> ≤ 3.6V; I <sub>OL</sub> = 12mA		0.4	
I <sub>I</sub>	Input Leakage Current	2.7V ≤ V <sub>CC</sub> ≤ 3.6V; V <sub>I</sub> = V <sub>CC</sub> , GND		±1.0	μA
I <sub>OZ</sub>	Maximum 3-State Leakage Current	V <sub>I</sub> (OE) = V <sub>IL</sub> , V <sub>IH</sub> ; V <sub>I</sub> , V <sub>O</sub> = V <sub>CC</sub> , GND		±2.5	μA
I <sub>OLD</sub>	Minimum Dynamic Output Current (Note 2)	V <sub>CC</sub> = 3.6V; V <sub>OLD</sub> = 0.8V Max		36	mA
I <sub>OHD</sub>		V <sub>CC</sub> = 3.6V; V <sub>OHD</sub> = 2.0V Min		-25	mA
I <sub>CC</sub>	Quiescent Supply Current	2.7V ≤ V <sub>CC</sub> ≤ 3.6V; V <sub>I</sub> = V <sub>CC</sub> , GND		10	μA

1. These values of V<sub>I</sub> are used to test DC electrical characteristics only. Functional test should use V<sub>IH</sub> ≥ 2.4V, V<sub>IL</sub> ≤ 0.5V.
2. Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed. Maximum test duration is 2ms, one output loaded at a time.

**DYNAMIC SWITCHING CHARACTERISTICS** ( $V_{CC} = 3.3V$ )

Symbol	Characteristic	Condition	$T_A = +25^\circ C$			Unit
			Min	Typ	Max	
VOLP	Dynamic LOW Peak Voltage (Note 1)	$C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V$		0.6	1.0	V
VOLV	Dynamic LOW Valley Voltage (Note 1)	$C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V$		-0.5	-1.0	V
V <sub>I</sub> HD	High Level Dynamic Input Voltage (Note 2)	Input–Under–Test Switching 0V to Threshold, $f=1MHz$		1.5	2.0	V
V <sub>I</sub> LD	Low Level Dynamic Input Voltage (Note 2)	Input–Under–Test Switching 3.3V to Threshold, $f=1MHz$		1.5	0.8	V

- Number of outputs defined as “n”. Measured with “n–1” outputs switching from HIGH–to–LOW. The remaining output is measured in the LOW state.
- Number of data inputs is defined as “n” switching, “n–1” inputs switching 0V to 3.3V.

**AC CHARACTERISTICS** ( $t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500\Omega$ )

Symbol	Parameter	Limits									Unit
		$T_A = +25^\circ C$						$T_A = -40^\circ C \text{ to } +85^\circ C$			
		$V_{CC} = 3.0V \text{ to } 3.6V$			$V_{CC} = 2.7V$			$V_{CC} = 3.0V \text{ to } 3.6V$		$V_{CC} = 2.7V$	
		Min	Typ	Max	Min	Typ	Max	Min	Max	Max	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Dn to On	2.5 2.5	10.0 8.5	12.0 10.5	2.5 2.5	11.0 9.5	14.0 12.5	2.5 2.5	13.0 11.5	16.0 14.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay LE to On	2.5 2.5	10.0 8.5	12.5 11.0	2.5 2.5	11.0 10.0	14.5 13.5	2.5 2.5	13.5 12.0	15.5 14.5	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time to High and Low Level	2.5 2.5	8.0 8.0	10.0 10.0	2.5 2.5	9.0 9.0	11.5 11.5	2.5 2.5	10.5 10.5	12.0 12.0	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time From High and Low Level	1.0 1.0	9.5 6.5	12.0 9.0	1.0 1.0	11.0 7.0	13.5 10.0	1.0 1.0	12.5 10.0	14.5 11.0	ns
t <sub>O</sub> SHL t <sub>O</sub> SLH	Output–to–Output Skew (Note 1)		1.0 1.0	1.5 1.5		1.0 1.0	1.5 1.5		1.5 1.5		ns

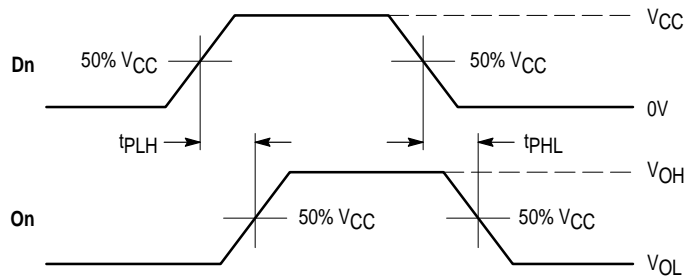
- Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t<sub>O</sub>SHL) or LOW–to–HIGH (t<sub>O</sub>SLH); parameter guaranteed by design.

**AC OPERATING REQUIREMENTS** ( $t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500\Omega$ )

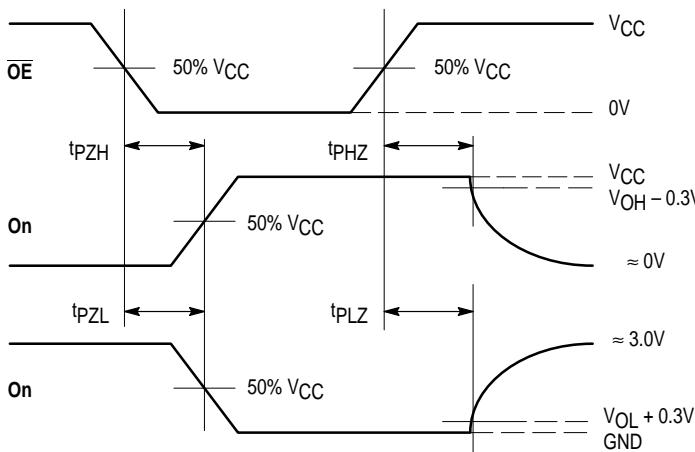
Symbol	Parameter	Limits				Unit
		$T_A = +25^\circ C$		$T_A = -40^\circ C \text{ to } +85^\circ C$		
		$V_{CC} = 3.0V \text{ to } 3.6V$		$V_{CC} = 2.7V$		
		Min	Min	Min	Min	
t <sub>s</sub>	Setup Time, HIGH or LOW Dn to LE	3.0		4.0		ns
t <sub>h</sub>	Hold Time, HIGH or LOW Dn to LE	1.5		1.5		ns
t <sub>w</sub>	LE Pulse Width, HIGH	4.0		5.0		ns

**CAPACITIVE CHARACTERISTICS**

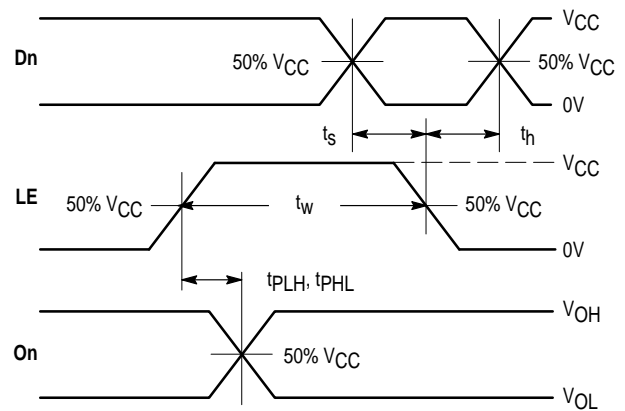
Symbol	Parameter	Condition	Typical	Unit
C <sub>PD</sub>	Power Dissipation Capacitance	10MHz, $V_{CC} = 3.3V, V_I = 0V \text{ or } V_{CC}$	30	pF
C <sub>IN</sub>	Input Capacitance	$V_{CC} = \text{Open}, V_I = 0V \text{ or } V_{CC}$	4.5	pF



**WAVEFORM 1 – PROPAGATION DELAYS**  
 $t_R = t_F = 2.5\text{ns}$ , 10% to 90%;  $f = 1\text{MHz}$ ;  $t_W = 500\text{ns}$

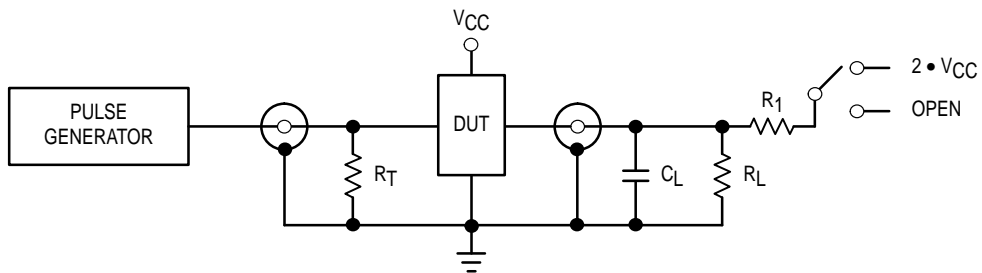


**WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES**  
 $t_R = t_F = 2.5\text{ns}$ , 10% to 90%;  $f = 1\text{MHz}$ ;  $t_W = 500\text{ns}$



**WAVEFORM 3 – LE to On PROPAGATION DELAYS, LE MINIMUM PULSE WIDTH, Dn to LE SETUP AND HOLD TIMES**  
 $t_R = t_F = 2.5\text{ns}$ , 10% to 90%;  $f = 1\text{MHz}$ ;  $t_W = 500\text{ns}$  except when noted

**Figure 1. AC Waveforms**



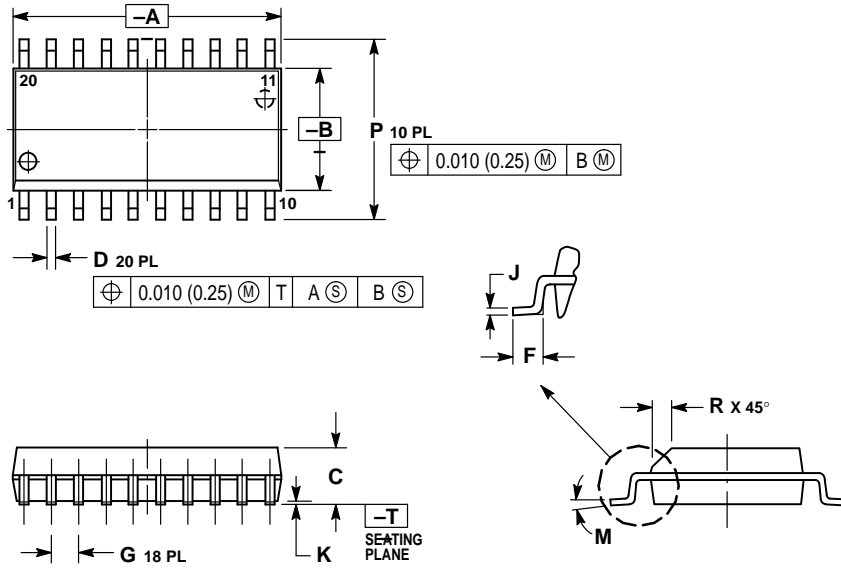
TEST	SWITCH
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PZL}$ , $t_{PLZ}$	$2 \cdot V_{CC}$
Open Collector/Drain $t_{PLH}$ and $t_{PHL}$	$2 \cdot V_{CC}$
$t_{PZH}$ , $t_{PHZ}$	Open

$C_L = 50\text{pF}$  or equivalent (Includes jig and probe capacitance)  
 $R_L = R_1 = 500\Omega$  or equivalent  
 $R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

**Figure 2. Test Circuit**

OUTLINE DIMENSIONS

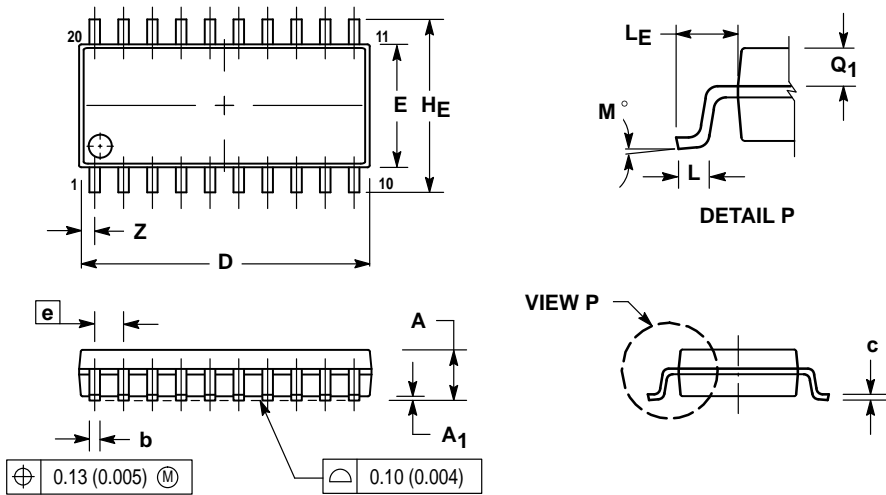
DW SUFFIX  
PLASTIC SOIC PACKAGE  
CASE 751D-04  
ISSUE E



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

M SUFFIX  
PLASTIC SOIC EIAJ PACKAGE  
CASE 967-01  
ISSUE O

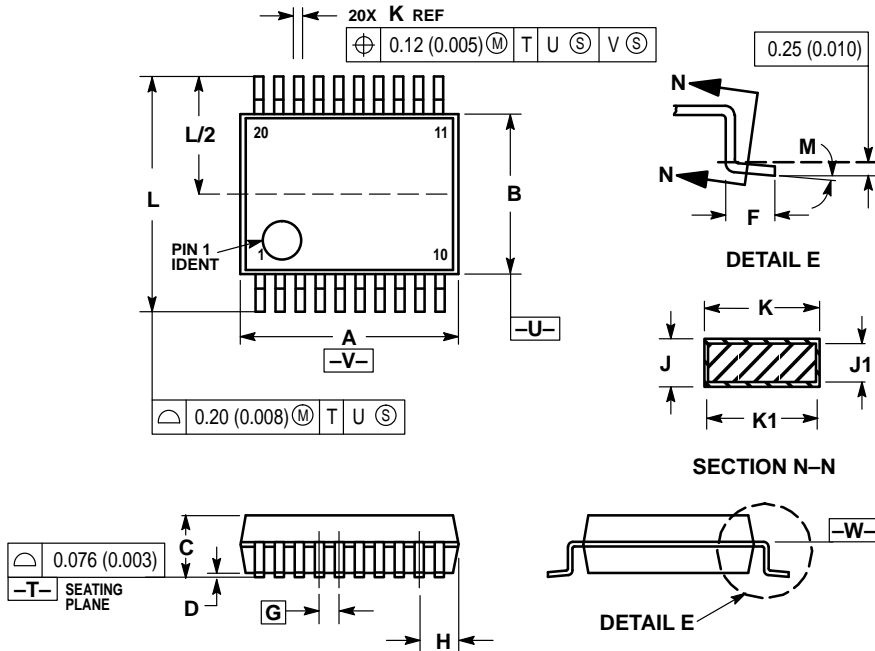


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A <sub>1</sub>	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L <sub>F</sub>	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q <sub>1</sub>	0.70	0.90	0.028	0.035
Z	---	0.81	---	0.032

OUTLINE DIMENSIONS

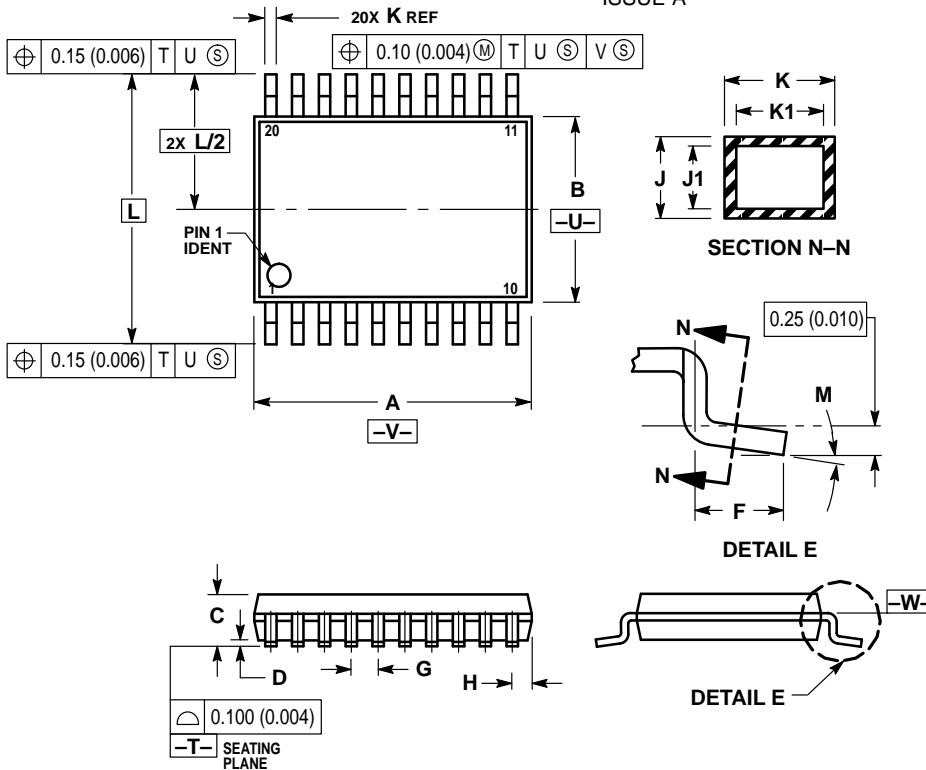
SD SUFFIX  
PLASTIC SSOP PACKAGE  
CASE 940C-03  
ISSUE B



- NOTES:
- 13 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  - 14 CONTROLLING DIMENSION: MILLIMETER.
  - 15 DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  - 16 DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  - 17 DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF K DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION K BY MORE THAN 0.07 (0.002) AT LEAST MATERIAL CONDITION.
  - 18 TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  - 19 DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	7.07	7.33	0.278	0.288
B	5.20	5.38	0.205	0.212
C	1.73	1.99	0.068	0.078
D	0.05	0.21	0.002	0.008
F	0.63	0.95	0.024	0.037
G	0.65 BSC		0.026 BSC	
H	0.59	0.75	0.023	0.030
J	0.09	0.20	0.003	0.008
J1	0.09	0.16	0.003	0.006
K	0.25	0.38	0.010	0.015
K1	0.25	0.33	0.010	0.013
L	7.65	7.90	0.301	0.311
M	0°	8°	0°	8°

DT SUFFIX  
PLASTIC TSSOP PACKAGE  
CASE 948E-02  
ISSUE A



- NOTES:
- 6 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  - 7 CONTROLLING DIMENSION: MILLIMETER.
  - 8 DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  - 9 DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  - 10 DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
  - 11 TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  - 12 DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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