

Low Skew CMOS PLL Clock Driver



The MC88915 Clock Driver utilizes phase-locked loop technology to lock its low skew outputs' frequency and phase onto an input reference clock. It is designed to provide clock distribution for high performance PC's and workstations.

The PLL allows the high current, low skew outputs to lock onto a single clock input and distribute it with essentially zero delay to multiple components on a board. The PLL also allows the MC88915 to multiply a low frequency input clock and distribute it locally at a higher (2X) system frequency. Multiple 88915's can lock onto a single reference clock, which is ideal for applications when a central system clock must be distributed synchronously to multiple boards (see Figure 7).

Five "Q" outputs (Q0-Q4) are provided with less than 500 ps skew between their rising edges. The Q5 output is inverted (180° phase shift) from the "Q" outputs. The 2X_Q output runs at twice the "Q" output frequency, while the Q/2 runs at 1/2 the "Q" frequency.

The VCO is designed to run optimally between 20 MHz and the 2X_Q Fmax specification. The wiring diagrams in Figure 5 detail the different feedback configurations which create specific input/output frequency relationships. Possible frequency ratios of the "Q" outputs to the SYNC input are 2:1, 1:1, and 1:2.

The **FREQ_SEL** pin provides one bit programmable divide-by in the feedback path of the PLL. It selects between divide-by-1 and divide-by-2 of the VCO before its signal reaches the internal clock distribution section of the chip (see the block diagram on page 2). In most applications **FREQ_SEL** should be held high (=1). If a low frequency reference clock input is used, holding **FREQ_SEL** low (=2) will allow the VCO to run in its optimal range (>20 MHz).

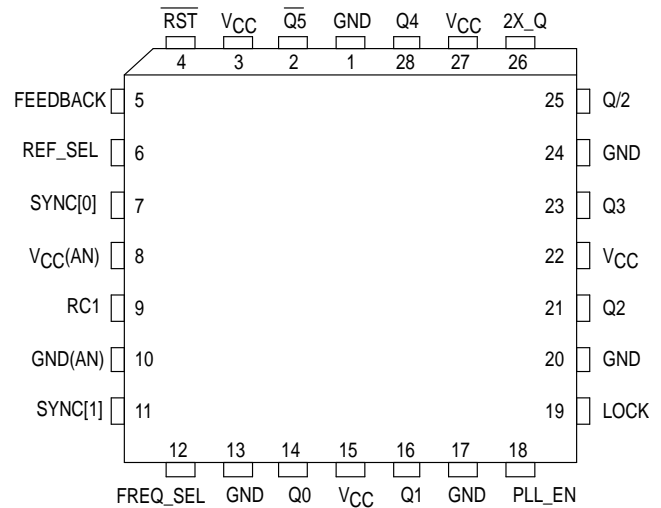
In normal phase-locked operation the **PLL_EN** pin is held high. Pulling the **PLL_EN** pin low disables the VCO and puts the 88915 in a static "test mode". In this mode there is no frequency limitation on the input clock, which is necessary for a low frequency board test environment. The second SYNC input can be used as a test clock input to further simplify board-level testing (see detailed description on page 11).

A lock indicator output (**LOCK**) will go high when the loop is in steady-state phase and frequency lock. The **LOCK** output will go low if phase-lock is lost or when the **PLL_EN** pin is low. Under certain conditions the lock output may remain low, even though the part is phase-locked. Therefore the **LOCK** output signal should not be used to drive any active circuitry; it should be used for passive monitoring or evaluation purposes only.

Yield Surface Modeling and YSM are trademarks of Motorola, Inc.

Features

- Five Outputs (Q0-Q4) with Output-Output Skew < 500 ps each being phase and frequency locked to the SYNC input
- The phase variation from part-to-part between the SYNC and FEEDBACK inputs is less than 550 ps (derived from the t_{PD} specification, which defines the part-to-part skew)
- Input/Output phase-locked frequency ratios of 1:2, 1:1, and 2:1 are available
- Input frequency range from 5MHz – 2X_Q FMAX spec
- Additional outputs available at 2X and +2 the system "Q" frequency. Also a Q (180° phase shift) output available
- All outputs have ±36 mA drive (equal high and low) at CMOS levels, and can drive either CMOS or TTL inputs. All inputs are TTL-level compatible
- Test Mode pin (**PLL_EN**) provided for low frequency testing. Two selectable **CLOCK** inputs for test or redundancy purposes



28-Lead Pinout (Top View)

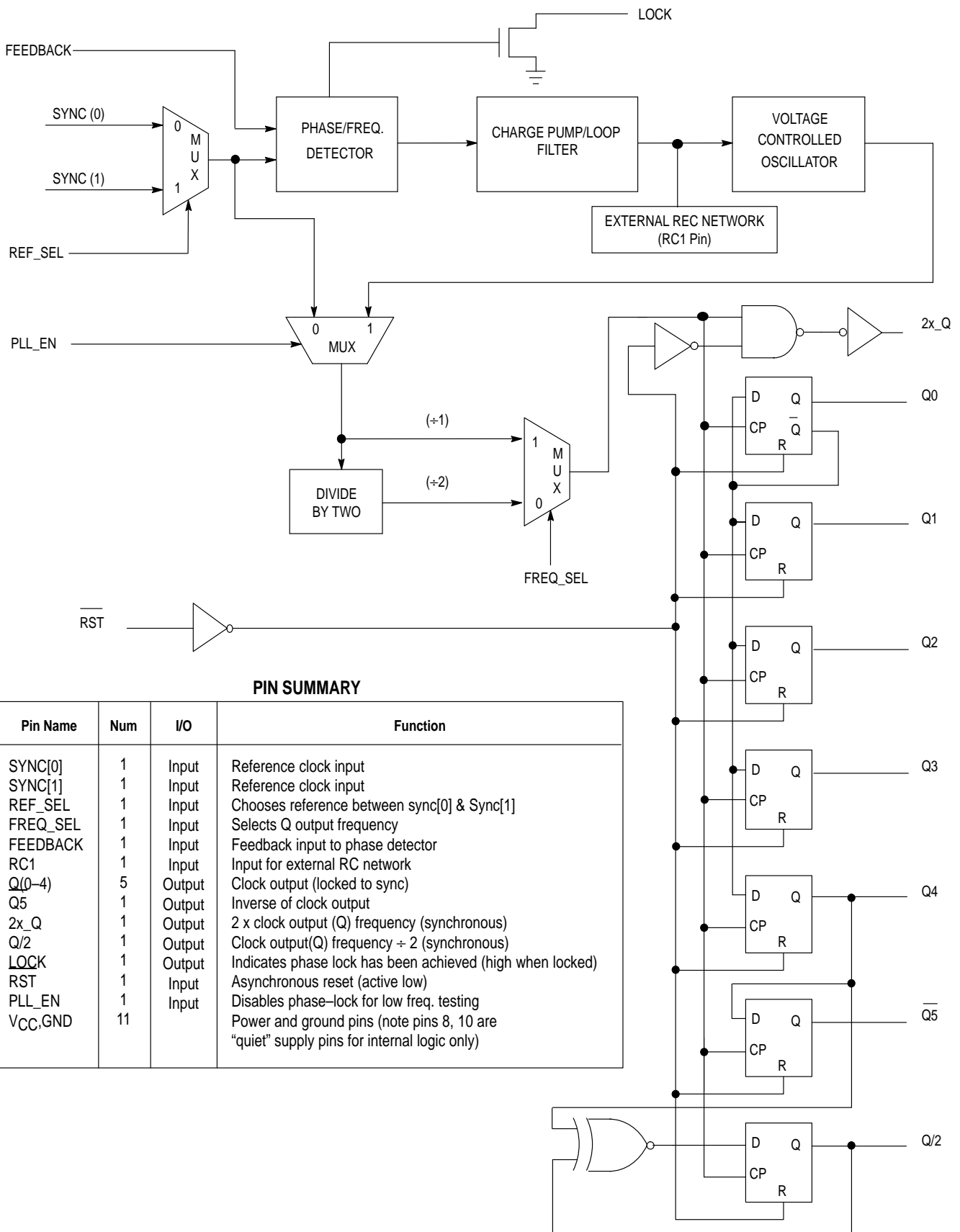
FN SUFFIX
PLASTIC PLCC
CASE 776-02

ORDERING INFORMATION

MC88915FN55 PLCC
MC88915FN70 PLCC



MC88915



MC88915 Block Diagram

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND; $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$)

| Symbol | Parameter | Test Conditions | V_{CC} V | Guaranteed Limit | Unit |
|-----------|--|---|---------------|------------------|---------------|
| V_{IH} | Minimum High-Level Input Voltage | $V_{out} = 0.1\text{V}$ or $V_{CC} - 0.1\text{V}$ | 4.75 5.25 | 2.0 2.0 | V |
| V_{IL} | Maximum Low-Level Input Voltage | $V_{out} = 0.1\text{V}$ or $V_{CC} - 0.1\text{V}$ | 4.75 5.25 | 0.8 0.8 | V |
| V_{OH} | Minimum High-Level Output Voltage | $V_{in} = V_{IH}$ or V_{IL} $I_{OH} = -36\text{mA}$ ¹ | 4.75 5.25 | 4.01 4.51 | V |
| V_{OL} | Maximum Low-Level Output Voltage | $V_{in} = V_{IH}$ or V_{IL} $I_{OL} = 36\text{mA}$ ¹ | 4.75 5.25 | 0.44 0.44 | V |
| I_{in} | Maximum Input Leakage Current | $V_I = V_{CC}$ or GND | 5.25 | ± 1.0 | μA |
| I_{CCT} | Maximum I_{CC} /Input | $V_I = V_{CC} - 2.1\text{V}$ | 5.25 | 1.5 ² | mA |
| I_{OLD} | Minimum Dynamic Output Current ³ | $V_{OLD} = 1.0\text{V}$ Max | 5.25 | 88 | mA |
| I_{OHD} | | $V_{OHD} = 3.85\text{V}$ Max | 5.25 | -88 | mA |
| I_{CC} | Maximum Quiescent Supply Current (per Package) | $V_I = V_{CC}$ or GND | 5.25 | 1.0 | mA |

- I_{OL} and I_{OH} are 12mA and -12mA respectively for the LOCK output.
- The PLL_EN input pin is not guaranteed to meet this specification.
- Maximum test duration is 2.0ms, one output loaded at a time.

CAPACITANCE AND POWER SPECIFICATIONS

| Symbol | Parameter | Typical Values | Unit | Conditions |
|----------|--|---------------------------------|------|--|
| C_{IN} | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0\text{V}$ |
| C_{PD} | Power Dissipation Capacitance | 40 | pF | $V_{CC} = 5.0\text{V}$ |
| PD_1 | Power Dissipation @ 33MHz with 50 Ω Thevenin Termination | 15 mW/Output 120 mW/Device | mW | $V_{CC} = 5.0\text{V}$ $T = 25^\circ\text{C}$ |
| PD_2 | Power Dissipation @ 33MHz with 50 Ω Parallel Termination to GND | 37.5 mW/Output 300 mW/Device | mW | $V_{CC} = 5.0\text{V}$ $T = 25^\circ\text{C}$ |

SYNC INPUT TIMING REQUIREMENTS

| Symbol | Parameter | Min | | Max | Unit |
|----------------------|--|---------------|------|------------------|------|
| t_{RISE}, t_{FALL} | Maximum Rise and Fall times, (SYNC Inputs: From 0.8V – 2.0V) | – | | 3.0 | ns |
| t_{CYCLE} | Input Clock Period (SYNC Inputs) | FN55 | FN70 | 200 ¹ | ns |
| | | 36 | 28.5 | | |
| Duty Cycle | Input Duty Cycle (SYNC Inputs) | 50% \pm 25% | | | |

- Information in Fig. 5 and in the "General AC Specification Notes", Note #3 describes this specification and its actual limits depending on the application.

FREQUENCY SPECIFICATIONS ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$, $C_L = 50\text{pF}$)

| Symbol | Parameter | Guaranteed Minimum | | Unit |
|------------------------|--|--------------------|-------------|------|
| | | MC88915FN55 | MC88915FN70 | |
| f_{max} ¹ | Maximum Operating Frequency (2X_Q Output) | 55 | 70 | MHz |
| | Maximum Operating Frequency (Q0–Q4, Q5 Output) | 27.5 | 35 | MHz |

- Maximum Operating Frequency is guaranteed with the part in a phase-locked condition, and all outputs loaded at 50 pF.

AC ELECTRICAL CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$, $C_L = 50\text{pF}$)

| Symbol | Parameter | Min | Max | Unit |
|---|--|--|----------------------|------|
| t_{RISE}, t_{FALL} (Outputs) | Rise and Fall Times, all Outputs Into a 50 pF, 500 Ω Load (Between $0.2V_{CC}$ and $0.8V_{CC}$) | 1.0 | 2.5 | ns |
| t_{RISE}, t_{FALL} ³ (2X_Q Output) | Rise and Fall Time, 2X_Q Output Into a 20 pF Load With Termination specified in note 2 (Between 0.8 V and 2.0 V) | 0.5 | 1.6 | ns |
| $t_{Pulse\ Width}$ ³ (Q0, Q1, Q3, Q4, Q5, Q/2) | Output Pulse Width (Q0, Q1, Q3, Q4, Q5, Q/2 @ $V_{CC}/2$) | $0.5t_{CYCLE} - 0.5$ | $0.5t_{CYCLE} + 0.5$ | ns |
| | | $t_{CYCLE} = 1/\text{Freq. at which the "Q"}$ Outputs are running | | |
| $t_{Pulse\ Width}$ ³ (Q2 only) | Output Pulse Width (Q2 Output @ $V_{CC}/2$) | $0.5t_{CYCLE} - 0.6$ | $0.5t_{CYCLE} + 0.6$ | |
| $t_{Pulse\ Width}$ ³ (2X_Q Output) | Output Pulse Width (2X_Q Output @ 1.5 V) (See AC Note 2) | $0.5t_{CYCLE} - 0.5$ | $0.5t_{CYCLE} + 0.5$ | ns |
| $t_{Pulse\ Width}$ ³ (2X_Q Output) | Output Pulse Width (2X_Q Output @ $V_{CC}/2$) | $0.5t_{CYCLE} - 1.0$ | $0.5t_{CYCLE} + 1.0$ | ns |
| t_{PD} ³ (Sync-Feedback) | SYNC input to feedback delay (meas. @ SYNC0 or 1 and FEEDBACK input pins) (See General AC Specification note 4 and Fig. 2 for explanation) | (470k Ω From RC1 to An.V _{CC}) | | ns |
| | | -1.05 | -0.50 | |
| | | (470k Ω From RC1 to An.GND) | | |
| | | +1.25 | +3.25 | |
| t_{SKEW_r} ^{1,3} (Rising) | Output-to-Output Skew Between Outputs Q0 – Q4, Q/2 (Rising Edges Only) | – | 500 | ps |
| t_{SKEW_f} ^{1,3} (Falling) | Output-to-Output Skew Between Outputs Q0 – Q4 (Falling Edges Only) | – | 750 | ps |
| $t_{SKEW_{all}}$ ^{1,3} | Output-to-Output Skew Between Outputs 2X_Q, Q/2, Q0 – Q4 Rising, Q5 Falling | – | 750 | ps |
| t_{LOCK} | Time Required to acquire ² Phase-Lock from time SYNC Input Signal is Received. | 1 | 10 | ms |
| t_{PHL} (Reset – Q) | Propagation Delay, RST to Any Output (High-Low) | 1.5 | 13.5 | ns |

- Under equally loaded conditions, $C_L \leq 50\text{pF}$ ($\pm 2\text{pF}$), and at a fixed temperature and voltage.
- With V_{CC} fully powered-on and an output properly connected to the FEEDBACK pin. t_{LOCK} Max. is with $C1 = 0.1\mu\text{F}$, t_{LOCK} Min is with $C1 = 0.01\mu\text{F}$.
- These specifications are not tested, they are guaranteed by statistical characterization. See General AC Specification note 1.

RESET TIMING REQUIREMENTS ¹

| Symbol | Parameter | Minimum | Unit |
|---------------------------|--|---------|------|
| $t_{REC, RST}$ to SYNC | Reset Recovery Time rising RST edge to falling SYNC edge | 9.0 | ns |
| $t_{W, RST}$ LOW | Minimum Pulse Width, RST input LOW | 5.0 | ns |

- These reset specs are valid only when PLL_EN is LOW and the part is in Test mode (not in phase-lock)

General AC Specification Notes

1. Several specifications can only be measured when the MC88915 is in phase-locked operation. It is not possible to have the part in phase-lock on ATE (automated test equipment). Statistical characterization techniques were used to guarantee those specifications which cannot be measured on the ATE. MC88915 units were fabricated with key transistor properties intentionally varied to create a 14 cell designed experimental matrix. IC performance was characterized over a range of transistor properties (represented by the 14 cells) in excess of the expected process variation of the wafer fabrication area. Response Surface Modeling (RSM) techniques were used to relate IC performance to the CMOS transistor properties over operation voltage and temperature. IC Performance to each specification and fab variation were used in conjunction with Yield Surface Modeling™ (YSM™) methodology to set performance limits of ATE testable specifications within those which are to be guaranteed by

statistical characterization. In this way all units passing the ATE test will meet or exceed the non-tested specifications limits.

2. These two specs (tRISE/FALL and tPULSE Width 2X_Q output) guarantee that the MC88915 meets the 25 MHz 68040 P-Clock input specification (at 50 MHz). For these two specs to be guaranteed by Motorola, the termination scheme shown below in Figure 1 must be used.
3. The wiring Diagrams and written explanations in Figure 5 demonstrate the input and output frequency relationships for three possible feedback configurations. The allowable SYNC input range for each case is also indicated. There are two allowable SYNC frequency ranges, depending whether FREQ_SEL is high or low. Although not shown, it is possible to feed back the Q5 output, thus creating a 180° phase shift between the SYNC input and the “Q” outputs. Table 1 below summarizes the allowable SYNC frequency range for each possible configuration.

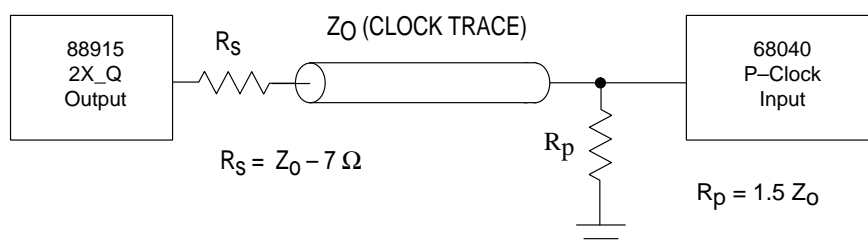


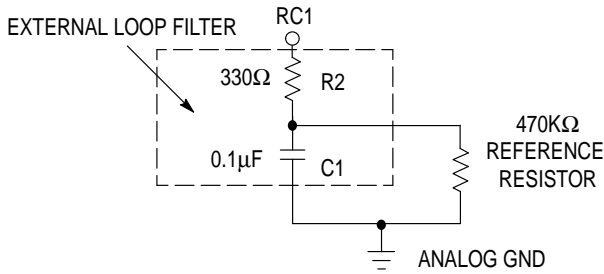
Figure 1. MC68040 P-Clock Input Termination Scheme

| FREQ_SEL Level | Feedback Output | Allowable SYNC Input Frequency Range (MHZ) | Corresponding VCO Frequency Range | Phase Relationships of the “Q” Outputs to Rising SYNC Edge |
|----------------|-----------------|--|-----------------------------------|--|
| HIGH | Q/2 | 5 to (2X_Q FMAX Spec)/4 | 20 to (2X_Q FMAX Spec) | 0° |
| HIGH | Any “Q” (Q0–Q4) | 10 to (2X_Q FMAX Spec)/2 | 20 to (2X_Q FMAX Spec) | 0° |
| HIGH | Q5 | 10 to (2X_Q FMAX Spec)/2 | 20 to (2X_Q FMAX Spec) | 180° |
| HIGH | 2X_Q | 20 to (2X_Q FMAX Spec) | 20 to (2X_Q FMAX Spec) | 0° |
| LOW | Q/2 | 2.5 to (2X_Q FMAX Spec)/8 | 20 to (2X_Q FMAX Spec) | 0° |
| LOW | Any “Q” (Q0–Q4) | 5 to (2X_Q FMAX Spec)/4 | 20 to (2X_Q FMAX Spec) | 0° |
| LOW | Q5 | 5 to (2X_Q FMAX Spec)/4 | 20 to (2X_Q FMAX Spec) | 180° |
| LOW | 2X_Q | 10 to (2X_Q FMAX Spec)/2 | 20 to (2X_Q FMAX Spec) | 0° |

Table 1. Allowable SYNC Input Frequency Ranges for Different Feedback Configurations.

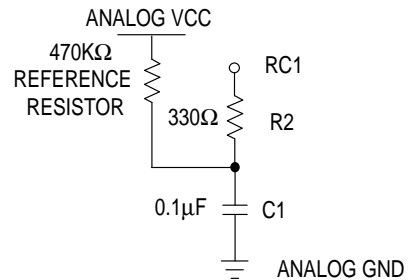
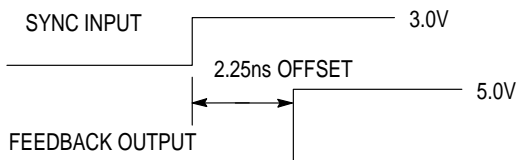
4. A 1 MΩ resistor tied to either Analog V_{CC} or Analog GND as shown in Figure 2 is required to ensure no jitter is present on the MC88915 outputs. This technique causes a phase offset between the SYNC input and the output connected to the FEEDBACK input, measured at the input pins. The t_{PD} spec describes how this offset varies with process, temperature, and voltage. The specs were arrived at by measuring the phase relationship for the 14

lots described in note 1 while the part was in phase-locked operation. The actual measurements were made with a 10 MHz SYNC input (1.0 ns edge rate from 0.8 V – 2.0 V) with the Q/2 output fed back. The phase measurements were made at 1.5 V. The Q/2 output was terminated at the FEEDBACK input with 100Ω to V_{CC} and 100 Ω to ground.



With the 470KΩ resistor tied in this fashion, the t_{PD} specification measured at the input pins is:

$$t_{PD} = 2.25\text{ns} \pm 1.0\text{ns}$$



With the 470KΩ resistor tied in this fashion, the t_{PD} specification measured at the input pins is:

$$t_{PD} = -0.775\text{ns} \pm 0.275\text{ns}$$

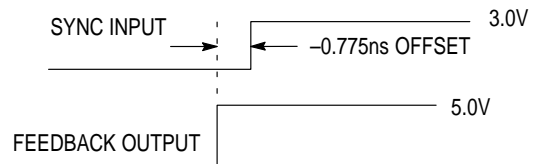


Figure 2. Depiction of the Fixed SYNC to Feedback Offset (t_{PD}) Which is Present When a 470KΩ Resistor is Tied to VCC or Ground

5. The t_{SKEW_r} specification guarantees that the rising edges of outputs Q/2, Q0, Q1, Q2, Q3, and Q4 will always fall within a 500ps window within one part. However, if the relative position of each output within this window is not specified, the 500 ps window must be added to each side of the t_{PD} specification limits to calculate the total part-to-part skew. For this reason the absolute

distribution of these outputs are provided in table 2. When taking the skew data, Q0 was used as a reference, so all measurements are relative to this output. The information in Table 2 is derived from measurements taken from the 14 process lots described in Note 1, over the temperature and voltage range.

| Output | - (ps) | + (ps) |
|--------|--------|--------|
| Q0 | 0 | 0 |
| Q1 | -72 | 40 |
| Q2 | -44 | 276 |
| Q3 | -40 | 255 |
| Q4 | -274 | -34 |
| Q/2 | -16 | 250 |
| 2X_Q | -633 | -35 |

Table 2. Relative Positions of Outputs Q/2, Q0–Q4, 2X_Q, Within the 500ps t_{SKEW_r} Spec Window

6. Calculation of Total Output-to-Skew between multiple parts (Part-to-Part skew)

By combining the t_{PD} specification and the information in Note 5, the worst case output-to-output skew between multiple 88915's connected in parallel can be calculated. This calculation assumes that all parts have a common SYNC input clock with equal delay of that input signal to each part. This skew value is valid at the 88915 output pins only (equally loaded), it does not include PCB trace delays due to varying loads.

With a $1M\Omega$ resistor tied to analog V_{CC} as shown in note 4, the t_{PD} spec. limits between SYNC and the Q/2 output (connected to the FEEDBACK pin) are $-1.05ns$ and $-0.5ns$. To calculate the skew of any given output between two or more parts, the absolute value of the distribution of that output given in table 2 must be subtracted and added to the lower and upper t_{PD} spec limits respectively. For output Q2, $[276 - (-44)] = 320ps$ is the absolute value of the distribution. Therefore $[-1.05ns$

$-0.32ns] = -1.37ns$ is the lower t_{PD} limit, and $[-0.5ns + 0.32ns] = -0.18ns$ is the upper limit. Therefore the worst case skew of output Q2 between any number of parts is $|(-1.37) - (-0.18)| = 1.19ns$. Q2 has the worst case skew distribution of any output, so $1.2ns$ is the absolute worst case output-to-output skew between multiple parts.

7. Note 4 explains that the t_{PD} specification was measured and is guaranteed for the configuration of the Q/2 output connected to the FEEDBACK pin and the SYNC input running at 10MHz. The fixed offset (t_{PD}) as described above has some dependence on the input frequency and at what frequency the VCO is running. The graphs of Figure 3 demonstrate this dependence.

The data presented in Figure 3 is from devices representing process extremes, and the measurements were also taken at the voltage extremes ($V_{CC} = 5.25V$ and $4.75V$). Therefore the data in Figure 3 is a realistic representation of the variation of t_{PD} .

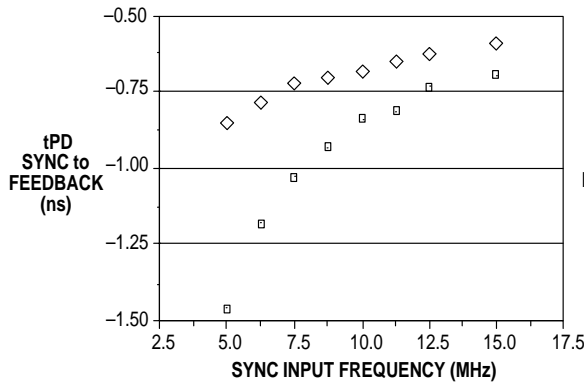


Figure 3a.

t_{PD} versus Frequency Variation for Q/2 Output Fed Back, Including Process and Voltage Variation @ 25°C (With $1M\Omega$ Resistor Tied to Analog V_{CC})

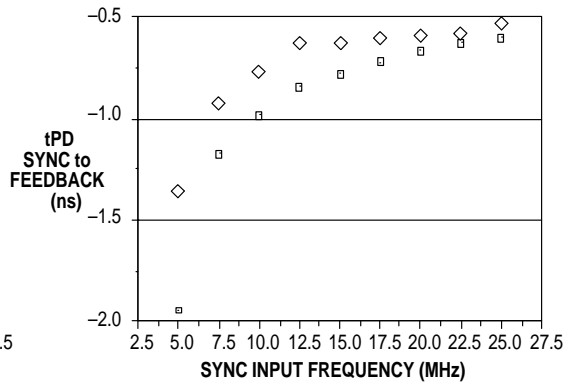


Figure 3b.

t_{PD} versus Frequency Variation for Q4 Output Fed Back, Including Process and Voltage Variation @ 25°C (With $1M\Omega$ Resistor Tied to Analog V_{CC})

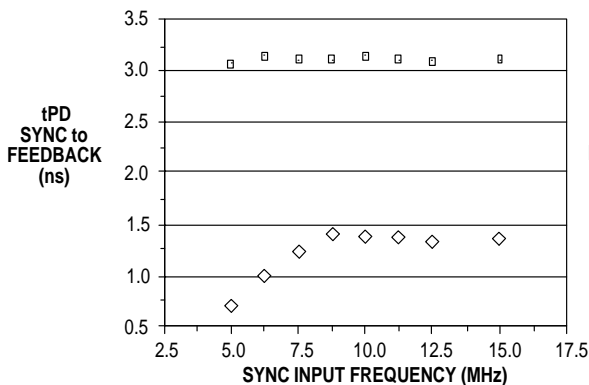


Figure 3c.

t_{PD} versus Frequency Variation for Q/2 Output Fed Back, Including Process and Voltage Variation @ 25°C (With $1M\Omega$ Resistor Tied to Analog GND)

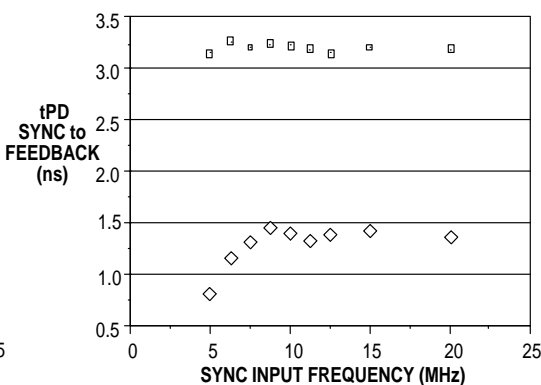


Figure 3d.

t_{PD} versus Frequency Variation for Q4 Output Fed Back, Including Process and Voltage Variation @ 25°C (With $1M\Omega$ Resistor Tied to Analog GND)

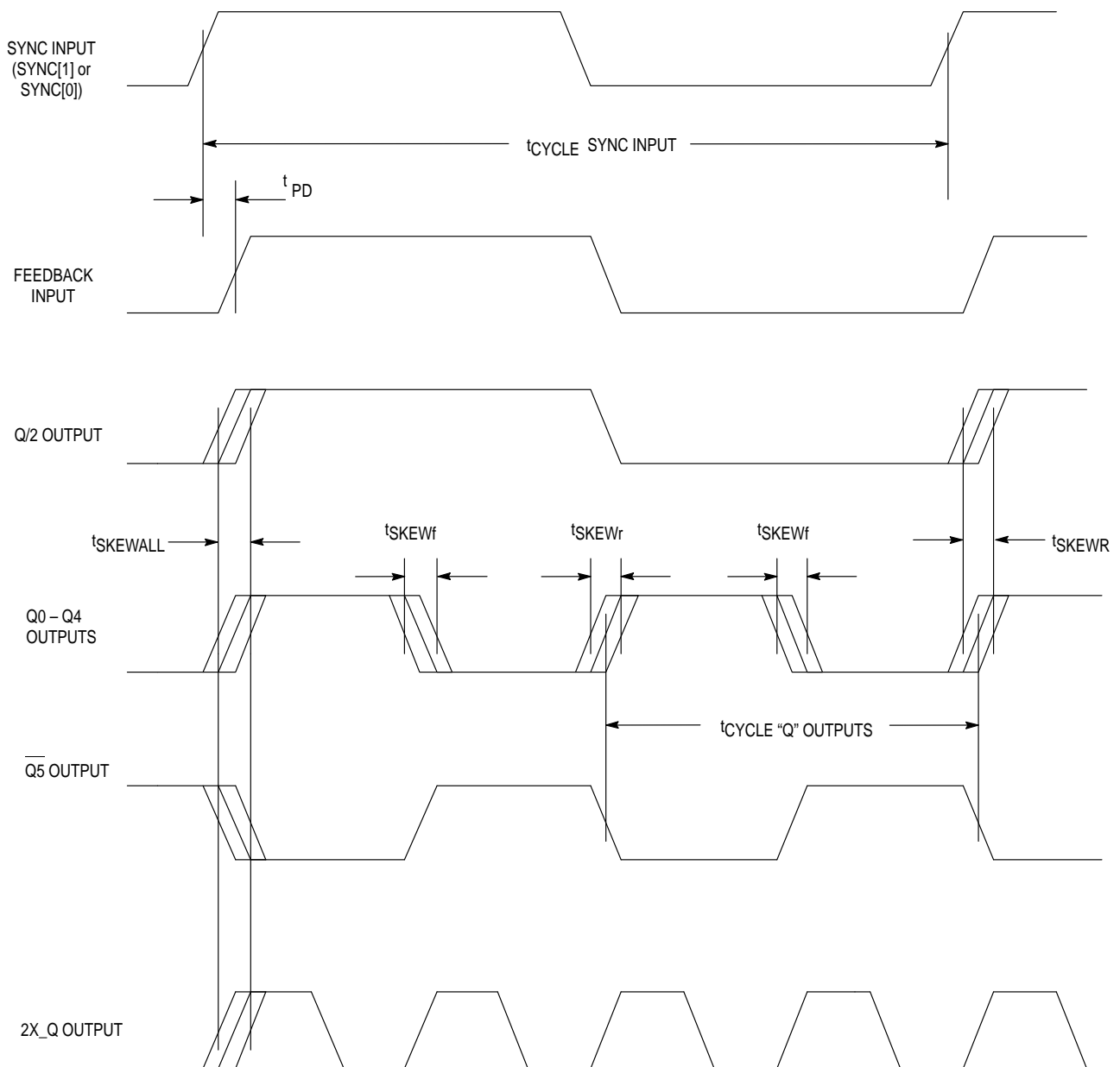
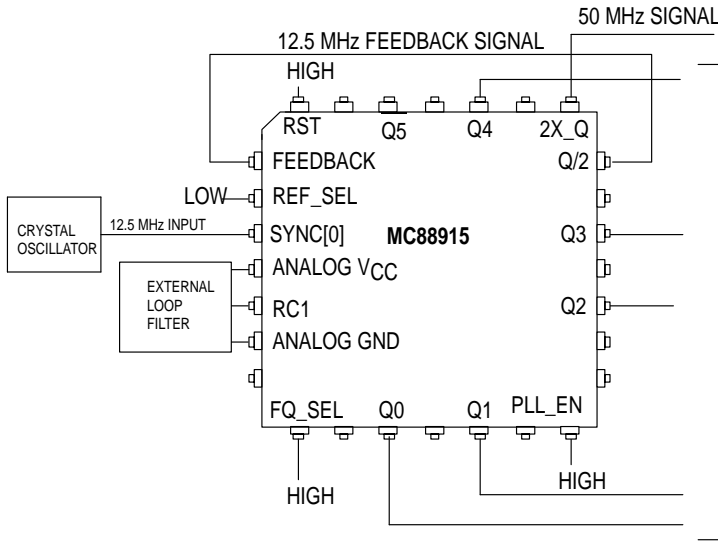


Figure 4. Output / Input Switching Waveforms and Timing Diagrams
 (These waveforms represent the hook-up configuration of Figure 5a on page 9)

Timing Notes:

- The MC88915 aligns rising edges of the FEEDBACK input and SYNC input, therefore the SYNC input does not require a 50% duty cycle.
- All skew specs are measured between the $V_{\text{CC}}/2$ crossing point of the appropriate output edges. All skews are specified as 'windows', not as a \pm deviation around a center point.
- If a "Q" output is connected to the FEEDBACK input (this situation is not shown), the "Q" output frequency would match the SYNC input frequency, the 2X_Q output would run at twice the SYNC frequency, and the Q/2 output would run at half the SYNC frequency.



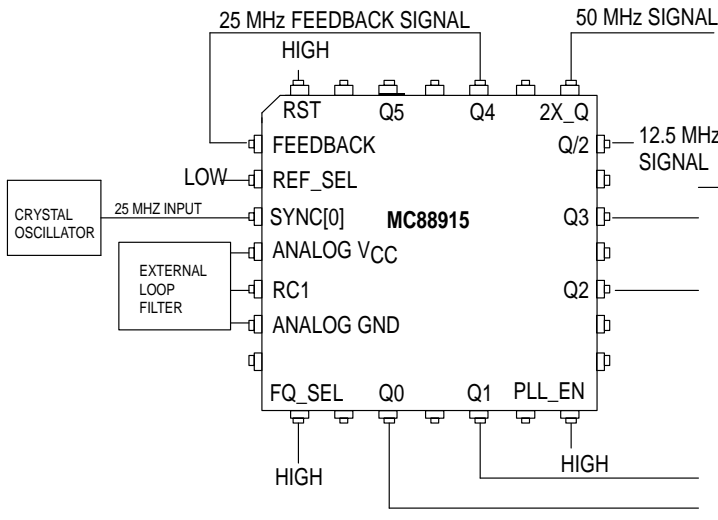
1:2 Input to “Q” Output Frequency Relationship

In this application, the Q/2 output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of Q/2 and SYNC, thus the Q/2 frequency will equal the SYNC frequency. The “Q” outputs (Q0–Q4, Q5) will always run at 2X the Q/2 frequency, and the 2X_Q output will run at 4X the Q/2 frequency.

Allowable Input Frequency Range:

5MHz to (2X_Q FMAX Spec)/4 (for FREQ_SEL HIGH)
2.5MHz to (2X_Q FMAX Spec)/8 (for FREQ_SEL LOW)

Figure 5a. Wiring Diagram and Frequency Relationships With Q/2 Output Feed Back



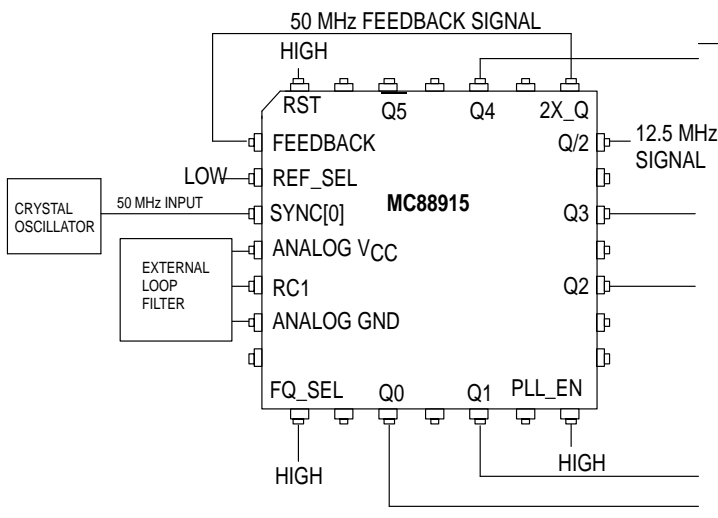
1:1 Input to “Q” Output Frequency Relationship

In this application, the Q4 output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of Q4 and SYNC, thus the Q4 frequency (and the rest of the “Q” outputs) will equal the SYNC frequency. The Q/2 output will always run at 1/2 the “Q” frequency, and the 2X_Q output will run at 2X the “Q” frequency.

Allowable Input Frequency Range:

10MHz to (2X_Q FMAX Spec)/2 (for FREQ_SEL HIGH)
5MHz to (2X_Q FMAX Spec)/4 (for FREQ_SEL LOW)

Figure 5b. Wiring Diagram and Frequency Relationships With Q4 Output Feed Back



2:1 Input to “Q” Output Frequency Relationship

In this application, the 2X_Q output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of 2X_Q and SYNC, thus the 2X_Q frequency will equal the SYNC frequency. The Q/2 output will always run at 1/4 the 2X_Q frequency, and the “Q” outputs will run at 1/2 the 2X_Q frequency.

Allowable Input Frequency Range:

20MHz to (2X_Q FMAX Spec) (for FREQ_SEL HIGH)
10MHz to (2X_Q FMAX Spec)/2 (for FREQ_SEL LOW)

Figure 5c. Wiring Diagram and Frequency Relationships with 2X_Q Output Feed Back

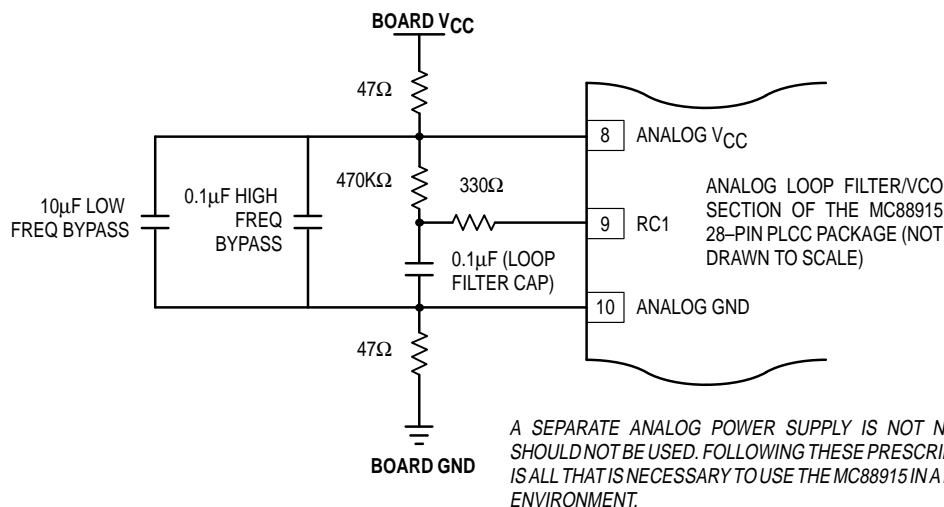


Figure 6. Recommended Loop Filter and Analog Isolation Scheme for the MC88915

Notes Concerning Loop Filter and Board Layout Issues

1. Figure 6 shows a loop filter and analog isolation scheme which will be effective in most applications. The following guidelines should be followed to ensure stable and jitter-free operation:

1a. All loop filter and analog isolation components should be tied as close to the package as possible. Stray current passing through the parasitics of long traces can cause undesirable voltage transients at the RC1 pin.

1b. The 47Ω resistors, the 10µF low frequency bypass capacitor, and the 0.1µF high frequency bypass capacitor form a wide bandwidth filter that will minimize the 88915's sensitivity to voltage transients from the system digital V_{CC} supply and ground planes. This filter will typically ensure that a 100mV step deviation on the digital V_{CC} supply will cause no more than a 100pS phase deviation on the 88915 outputs. A 250mV step deviation on V_{CC} using the recommended filter values should cause no more than a 250pS phase deviation; if a 25µF bypass capacitor is used (instead of 10µF) a 250mV V_{CC} step should cause no more than a 100pS phase deviation.

If good bypass techniques are used on a board design near components which may cause digital V_{CC} and ground noise, the above described V_{CC} step deviations should not occur at the 88915's digital V_{CC} supply. The purpose of the bypass filtering scheme shown in Figure 6

is to give the 88915 additional protection from the power supply and ground plane transients that can occur in a high frequency, high speed digital system.

1c. There are no special requirements set forth for the loop filter resistors (470K and 330Ω). The loop filter capacitor (0.1µF) can be a ceramic chip capacitor, the same as a standard bypass capacitor.

1d. The 470K reference resistor injects current into the internal charge pump of the PLL, causing a fixed offset between the outputs and the SYNC input. This also prevents excessive jitter caused by inherent PLL dead-band. If the VCO (2X_Q output) is running above 40MHz, the 470K resistor provides the correct amount of current injection into the charge pump (2–3µA). If the VCO is running below 40MHz, a 1MΩ reference resistor should be used (instead of 470K).

2. In addition to the bypass capacitors used in the analog filter of Figure 6, there should be a 0.1µF bypass capacitor between each of the other (digital) four V_{CC} pins and the board ground plane. This will reduce output switching noise caused by the 88915 outputs, in addition to reducing potential for noise in the 'analog' section of the chip. These bypass capacitors should also be tied as close to the 88915 package as possible.

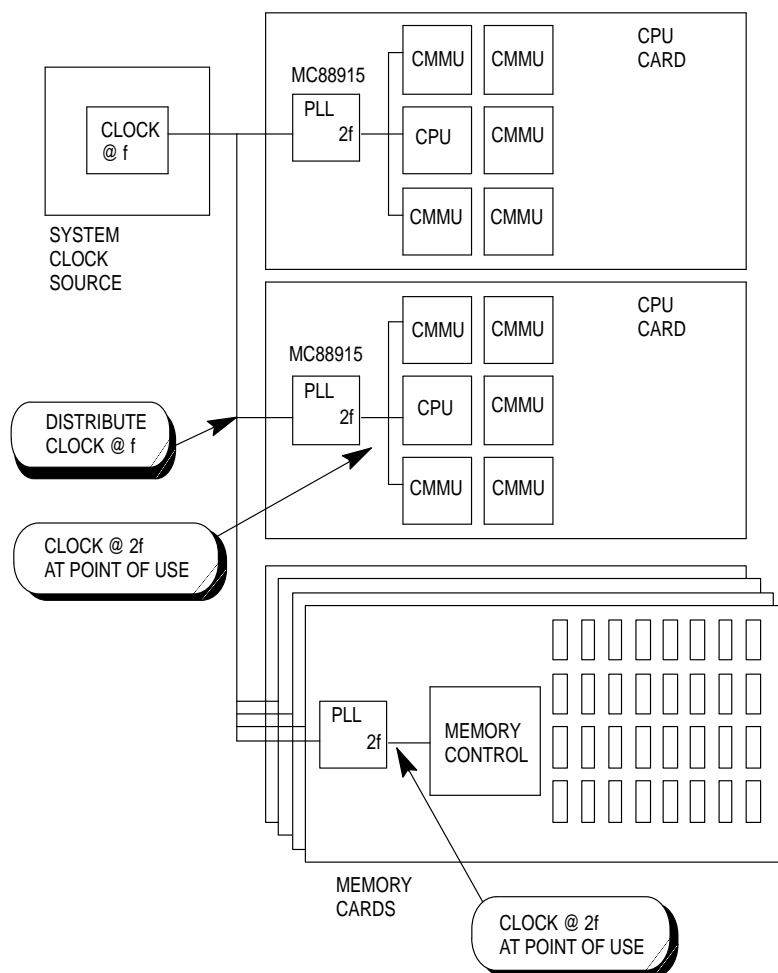


Figure 7. Representation of a Potential Multi-Processing Application Utilizing the MC88915 for Frequency Multiplication and Low Board-to-Board Skew

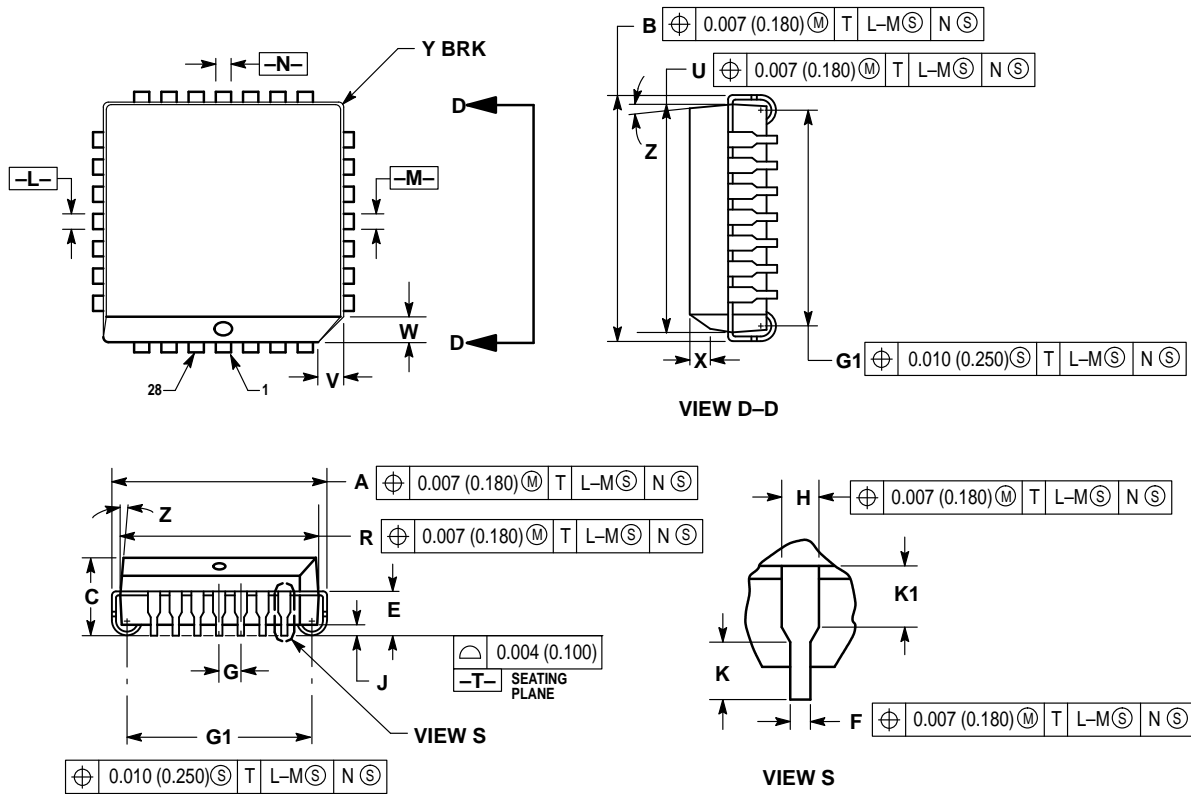
MC88915 System Level Testing Functionality

When the PLL_EN pin is low, the VCO is disabled and the 88915 is in low frequency “test mode”. In test mode (with FREQ_SEL high), the 2X_Q output is inverted from the selected SYNC input, and the “Q” outputs are divide-by-2 (negative edge triggered) of the SYNC input, and the Q/2 output is divide-by-4. With FREQ_SEL low the 2X_Q output is divide-by-2 of the SYNC, the “Q” outputs divide-by-4, and the Q/2 output divide-by-8. These relationships can be seen on the block diagram. A recommended test configuration would be to use SYNC0 as the test clock input, and tie PLL_EN and REF_SEL together and connect them to the test select logic. When these inputs are low, the 88915 is in test mode and the SYNC0 input is selected.

This functionality is needed since most board-level testers run at 1 MHz or below, and the 88915 cannot lock onto that low of an input frequency. In the test mode described above, any frequency test signal can be used.


OUTLINE DIMENSIONS

FN SUFFIX
 PLASTIC PACKAGE
 CASE 776-02
 ISSUE D



- NOTES:
- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
 - DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
 - DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
 - DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 - CONTROLLING DIMENSION: INCH.
 - THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
 - DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.485 | 0.495 | 12.32 | 12.57 |
| B | 0.485 | 0.495 | 12.32 | 12.57 |
| C | 0.165 | 0.180 | 4.20 | 4.57 |
| E | 0.090 | 0.110 | 2.29 | 2.79 |
| F | 0.013 | 0.019 | 0.33 | 0.48 |
| G | 0.050 BSC | | 1.27 BSC | |
| H | 0.026 | 0.032 | 0.66 | 0.81 |
| J | 0.020 | — | 0.51 | — |
| K | 0.025 | — | 0.64 | — |
| R | 0.450 | 0.456 | 11.43 | 11.58 |
| U | 0.450 | 0.456 | 11.43 | 11.58 |
| V | 0.042 | 0.048 | 1.07 | 1.21 |
| W | 0.042 | 0.048 | 1.07 | 1.21 |
| X | 0.042 | 0.056 | 1.07 | 1.42 |
| Y | — | 0.020 | — | 0.50 |
| Z | 2° | 10° | 2° | 10° |
| G1 | 0.410 | 0.430 | 10.42 | 10.92 |
| K1 | 0.040 | — | 1.02 | — |

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and  are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

How to reach us:

USA/EUROPE/Locations Not Listed: Motorola Literature Distribution;
P.O. Box 5405; Denver, Colorado 80217. 303-675-2140 or 1-800-441-2447

Mfax™: RMFAX0@email.sps.mot.com – TOUCHTONE 602-244-6609
INTERNET: <http://Design-NET.com>

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, 6F Seibu-Butsuryu-Center,
3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 81-3-3521-8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

