Not Recommended for New Designs

CMOS PLL Clock Driver

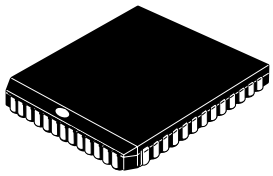
Programmable Frequency, Low Skew, High Fan-Out

MC88PL117

CMOS PLL CLOCK DRIVER

The MC88PL117 utilizes proven phase–locked loop clock driver technology to create a large fan–out, multiple frequency and phase, low skew clock driver. The 88PL117 provides the clock frequencies necessary to drive systems using the PowerPC™ 601 microprocessor and the Pentium™ microprocessor (see applications section for details). A total of 14 high current, matched impedance outputs are available in 8 programmable output frequency and phase configurations. Output frequencies are referenced to a system frequency, Q, and are available at 2X, 1X, and 1/2X the Q frequency. Four programmable input frequency multiplication ratios can be programmed to provide outputs at 1X, 2X, and 4X the system frequency Q. Details on the programmable configurations can be found in the applications section of this data sheet.

- Clock Driver for PowerPC 601 and Pentium Microprocessors
- 14 programmable outputs
- Maximum output–to–output skew of 500ps for a single frequency
- Maximum output–to–output skew of 500ps for multiple frequencies
- f_{MAX} of 2X_Q = 120MHz
- One output with programmable phase capability
- ±36mA DC current outputs drive 50Ω transmission lines
- A lock indicator output (LOCK) goes high when steady–state phase–lock is achieved
- OE/MR 3–state control
- Dedicated feedback output
- Two selectable clock inputs
- PLL enable pin for testability
- Dynamic Switch Between SYNC Inputs



FN SUFFIX
52–LEAD PLASTIC LEADLESS
CHIP CARRIER (PLCC)
CASE 778–02

One output (QFEED) is dedicated for feedback. It is located physically close to the FEEDBACK input pin to minimize the feedback line length. External delay (increased wire length) or logic can be inserted in the feedback path if necessary. Proper termination of the feedback line is necessary for any line length over one inch.

One output is provided with up to eight selectable 1/8 or 1/4 period (45° or 90°) delay increments. Three control pins, ∅2, ∅1 and ∅0, program the eight increments; the increment/phase shift positions are shown in Table 3. in the applications section.

All outputs can be 3–stated (high impedance) during board–level testing with the OE/MR pin; the QFEED and LOCK outputs will not be 3–stated, which allows the 88PL117 to remain in a phase–locked condition. Correct phase and frequency coherency will be guaranteed one to two cycles after bringing the OE/MR pin high. The PLL_EN pin disables the PLL and gates the SYNC input signal directly into the internal clock distribution network to provide low frequency testability. Two selectable SYNC inputs (SYNC0 and SYNC1) are provided for clock redundancy or ease of testability. The device is guaranteed to lock to the new SYNC input when the REF_SEL input is switched dynamically.

A phase–lock indicator output (LOCK) stays low when the part is out of lock (start–up, etc.) and goes high when steady–state phase–lock is achieved. The lock indicator circuitry works reliably for VCO frequencies down to 55MHz. For VCO frequencies less than 55MHz, no guarantees are offered for the lock indicator output.

The MC88PL117 VCO is capable of operating at frequencies higher than the output divider and feedback structures are able to follow. When the VCO is in the mode described above, it is referred to as “runaway” and the device will not lock. The condition usually occurs at power–up. To avoid runaway, it is recommended that the device be fully powered before a sync signal is applied.

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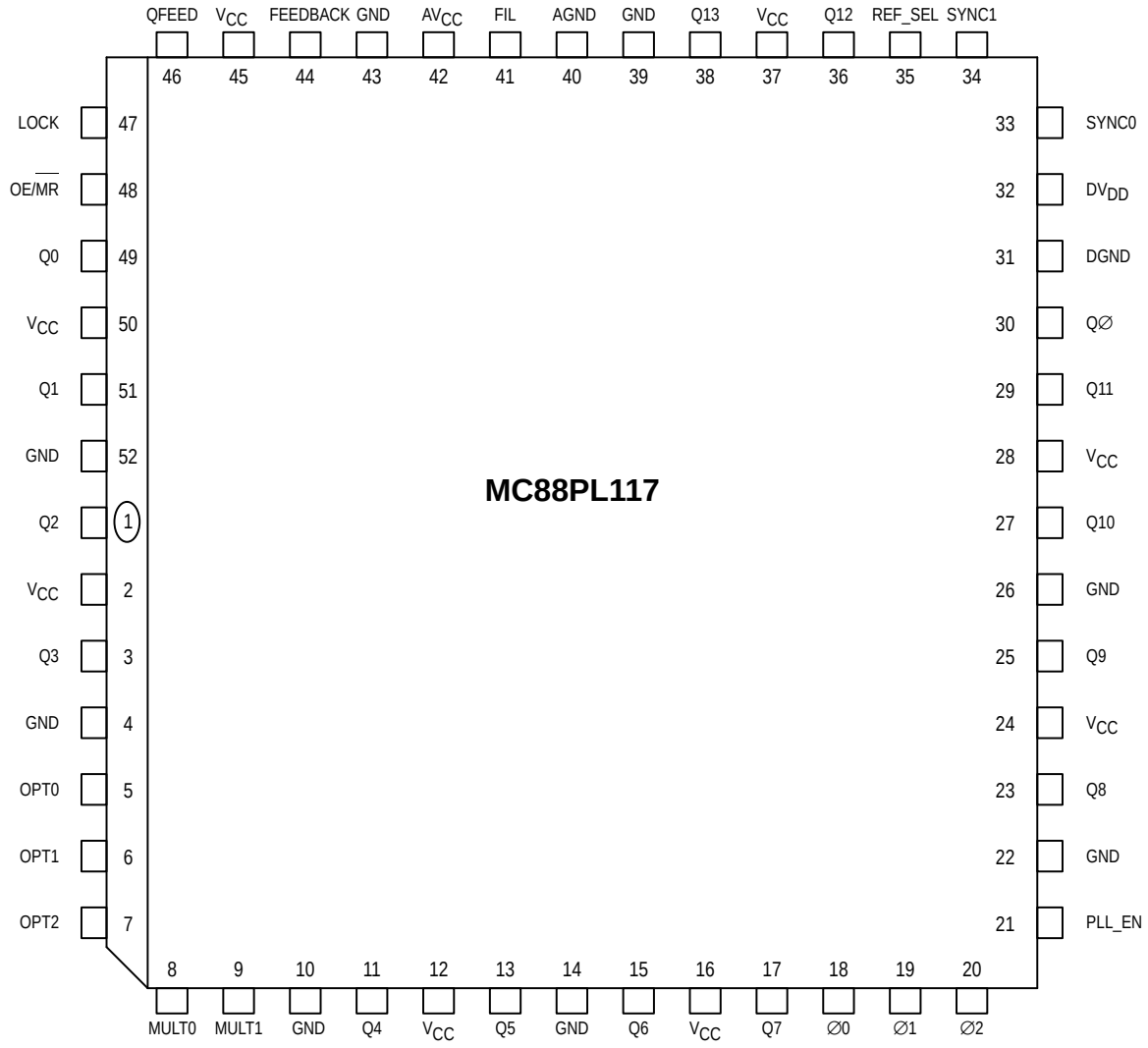
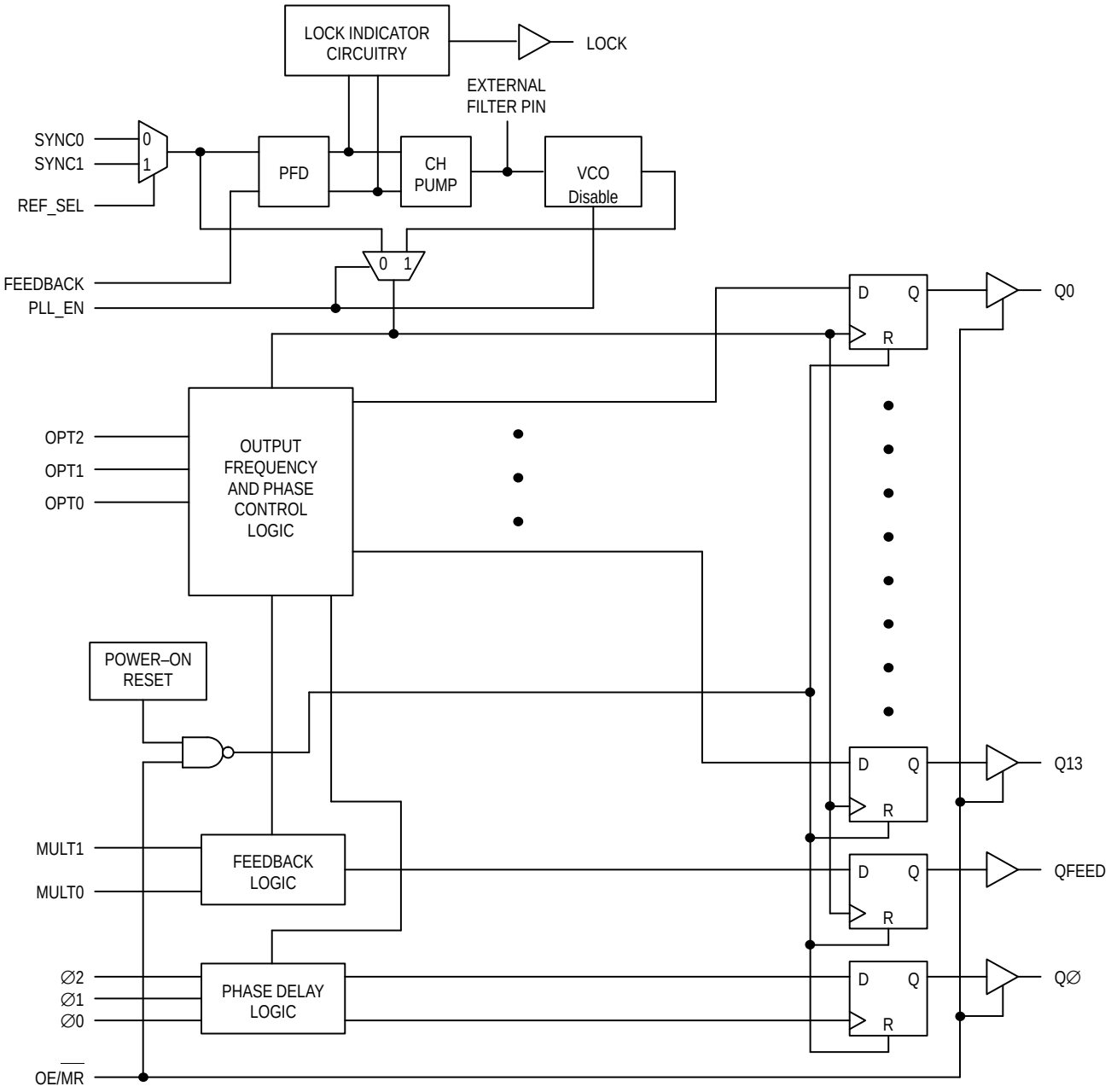


Pinout: 52–Lead PLCC (Top View)



MC88PL117 Block Diagram (Logical Representation)

Explanation of Programmable Frequency Configurations

The MC88PL117 has six different output frequency configurations. Figures 1 to 6 graphically depict these output configurations. There are also three feedback frequency options, which yields a total of 18 unique input–to–output frequency configurations. All configurations use ‘Q’ as the system frequency frame of reference. Therefore all output and feedback frequencies are referenced as a multiple of Q. Figures 1 to 6 also indicate the input levels of OPT0, OPT1, and OPT2 for each of the eight output configurations. The input levels of MULT0 and MULT1 are varied in these figures to represent the different feedback (multiplication) frequencies. The frequency of the phase shift output, Q∅, is also indicated in the figures. Tables 1. and 2. lists all 18 input/output frequency configurations. Table 3. gives the Q∅ phase shift increments.

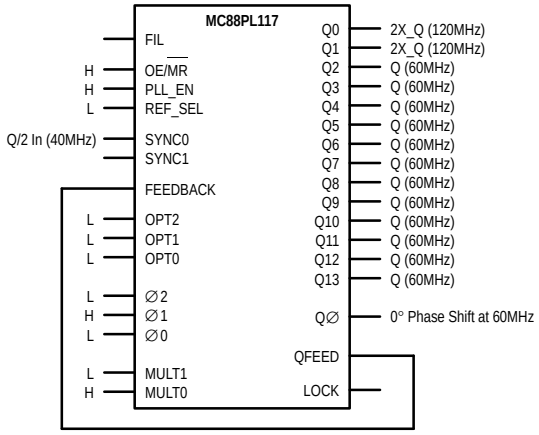


Figure 1. Output Frequency Configuration 1
(OPT0 = L, OPT1 = L, OPT2 = L
Q/2 Input Frequency, MULT0 = H, MULT1 = L)

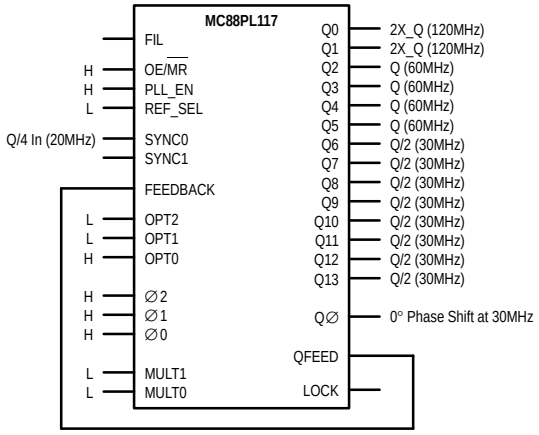


Figure 2. Output Frequency Configuration 2
(OPT0 = H, OPT1 = L, OPT2 = L
Q/4 Input Frequency, MULT0 = L, MULT1 = L)

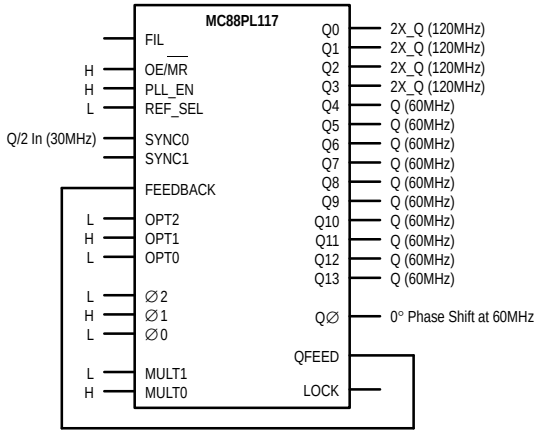


Figure 3. Output Frequency Configuration 3
(OPT0 = L, OPT1 = H, OPT2 = L
Q/2 Input Frequency, MULT0 = H, MULT1 = L)

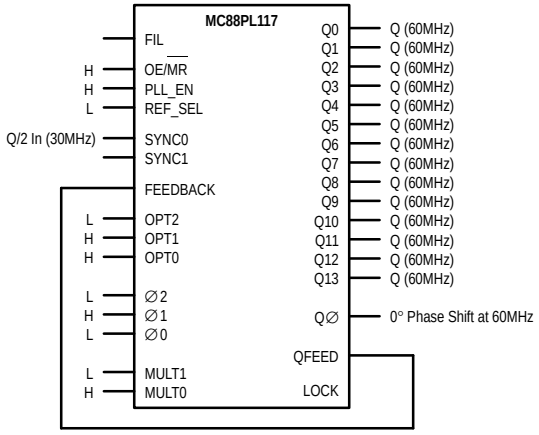


Figure 4. Output Frequency Configuration 4
(OPT0 = H, OPT1 = H, OPT2 = L
Q/2 Input Frequency, MULT0 = H, MULT1 = L)

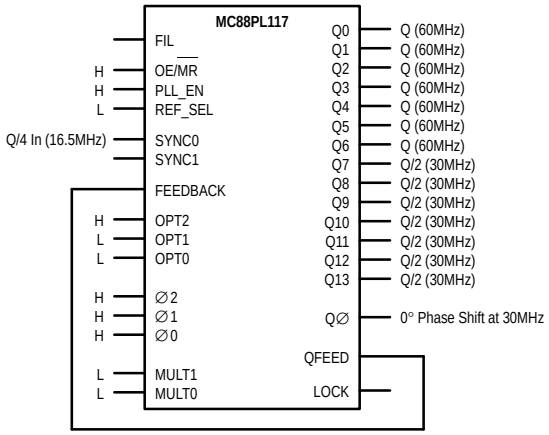


Figure 5. Output Frequency Configuration 5
(OPT0 = L, OPT1 = L, OPT2 = H
Q/4 Input Frequency, MULT0 = L, MULT1 = L)

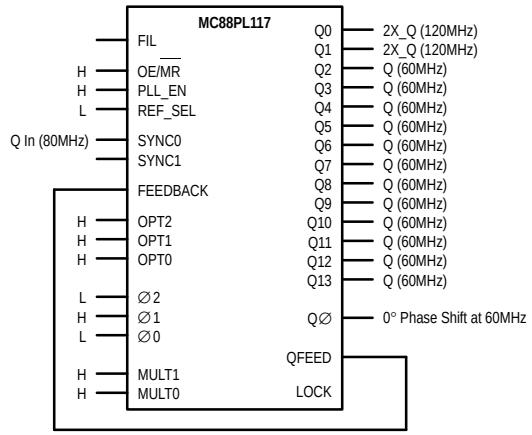


Figure 6. Output Frequency Configuration 6
(OPT0 = H, OPT1 = H, OPT2 = H
Q Input Frequency, MULT0 = H, MULT1 = H)

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND) T_A =0° C to + 70° C, V_{CC} = 5.0 V ± 5%

Symbol	Parameter	Test Conditions	V_{CC} V	Target Limit	Unit
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V	4.75 5.25	2.0 2.0	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V	4.75 5.25	0.8 0.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = –36 mA **1**	4.75 5.25	4.01 4.51	V
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OL} = 36 mA **1**	4.75 5.25	0.44 0.44	V
I_{in}	Maximum Input Leakage Current	V_I = V_{CC} or GND	5.25	±1.0	μA
I_{CCT}	Maximum I_{CC}/Input	V_I = V_{CC} – 2.1 V	5.25	2.0 **2**	mA
I_{OLD}	Minimum Dynamic Output Current **3**	V_{OLD} = 1.0V Max	5.25	88	mA
I_{OHD}		V_{OHD} = 3.85V Min	5.25	–88	mA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_I = V_{CC} or GND	5.25	1.0	mA
I_{OZ}	Maximum 3–State Leakage Current	V_I = V_{IH} or V_{IL};V_O = V_{CC} or GND	5.25	±50 **4**	μA

1. I_{OL} and I_{OH} are 12mA and –12mA respectively for the LOCK output.
2. The PLL_EN input pin is not guaranteed to meet this specification.
3. Maximum test duration is 2.0ms, one output loaded at a time.
4. Specification value for I_{OZ} is preliminary, will be finalized upon ‘MC’ status.

PRELIMINARY AC ELECTRICAL CHARACTERISTICS (T_A = 0 to 70°C, V_{CC} = 5.0V ±5%)

Symbol	Parameter	Target Specifications		Unit	Condition
		Min	Max		
t_{skewr}	Output–to–Output Skew (Same Frequency, Coincident Rising Edges)		500	ps	50Ω Load[2]
$t_{skewrall}$	Output–to–Output Skew (Any Frequency, Coincident Rising Edges, Q0–Q13, QFEED)		500	ps	50Ω Load[2]
t_{skewp}	Part–to–Part Skew[1]		1.0	ns	50Ω Load[2]
t_r/t_f	Output Rise/Fall Time (0.8 to 2.0V)	0.15	1.0	ns	50Ω Load[2]
t_{PULSE}	Output Pulse Width, All Outputs[2] (Measured at $V_{CC}/2$)	$0.5t_{CYCLE}$ – 0.5	$0.5t_{CYCLE}$ + 0.5	ns	50Ω Load[2]
t_{pd}	SYNC Input to FEEDBACK Delay f_{SYNC}=15MHz	–200	400	ps	Feedback=Q,Q/2
	f_{SYNC}=20MHz	–200	400		
	f_{SYNC}=25MHz	–100	500		
	f_{SYNC}=30MHz	0	600		
	f_{SYNC}=15MHz	–50	550		Feedback=Q/4
$Jitter_{CC}$	Cycle–to–Cycle Jitter (Clock Period Stability)		±250	ps	
f_{MAX}	Maximum Output Frequency for 2X_Q Outputs	8	120	MHz	50Ω Load[2]
f_{MAX}	Maximum Output Frequency for Q Outputs	4	60	MHz	50Ω Load[2]
f_{MAX}	Maximum Output Frequency for Q/2 Outputs	2	30	MHz	50Ω Load[2]
$t_{skew∅}$	Phase Accuracy of Q∅ versus Q or Q/2	Phase Offset – 750	Phase Offset + 250	ps	

1. This assumes that each device is running off of the same clock source with zero skew between clock source signals. A small amount of negative offset may be present between SYNC and FEEDBACK (t_{PD} Spec).
2. 50Ω load terminated to $V_{CC}/2$.

TABLE 1. PROGRAMMABLE OUTPUT CONFIGURATIONS (Q is system reference frequency)

Output Configuration Number	OPT2	OPT1	OPT0	No of 2X_Q Outputs	No of Q Outputs	No of Q/2 Outputs
1	L	L	L	2	12	0
2	L	L	H	2	4	8
3	L	H	L	4	10	0
4	L	H	H	0	14	0
5	H	L	L	0	7	7
6	H	H	H	2	12	0

TABLE 2. PROGRAMMABLE INPUT FREQUENCY MODES (Multiplication factors)

Input Frequency Mode	MULT1	MULT0	Input Frequency
1	L	L	Q/4
2	L	H	Q/2
3	H	H	Q

TABLE 3. Q∅ PROGRAMMABLE PHASE INCREMENTS FOR Q AND Q/2 OUTPUTS

∅2	∅1	∅0	Q∅ Phase to Q Outputs[1]	Q∅/2 Phase to Q Outputs[2]	∅2	∅1	∅0	Q∅ Phase to Q Outputs[1]	Q∅/2 Phase to Q Outputs[2]
L	L	L	180°	45°	H	L	L	180°	225°
L	L	H	90°	90°	H	L	H	90°	270°
L	H	L	0°	135°	H	H	L	0°	315°
L	H	H	270°	180°	H	H	H	270°	360°

1. Valid for output configurations 1, 3, 4, 6, 8
2. Valid for output configurations 2, 5, 7

Applications Information

Introduction

The 88PL117 provides the necessary clock frequencies for the PowerPC 601 and Pentium Microprocessors. With output frequency capabilities up to 120MHz and the ability to also generate half and quarter frequency clocks the 88PL117 simplifies the system implementation of a PowerPC 601 or Pentium Microprocessor. This section will overview the clock requirements of the PowerPC 601 and Pentium Microprocessors and apply those to the specification limits of the 88PL117 to demonstrate compatibility. Although not exhaustive the intent is to provide a basic set of guidelines on system implementation. For more cost sensitive applications which require fewer clocks the designer should refer to the MC88915TFN133 data sheet for an alternative clock driver suitable for PowerPC 601 or Pentium Microprocessor based designs.

Figures 7 and 8 illustrate two common output config–urations of the 88PL117 which will facilitate POWERPC 601 (MPC601) system designs. Figure 7 would prove beneficial for high frequency processor designs where the bus clock would likely run at one fourth the 2X_PCLK input. In this configuration a 2X_Q output of the 88PL117 can drive the 2X_PCLK of the PowerPC 601 processor while a Q and Q/2 output can drive the PCLK_EN and BCLK_EN inputs respectively. For designs where the system bus will run at half the frequency of the 2X_PCLK (same frequency as the internal processor clock) a larger number of Q outputs would be required. Figure 8 could be used in this situation with a

2X_Q output driving the 2X_PCLK input and a Q output driving the PCLK_EN. In this implementation the BCLK_EN input of the MPC601 is simply tied LOW.

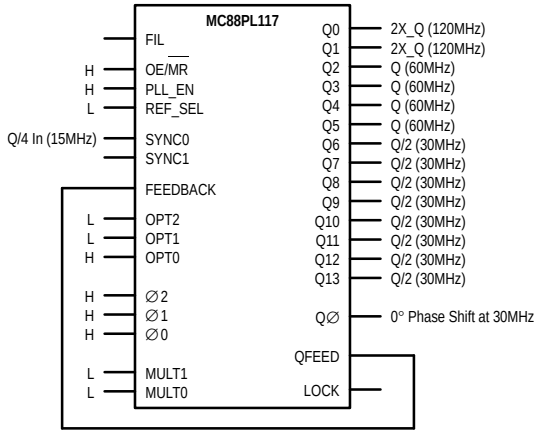


Figure 7. 88PL117 Output Configuration 1 for Driving the MPC601 Microprocessor

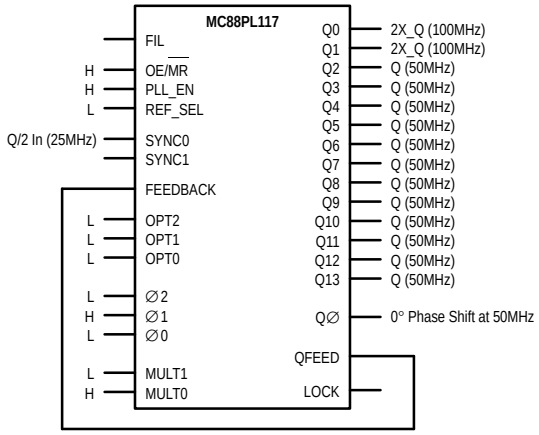


Figure 8. 88PL117 Output Configuration 2 for Driving the MPC601 Microprocessor

Driving the PowerPC 601 Microprocessor

Figures 9 and 10 illustrate the required waveforms for driving the MPC601 processor in both bus clock frequency modes. Figure 10 illustrates the relationship between the 2X_Q, Q and Q/2 outputs of the 88PL117. For the case of the BCLK_EN input being held LOW, the setup and hold specifications for PCLK_EN are automatically satisfied by the internal design of the 88PL117. For the first case pictured in Figure 9, there may be a potential problem: the hold time spec for BCLK_EN rising to 2X_PCLK is 0ns. Because there can be up to ±250ps skew between the 2X_Q and Q/2 outputs of the 88PL117, this hold spec may be violated. This situation can be remedied in one of two ways: first extra PCB etch can be added to the Q/2 output to delay it relative to the 2X_Q output; or secondly, the Q∅ output can be used to drive the $\overline{\text{BCLK\_EN}}$ input. The Q∅ output can be phase delayed relative to the 2X_Q output to ensure the hold time requirement of the MPC601 processor will be met.

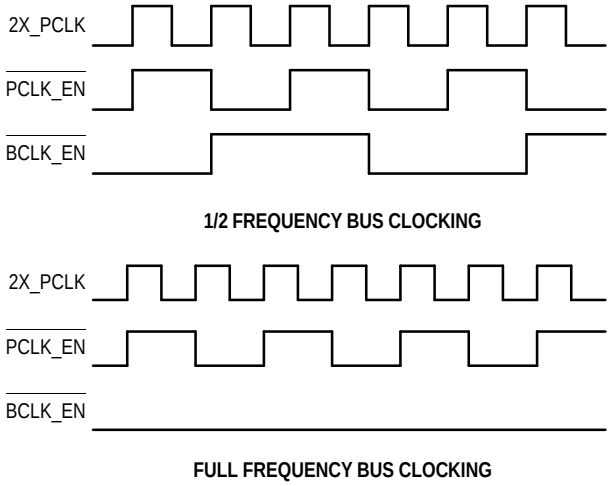


Figure 9. MPC601 Processor Clocking Waveforms

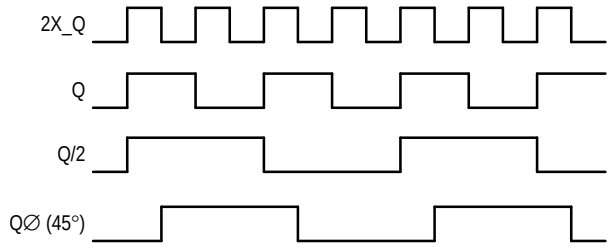


Figure 10. 88PL117 Output Waveforms

The 88PL117 features CMOS level outputs to minimize edge transition time and optimize transmission line driving capability. The MPC601 processor inputs are TTL level compatible inputs and therefore specification limits are calculated from TTL level thresholds. The specification limits of concern are the input duty cycle and input pulse width requirements outlined in the MPC601 specification for the 2X_PCLK input. Figure 11 demonstrates the termination technique required on the 2X_Q output of the 88PL117 to ensure compatibility with the 2X_PCLK input of the MPC601 processor. At 100 or 120MHz, the 2X_Q output threshold must be shifted down to the 1.4V threshold to meet the input pulse width specification limits. The termination scheme in Figure 11 creates a voltage division which essentially translates the CMOS threshold down to a TTL threshold, while at the same time effectively terminating the transmission line. The 88PL117 exhibits a very tight duty cycle specification at CMOS thresholds. Therefore, once translated via the termination scheme of Figure 11, the MPC601 processor input specifications are easily met.

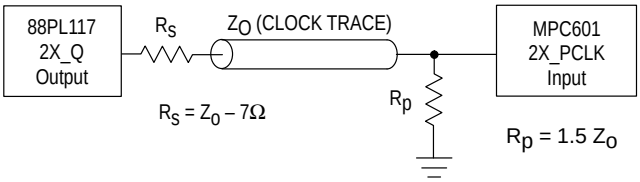


Figure 11. MPC601 2X_PCLK Input Termination Scheme

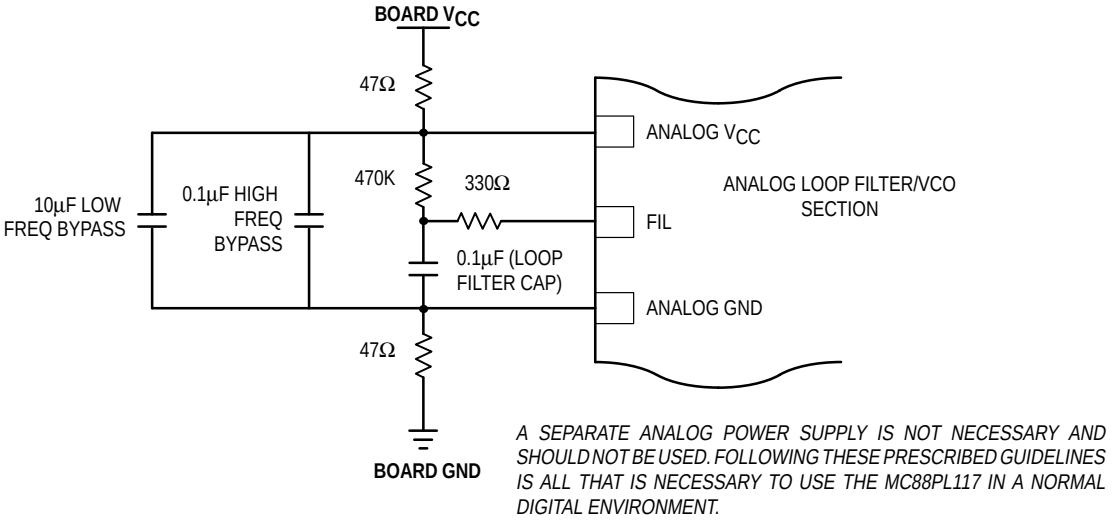


Figure 12. Recommended Loop Filter and Analog Isolation Scheme

Notes Concerning Loop Filter and Board Layout Issues

1 Figure 12 shows a loop filter and analog isolation scheme which will be effective in most applications. The following guidelines should be followed to ensure stable and jitter–free operation:

1a All loop filter and analog isolation components should be tied as close to the package as possible. Stray current passing through the parasitics of long traces can cause undesirable voltage transients at the FIL pin.

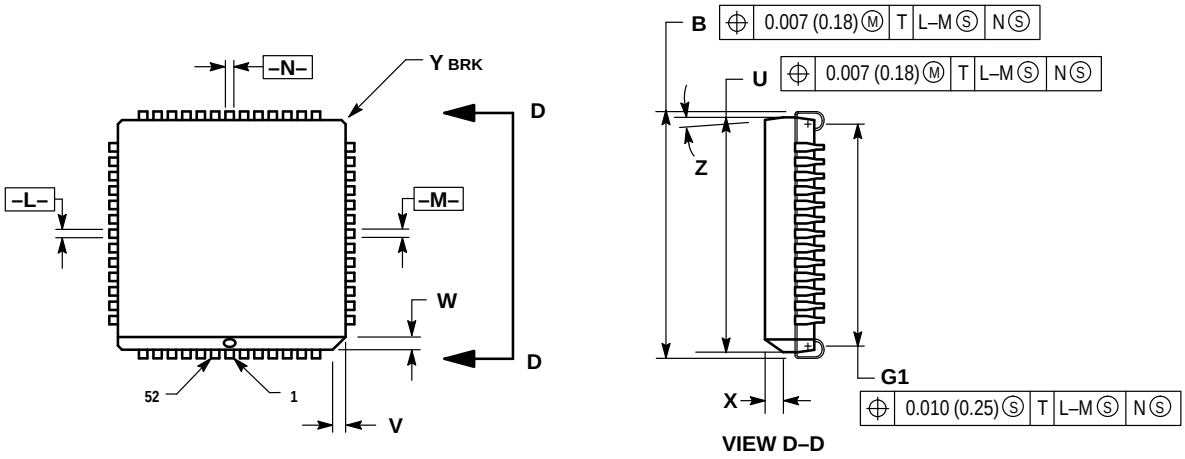
1b The 47Ω resistors, the 10μF low frequency bypass capacitor, and the 0.1μF high frequency bypass capacitor form a wide bandwidth filter that will minimize the PLL's sensitivity to voltage transients from the system digital V_{CC} supply and ground planes. This filter will typically ensure that a 100mV step deviation on the digital V_{CC} supply will cause no more than a 100pS phase deviation on the device outputs. A 250mV step deviation on V_{CC} using the recommended filter values should cause no more than a 250pS phase deviation; if a 25μF bypass capacitor is used (instead of 10μF) a 250mV V_{CC} step should cause no more than a 100pS phase deviation. If good bypass techniques are used on a board design near components which may cause digital V_{CC} and ground noise, the above described V_{CC} step deviations should not occur at the digital V_{CC} supply. The purpose of the bypass filtering scheme shown in Figure 12 is to give the chip additional protection from the power supply and ground plane transients that can occur in a a high frequency, high speed digital system.

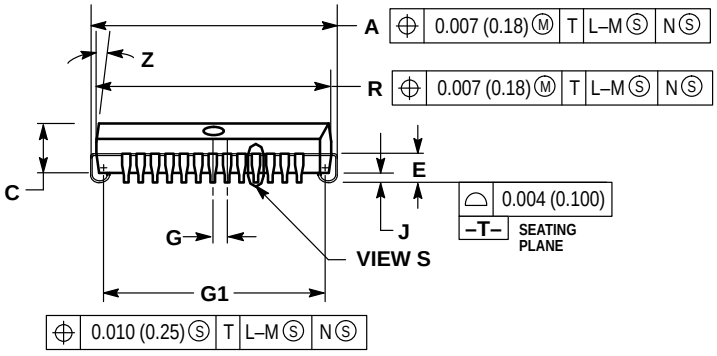
1c There are no special requirements set forth for the loop filter resistors (470K and 330Ω). The loop filter capacitor (0.1μF) can be a ceramic chip capacitor, the same as a standard bypass capacitor.

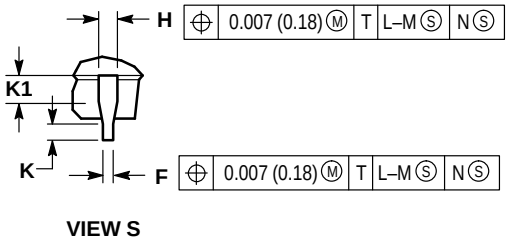
2 In addition to the bypass capacitors used in the analog filter of Figure 12, there should be a 0.1μF bypass capacitor between each of the other (digital) nine V_{CC} pins and the board ground plane. This will reduce output switching noise caused by the high current outputs, in addition to reducing potential for noise in the 'analog' section of the chip. These bypass capacitors should also be tied as close to the package as possible.

OUTLINE DIMENSIONS

FN SUFFIX
PLASTIC PACKAGE
CASE 778-02
ISSUE C







NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.785	0.795	19.94	20.19
B	0.785	0.795	19.94	20.19
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.750	0.756	19.05	19.20
U	0.750	0.756	19.05	19.20
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2 °	10 °	2 °	10 °
G1	0.710	0.730	18.04	18.54
K1	0.040	—	1.02	—

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