MCM321024

Advance Information

1M x 32 Bit
Fast Static RAM Module

The MCM321024 is an 32M bit static random access memory module orga-nized as 1,048,576 words of 32 bits. The module is a 72–lead single in–line memory module (SIMM) consisting of eight MCM6249 fast static RAMs pack-aged in 32–lead SOJ packages and mounted on a printed circuit board along with sixteen decoupling capacitors.

The MCM6249 is a high performance CMOS fast static RAM organized as 1,048,576 words of 4 bits. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and pro-vides for greater reliability.

The MCM321024 is equipped with output enable ($\overline{G}$) and four separate byte enable ($\overline{E1}$ – $\overline{E4}$) inputs, allowing for greater system flexibility. The G input, when high, will force the outputs to high impedance. Ex high will do the same for byte x.
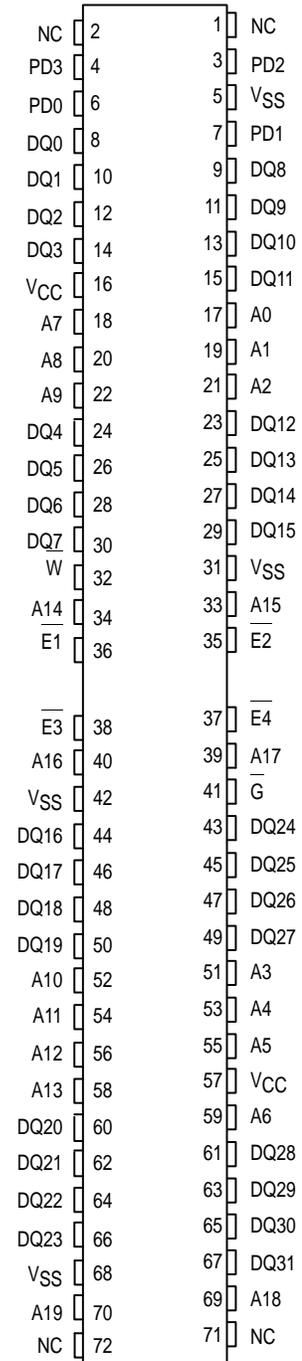
PD0 – PD3 are reserved for density identification. PD0 and PD2 are connected to ground. These pins can be used to identify the density of the memory module.

- Single 5 V ± 10% Power Supply
- Fast Access Time: 20/25 ns
- Three–State Outputs
- Fully TTL Compatible
- JEDEC Standard Pinout
- Power Requirement: 1520/1400 mA Maximum, Active AC
- High Board Density SIMM Package
- Byte Operation: Four Separate Chip Enables, One for Each Byte (Eight Bits)
- High Quality Six–Layer FR4 PWB with Separate Internal Power and Ground Planes
- Incorporates Motorola's State–of–the–Art Fast Static RAMs

**PIN ASSIGNMENT
TOP VIEW
72 LEAD SIMM — CASE TBD**

Pin	Name		Pin	Name
2	NC		1	NC
4	PD3		3	PD2
6	PD0		5	V_{SS}
8	DQ0		7	PD1
10	DQ1		9	DQ8
12	DQ2		11	DQ9
14	DQ3		13	DQ10
16	V_{CC}		15	DQ11
18	A7		17	A0
20	A8		19	A1
22	A9		21	A2
24	DQ4		23	DQ12
26	DQ5		25	DQ13
28	DQ6		27	DQ14
30	DQ7		29	DQ15
32	W		31	V_{SS}
34	A14		33	A15
36	$\overline{E1}$		35	$\overline{E2}$
38	$\overline{E3}$		37	$\overline{E4}$
40	A16		39	A17
42	V_{SS}		41	$\overline{G}$
44	DQ16		43	DQ24
46	DQ17		45	DQ25
48	DQ18		47	DQ26
50	DQ19		49	DQ27
52	A10		51	A3
54	A11		53	A4
56	A12		55	A5
58	A13		57	V_{CC}
60	DQ20		59	A6
62	DQ21		61	DQ28
64	DQ22		63	DQ29
66	DQ23		65	DQ30
68	V_{SS}		67	DQ31
70	A19		69	A18
72	NC		71	NC

PIN NAMES

A0 – A19	Address Inputs
W	Write Enable
G	Output Enable
E1 – E4	Byte Enables
DQ0 – DQ31	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
PD0 – PD3	Package Density
NC	No Connect

For proper operation of the device, V_{SS} must be connected to ground.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MOTOROLA

FUNCTIONAL BLOCK DIAGRAM
1M x 32 MEMORY MODULE

MOTOROLA FAST SRAM
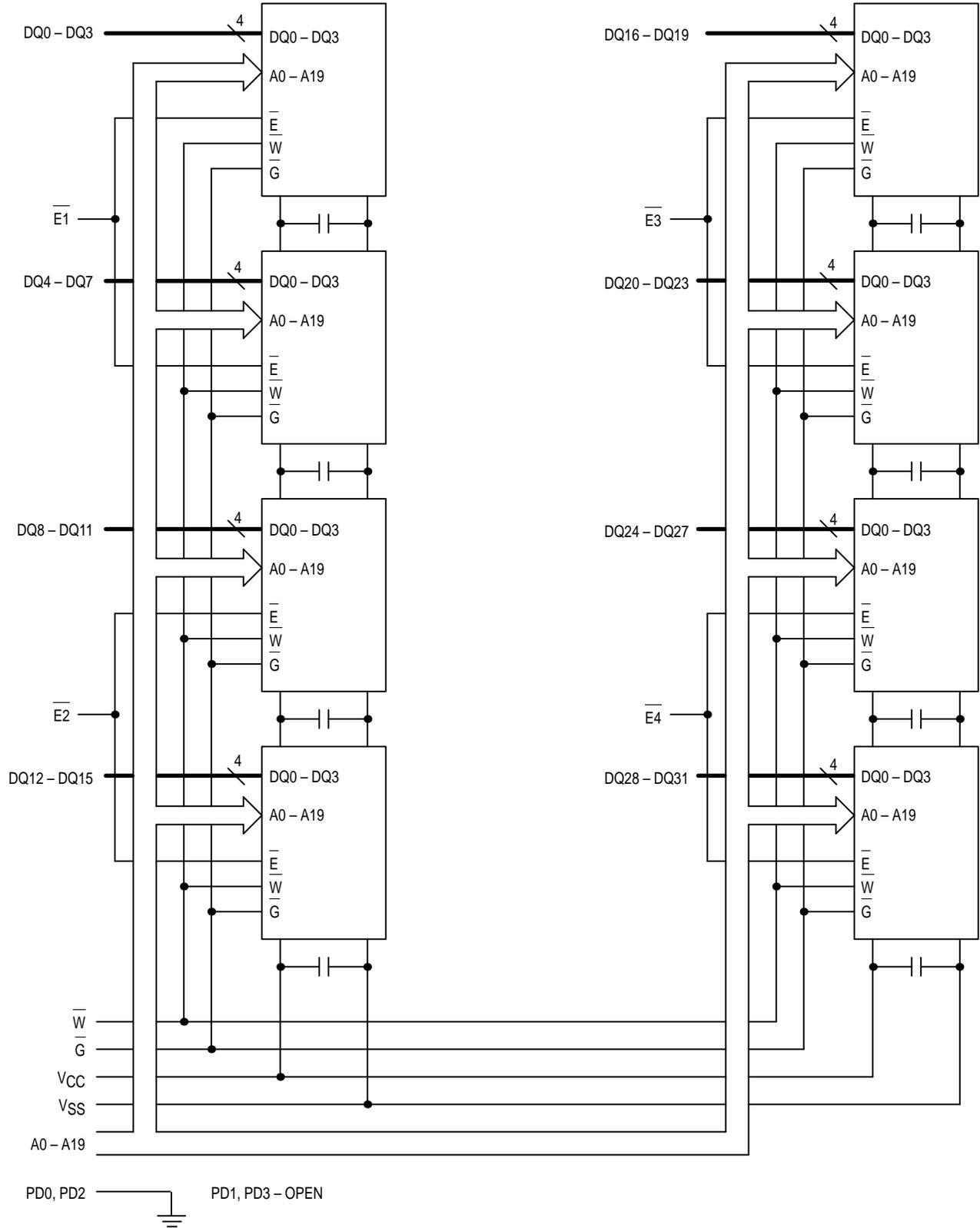
TRUTH TABLE

Ex	G	W	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1} or I_{SB2}	High–Z	—
L	H	H	Read	I_{CCA}	High–Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	D_{in}	Write Cycle

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	8.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperatrue	T_{stg}	– 25 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

The devices on this module contain circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedance circuits.

These CMOS memory circuits have been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The module is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS
(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3*	V
Input Low Voltage	V_{IL}	– 0.5**	—	0.8	V

 * V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns)
** V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	—	± 8	µA
Output Leakage Current (G, Ex = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	—	± 8	µA
AC Active Supply Current (G, Ex = V_{IL}, I_{out} = 0 mA, MCM321024–20: t_{AVAV} = 20 ns Cycle time ≥ t_{AVAV} min) MCM321024–25: t_{AVAV} = 25 ns	I_{CCA}	— —	1440 1320	1520 1400	mA
AC Standby Current (Ex = V_{IH}, Cycle time ≥ t_{AVAV} min)	I_{SB1}	—	400	480	mA
CMOS Standby Current (Ex ≥ V_{CC} – 0.2 V, All Inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V)	I_{SB2}	—	80	120	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	—	V

NOTE: Good decoupling of the local power supply should always be used.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	(All pins except DQ0 – DQ31, W, G, and E1 – E4) E1 – E4 W, G	C_{in}	32 10 40	48 14 64	pF
Input/Output Capacitance	(DQ0 – DQ31)	C_{out}	8	9	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS
(V_{CC} = 5.0 V $\pm$ 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . 1.5 V
Output Timing Reference Level . . . . 1.5 V
Input Pulse Levels . . . . 0 to 3.0 V

Output Load . . . . See Figure 1a Unless Otherwise Noted
Input Rise/Fall Time . . . . 3 ns

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM321024–20		MCM321024–25		Unit	Notes
		Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	20	—	25	—	ns	3
Address Access Time	t_{AVQV}	—	20	—	25	ns	
Enable Access Time	t_{ELQV}	—	20	—	25	ns	
Output Enable Access Time	t_{GLQV}	—	7	—	9	ns	
Output Hold from Address Change	t_{AXQX}	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	5	—	5	—	ns	4,5,6
Output Enable to Output Active	t_{GLQX}	0	—	0	—	ns	4,5,6
Enable High to Output High–Z	t_{EHQZ}	0	9	0	10	ns	4,5,6
Output Enable High to Output High–Z	t_{GHQZ}	0	9	0	10	ns	4,5,6
Power Up Time	t_{ELICCH}	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	—	20	—	25	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. E1 – E4 are represented by $\overline{E}$ in these timing specifications, any combination of Exs may be asserted.
3. All read cycle timing is referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured $\pm$ 500 mV from steady–state voltage with load of Figure 1b.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}). See Read Cycle 1.
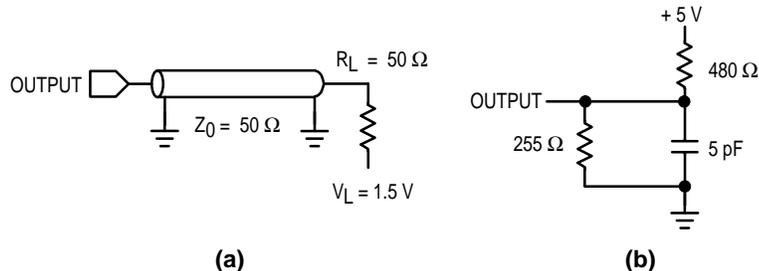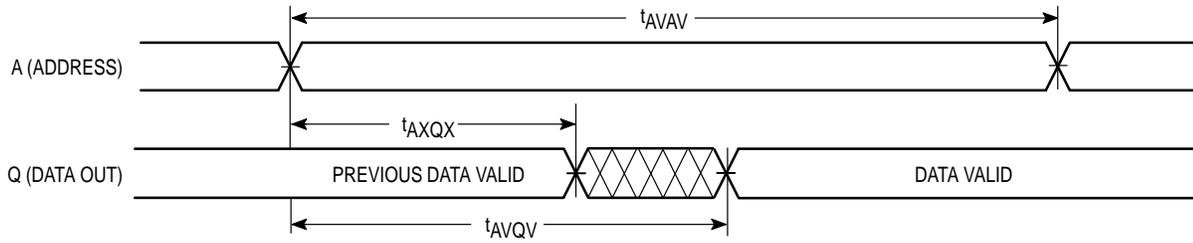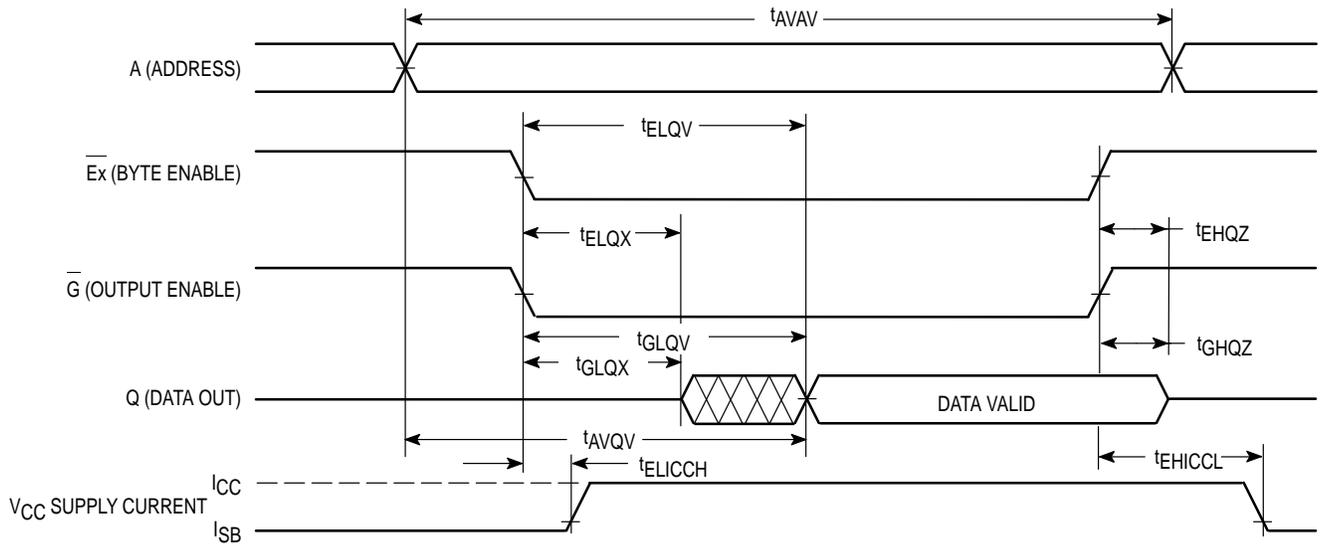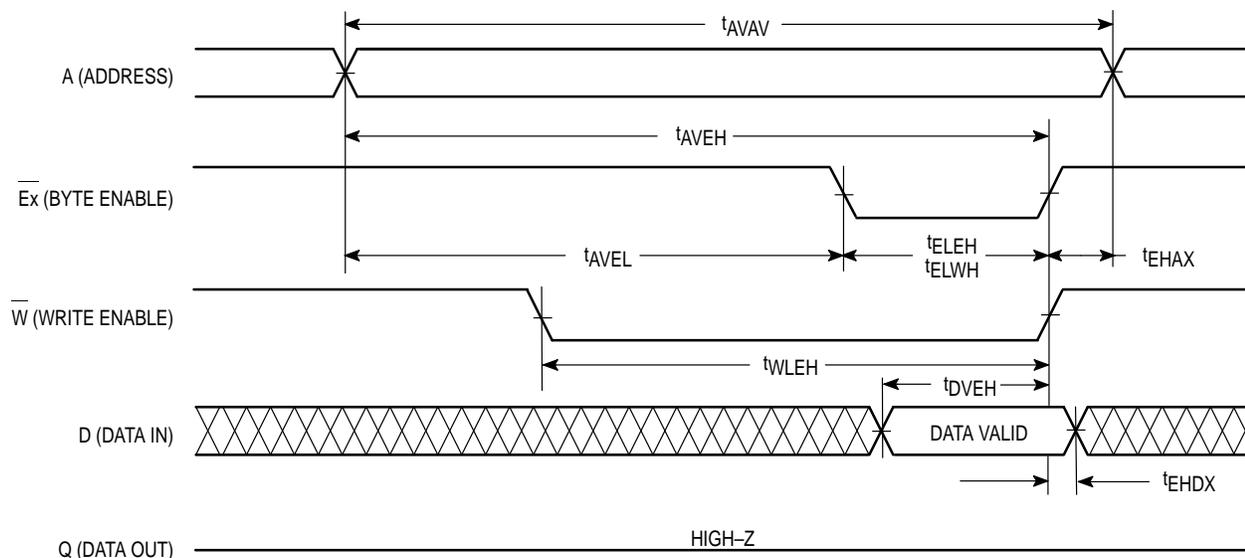
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

(a)   **(b)**

Figure 1. Test Loads

READ CYCLE 1 (See Note 7 Above)

A (ADDRESS)

t_{AVAV}

Q (DATA OUT)

t_{AXQX}

PREVIOUS DATA VALID   DATA VALID

t_{AVQV}

READ CYCLE 2 (See Note)

A (ADDRESS)

t_{AVAV}

$\overline{Ex}$ (BYTE ENABLE)

t_{ELQV}

t_{EHQZ}

t_{ELQX}

$\overline{G}$ (OUTPUT ENABLE)

t_{GLQV}

t_{GHQZ}

t_{GLQX}

Q (DATA OUT)

DATA VALID

t_{AVQV}

t_{ELICCH}

t_{EHICCL}

I_{CC}

V_{CC} SUPPLY CURRENT

I_{SB}

NOTE: Addresses valid prior to or coincident with $\overline{E}$ going low.

MOTOROLA FAST SRAM

MCM321024

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM321024–20		MCM321024–25		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	20	—	25	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	15	—	17	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	15	—	17	—	ns	
Data Valid to End of Write	t_{DVWH}	10	—	10	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	9	0	10	ns	4,5,6
Write High to Output Active	t_{WHQX}	5	—	5	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. E1 – E4 are represented by $\overline{E}$ in these timing specifications, any combination of $\overline{E}$xs may be asserted. $\overline{G}$ is a don't care when $\overline{W}$ is low.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1b.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1
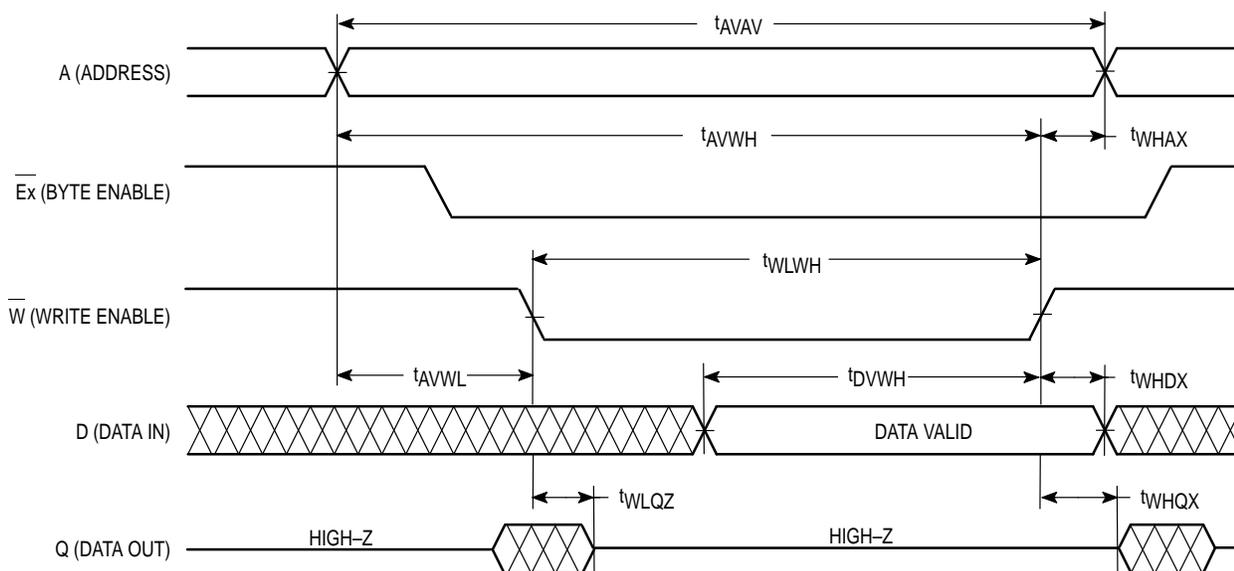
WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM321024–20 Min	MCM321024–20 Max	MCM321024–25 Min	MCM321024–25 Max	Unit	Notes
Write Cycle Time	t_{AVAV}	20	—	25	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	15	—	17	—	ns	
Enable to End of Write	t_{ELEH}	15	—	17	—	ns	4,5
Enable to End of Write	t_{ELWH}	15	—	17	—	ns	
Write Pulse Width	t_{WLEH}	15	—	17	—	ns	
Data Valid to End of Write	t_{DVEH}	10	—	10	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. E1 – E4 are represented by $\overline{E}$ in these timing specifications, any combination of $\overline{Ex}$s may be asserted. $\overline{G}$ is a don't care when $\overline{W}$ is low.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2

ORDERING INFORMATION
(Order by Full Part Number)

MCM 321024 XX XX

Motorola Memory Prefix

Part Number

Speed (20 = 20 ns, 25 = 25 ns)

Package (SG = Gold Pad SIMM)
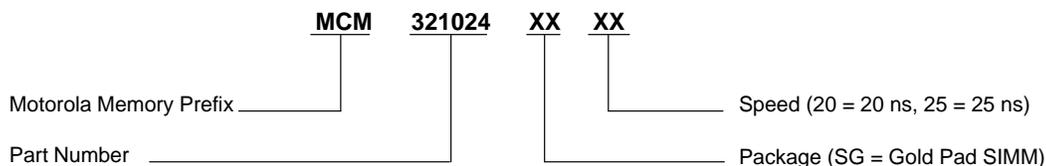
Full Part Numbers — MCM321024SG20   MCM321024SG25

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