MCM44256B Series

4MB R4000 Secondary Cache Fast Static RAM Module Set

Four MCM44256B modules comprise a full 4 MB of secondary cache for the R4000 processor. Each module contains nine MCM6729DWJ fast static RAMs for a cache data size of 256K x 36. The tag portion, dependent on word line size, contains either two MCM6729DWJ or one MCM6726DWJ fast static RAMs. All input signals, except A0 and WE are buffered using 74FBT2827 drivers with series 25 Ω resistors.

The MCM6729DWJ and MCM6726DWJ are fabricated using high–performance silicon–gate BiCMOS technology. Static design eliminates the need for internal clocks or timing strobes.

All 4MB R4000 supported secondary cache options are available.

- Single 5 V ± 10% Power Supply
- All Inputs and Outputs are TTL Compatible
- Fast Module Access Time: 12/15/17 ns
- Zero Wait–State Operation
- Unified or Split Secondary Cache is Supported
- Word Line Sizes of 4, 8, 16, and 32 are Available (See Ordering Information for Details)
- Decoupling Capacitors are Used for Each Fast Static RAM and Buffer, Along with Bulk Capacitance for Maximum Noise Immunity
- High Quality Multi–Layer FR4 PWB with Separate Power and Ground Planes

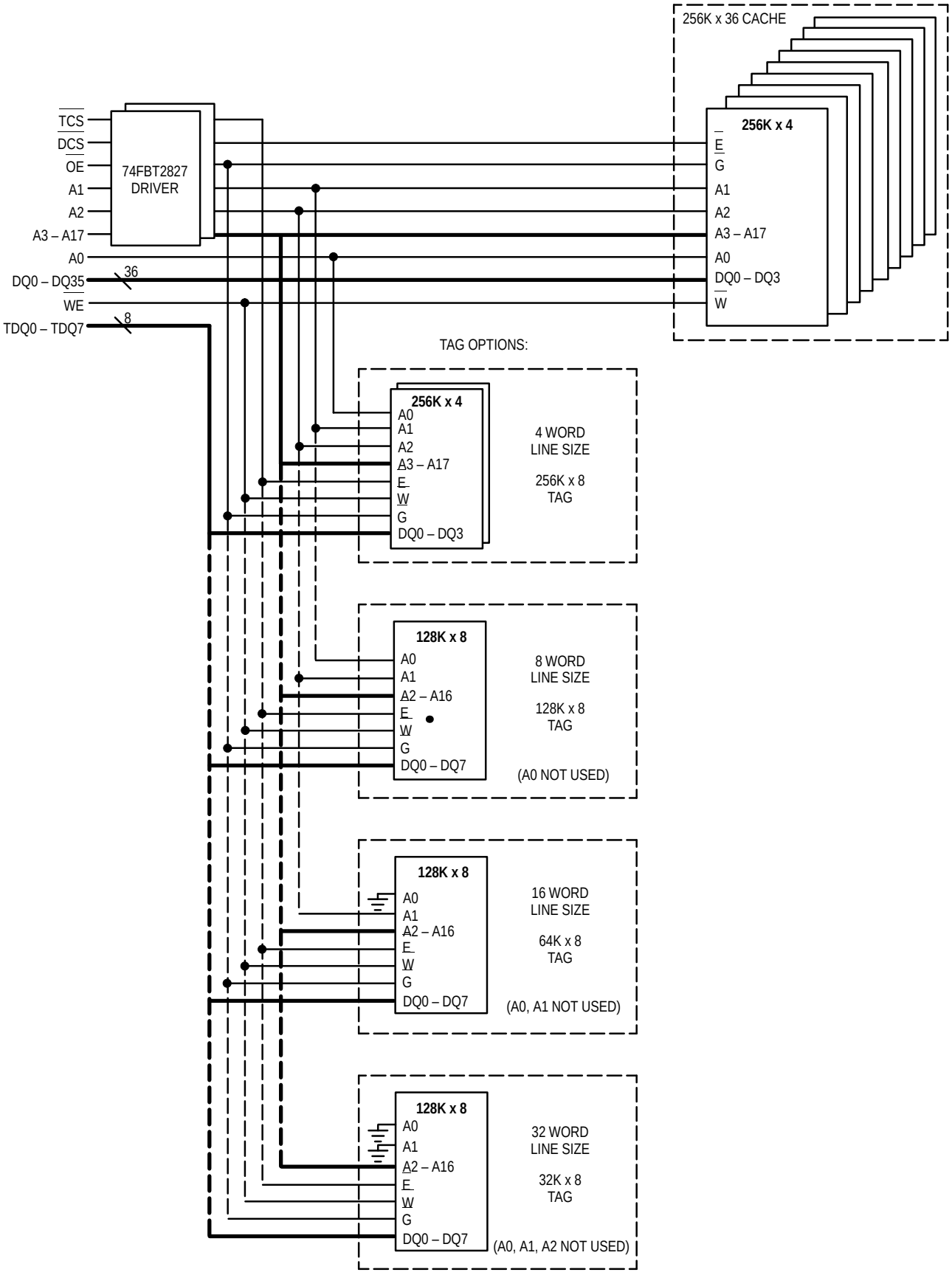
PIN NAMES	
$\overline{A0}$ – A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{DCS}$	Data Enable
$\overline{TCS}$	Tag Enable
$\overline{OE}$	Output Enable
DQ0 – DQ35	Data Input / Output
TDQ0 – TDQ7	TAG Data Input / Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

For proper operation of the device, V_{SS} must be connected to ground.

PIN ASSIGNMENT
80 LEAD SIMM — TOP VIEW

V_{CC}	2	1	V_{SS}
DQ1	4	3	DQ0
DQ3	6	5	DQ2
DQ5	8	7	DQ4
V_{SS}	10	9	DQ6
DQ8	12	11	DQ7
DQ10	14	13	DQ9
DQ12	16	15	DQ11
DQ14	18	17	DQ13
DQ15	20	19	V_{SS}
DQ17	22	21	DQ16
DQ19	24	23	DQ18
DQ21	26	25	DQ20
V_{SS}	28	27	DQ22
DQ23	30	29	V_{CC}
DQ25	32	31	DQ24
DQ27	34	33	DQ26
DQ29	36	35	DQ28
DQ30	38	37	V_{SS}
DQ32	40	39	DQ31
DQ34	42	41	DQ33
V_{SS}	44	43	DQ35
A0	46	45	$\overline{WE}$
A2	48	47	A1
A4	50	49	A3
A6	52	51	A5
V_{CC}	54	53	V_{SS}
$\overline{OE}$	56	55	$\overline{DCS}$
A8	58	57	A7
A10	60	59	A9
V_{SS}	62	61	A11
A13	64	63	A12
A15	66	65	A14
A17	68	67	A16
TDQ0	70	69	$\overline{TCS}$
TDQ1	72	71	V_{SS}
TDQ3	74	73	TDQ2
TDQ5	76	75	TDQ4
TDQ7	78	77	TDQ6
V_{SS}	80	79	V_{CC}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	10	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Storage Temperature	T_{stg}	– 25 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This devices on this module contain circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

These BiCMOS memory circuits have been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The module is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage (DQ0 – 35, TDQ0 – 7, $\overline{WE}$, A0) (A1 – A17, OE, DCS, TCS)	V_{IH}	 2.2 2.0	 — —	 V_{CC} + 0.3 V* V_{CC} + 0.3 V*	V
Input Low Voltage	V_{IL}	– 0.5**	—	0.8	V

*V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns).
**V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns).

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	—	± 10	µA
Output Leakage Current (G, xCS = V_{IH}, V_{out} = 0 to V_{CC})	Ilkg(O)	—	—	± 10	µA
AC Supply Current (G, xCS = V_{IL}, I_{out} = 0 mA)	I_{CCA}	—	—	1750	mA
Output Low Voltage (I_{OL} = + 8 mA)	V_{OL}	—	—	0.4	V
OUtput High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	—	V

NOTE: Good decoupling of the local power supply should always be used.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance ($\overline{WE}$, $\overline{A0}$) (A1 – A17, OE, DCS, TCS)	 C_{in} C_{in}	 — —	 110 10	 pF pF
Input/Output Capacitance	C_{out}	—	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 1 V/ns (20% to 80%)

Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . See Figure 1

READ CYCLE (See Notes 1 and 2)

Parameter	Symbol	–12		–15		–17		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Address Access Time	t_{AVQV}	—	12	—	15	—	17	ns	
A0 Access Time	t_{A0AQV}	—	10	—	12	—	14	ns	
Data/Tag Enable Access Time	t_{ELQV}	—	12	—	15	—	17	ns	
Output Enable Access Time	t_{GLQV}	—	9	—	10	—	11	ns	
Output Hold from Address Change	t_{AXQX}	4	—	4	—	4	—	ns	
Output Hold from A0 Change	t_{A0XQX}	4	—	4	—	4	—	ns	
Data/Tag Enable Low to Output Active	t_{ELQX}	2	—	2	—	2	—	ns	3, 4
Data/Tag Enable High to Output High–Z	t_{EHQZ}	1	9	1	10	1	11	ns	3, 4
Output Enable Low to Output Active	t_{GLQX}	1	—	1	—	1	—	ns	3, 4
Output Enable High to Output High–Z	t_{GHQZ}	1	9	1	10	1	11	ns	3, 4

NOTES:
1. WE is high for read cycle.
2. Enable timings are the same for both $\overline{DCS}$ and $\overline{TCS}$.
3. Transition is measured 200 mV from steady–state voltage.
4. This parameter is sampled and not 100% tested.

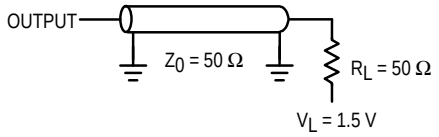
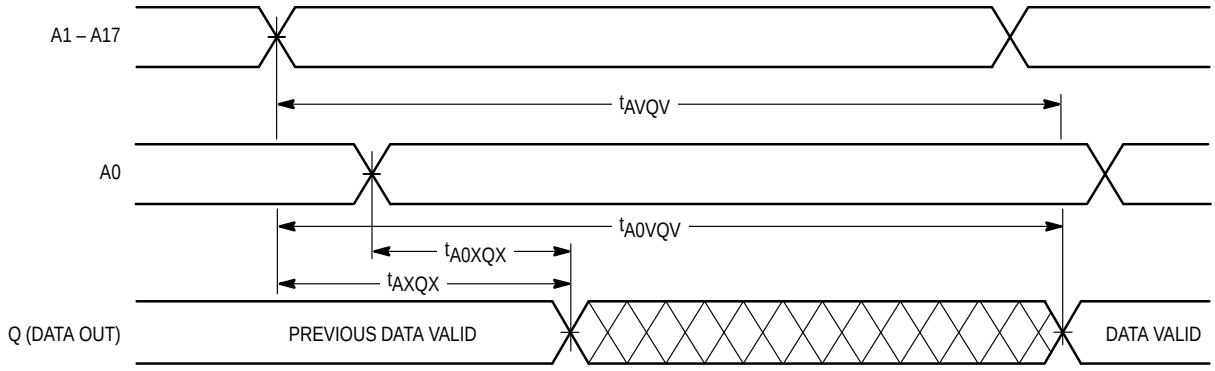


Figure 1. AC Test Load

TIMING LIMITS

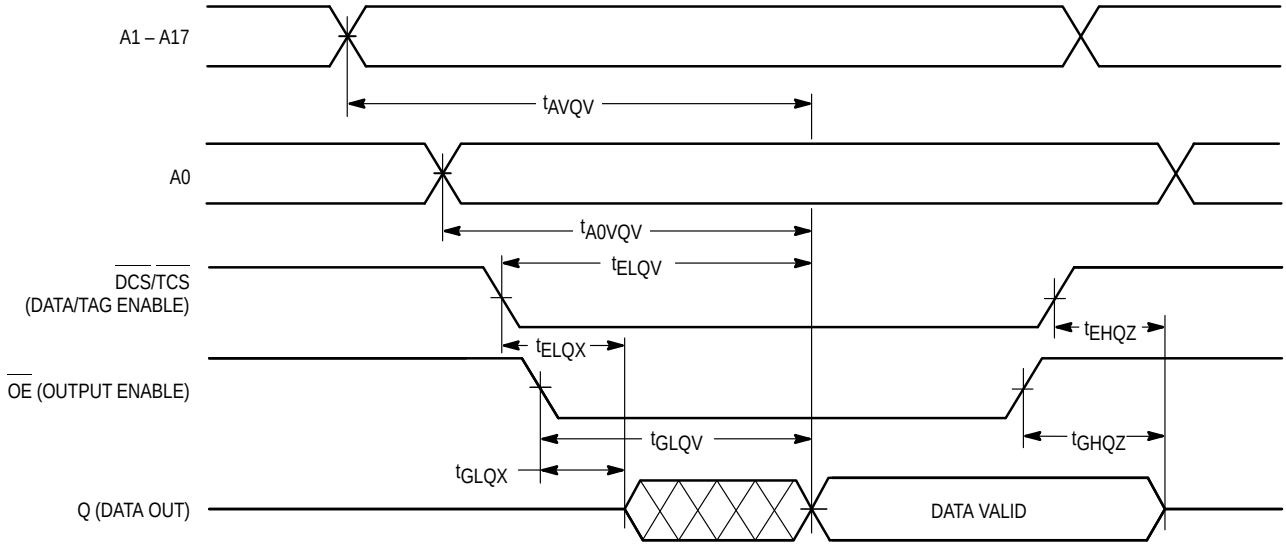
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note)



NOTE: Module is continuously selected ($\overline{DCS}$ or $\overline{TCS}$ = V_{IL}, $\overline{OE}$ = V_{IL}).

READ CYCLE 2 (See Note)



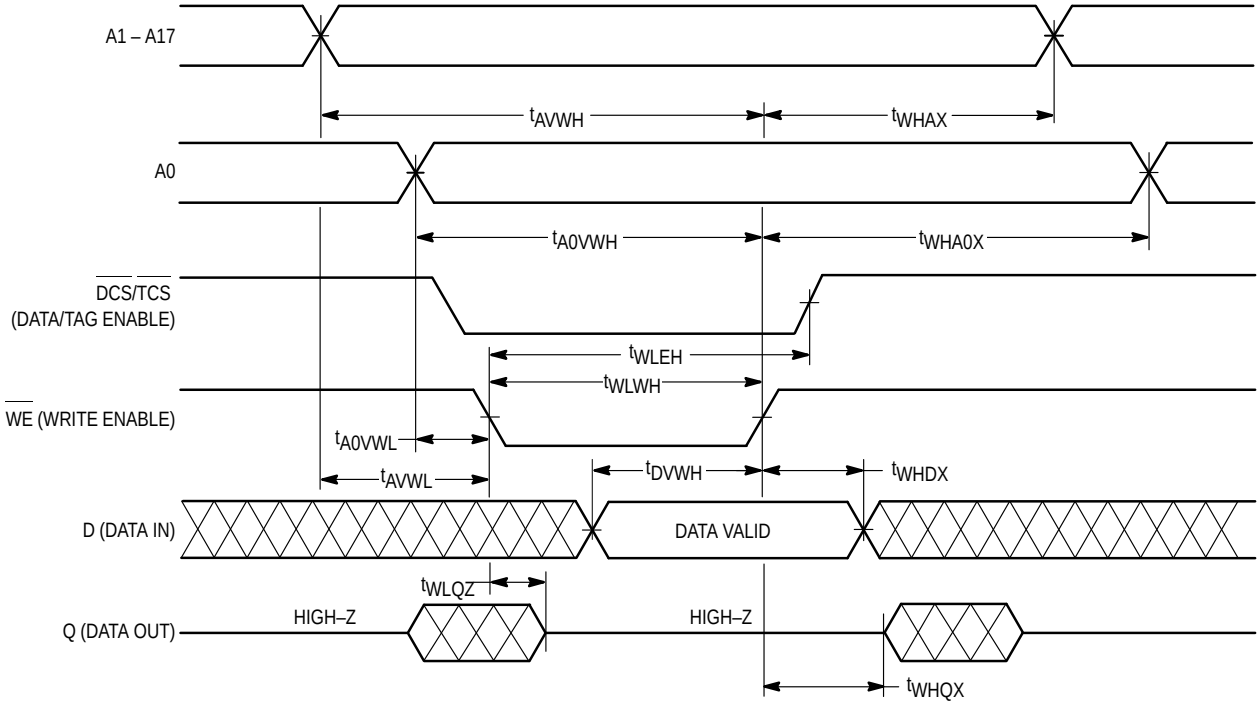
NOTE: Address valid prior to or coincident with $\overline{DCS}$ or $\overline{TCS}$ going low.

WRITE CYCLE 1 ($\overline{WE}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	–12		–15		–17		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Address Setup Time	t_{AVWL}	5	—	5	—	5	—	ns	
A0 Setup Time	t_{A0VWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	12	—	15	—	17	—	ns	
A0 Valid to End of Write	t_{A0VWH}	10	—	12	—	14	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	7	—	10	—	12	—	ns	
Data Valid to End of Write	t_{DVWH}	6	—	7	—	8	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	4	0	5	0	6	ns	3, 4
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	ns	3, 4
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	
Write Recovery Time — A0	t_{WHA0X}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{DCS}$ or $\overline{TCS}$ low and $\overline{WE}$ low.
2. Enable timings are the same for both DCS and TCS.
3. Transition is measured 200 mV from steady–state voltage.
4. This parameter is sampled and not 100% tested.

WRITE CYCLE 1

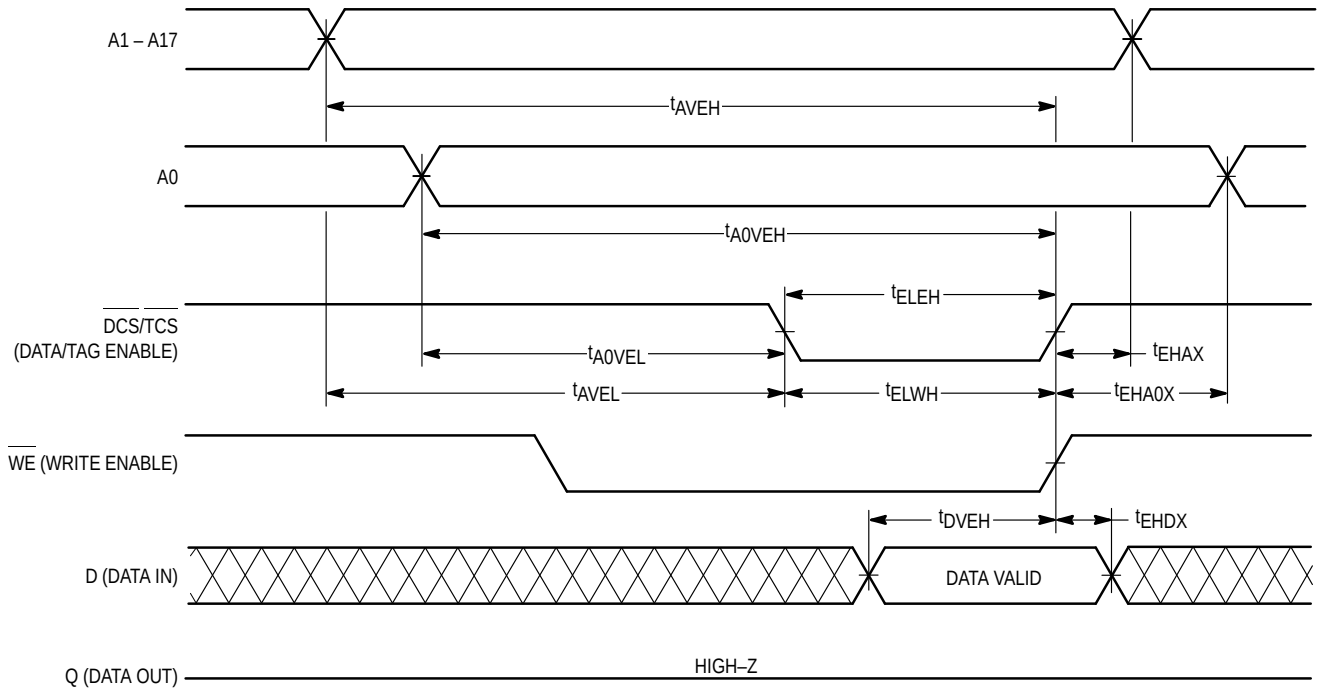


WRITE CYCLE 2 ($\overline{DCS}$ or $\overline{TCS}$ Controlled, See Notes 1 and 2)

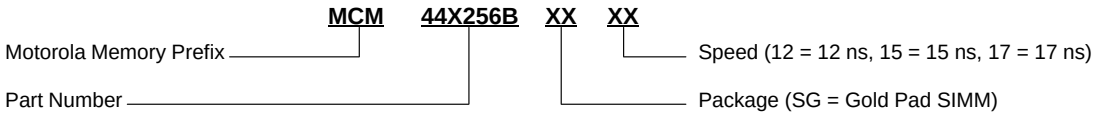
Parameter	Symbol	–12		–15		–17		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
A0 Setup Time	t_{A0VEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	12	—	15	—	17	—	ns	
A0 Valid to End of Write	t_{A0VEH}	10	—	12	—	14	—	ns	
Data/Tag Enable to End of Write	t_{ELEH}, t_{ELWH}	12	—	15	—	17	—	ns	
Data Valid to End of Write	t_{DVEH}	6	—	7	—	8	—	ns	
Data Hold Time	t_{EHDX}	5	—	5	—	5	—	ns	
Write Recovery Time	t_{EHAX}	5	—	5	—	5	—	ns	
Write Recovery Time — A0	t_{EHA0X}	5	—	5	—	5	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{DCS}$ or $\overline{TCS}$ low and $\overline{WE}$ low.
2. Enable timings are the same for both DCS and TCS.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)



Part Number	Unified/Split	Word Line Size	TAG Depth
MCM44A256B	Unified/Split	4	256K
MCM44B256B	Unified/Split	8	128K
MCM44C256B	Unified/Split	16	64K
MCM44D256B	Unified/Split	32	32K

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