MCM62110

32K x 9 Bit Synchronous Dual I/O or Separate I/O Fast Static RAM with Parity Checker

The MCM62110 is a 294,912 bit synchronous static random access memory organized as 32,768 words of 9 bits, fabricated using Motorola's high–performance silicon–gate CMOS technology. The device integrates a 32K x 9 SRAM core with advanced peripheral circuitry consisting of address registers, two sets of input data registers, two sets of output latches, active high and active low chip enables, and a parity checker. The RAM checks odd parity during RAM read cycles. The data parity error ($\overline{DPE}$) output is an open drain type output which indicates the result of this check. This device has increased output drive capability supported by multiple power pins. In addition, the output levels can be either 3.3 V or 5 V TTL compatible by choice of the appropriate output bus power supply.

The device has both asynchronous and synchronous inputs. Asynchronous inputs include the processor output enable ($\overline{POE}$), system output enable ($\overline{SOE}$), and the clock (K).

The address (A0 – A14) and chip enable ($\overline{E1}$ and E2) inputs are synchronous and are registered on the falling edge of K. Write enable ($\overline{W}$), processor input enable ($\overline{PIE}$) and system input enable ($\overline{SIE}$) are registered on the rising edge of K. Writes to the RAM are self–timed.

All data inputs/outputs, PDQ0 – PDQ7, SDQ0 – SDQ7, PDQP, and SDQP have input data registers triggered by the rising edge of the clock. These pins also have three–state output latches which are transparent during the high level of the clock and latched during the low level of the clock.

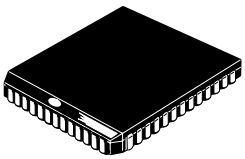
This device has a special feature which allows data to be passed through the RAM between the system and processor ports in either direction. This streaming is accomplished by latching in data from one port and asynchronously output enabling the other port. It is also possible to write to the RAM while streaming.

Additional power supply pins have been utilized for maximum performance. The output buffer power (V_{CCQ}) and ground pins (V_{SSQ}) are electrically isolated from V_{SS} and V_{CC}, and supply power and ground only to the output buffers. This allows connecting the output buffers to 3.3 V instead of 5.0 V if desired. If 3.3 V output levels are chosen, the output buffer impedance in the "high" state is approximately equal to the impedance in the "low" state thereby allowing simplified transmission line terminations.

The MCM62110 is available in a 52–pin plastic leaded chip carrier (PLCC).

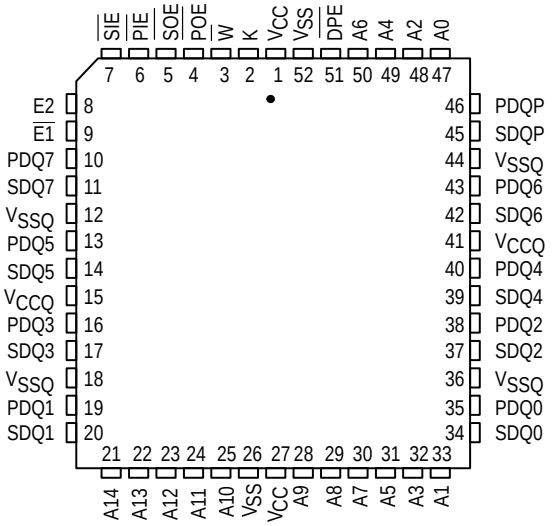
This device is ideally suited for pipelined systems and systems with multiple data buses and multiprocessing systems, where a local processor has a bus isolated from a common system bus.

- Single 5 V ± 10% Power Supply
- Choice of 5 V or 3.3 V ± 10% Power Supplies for Output Level Compatibility
- Fast Access and Cycle Times: 15/17/20 ns Max
- Self–Timed Write Cycles
- Clock Controlled Output Latches
- Address, Chip Enable, and Data Input Registers
- Common Data Inputs and Data Outputs
- Dual I/O for Separate Processor and Memory Buses
- Separate Output Enable Controlled Three–State Outputs
- Odd Parity Checker During Reads
- Open Drain Output on Data Parity Error ($\overline{DPE}$) Allowing Wire–ORing of Outputs
- High Output Drive Capability: 85 pF/Output at Rated Access Time
- High Board Density 52 Lead PLCC Package
- Active High and Low Chip Enables for Easy Memory Depth Expansion
- Can be used as Separate I/O x9



FN PACKAGE
PLASTIC
CASE 778–02

PIN ASSIGNMENT



PIN NAMES	
A0 – A14	Address Inputs
K	Clock Input
$\overline{W}$	Write Enable
$\overline{E1}$	Active Low Chip Enable
E2	Active High Chip Enable
$\overline{PIE}$	Processor Input Enable
$\overline{SIE}$	System Input Enable
$\overline{POE}$	Processor Output Enable
$\overline{SOE}$	System Output Enable
$\overline{DPE}$	Data Parity Error
PDQ0 – PDQ7	Processor Data I/O
PDQP	Processor Data Parity
SDQ0 – SDQ7	System Data I/O
SDQP	System Data Parity
V_{CC}	+ 5 V Power Supply
V_{CCQ}	Output Buffer Power Supply
V_{SSQ}	Output Buffer Ground
V_{SS}	Ground

All power supply and ground pins must be connected for proper operation of the device. $V_{CC} \geq V_{CCQ}$ at all times including power up.

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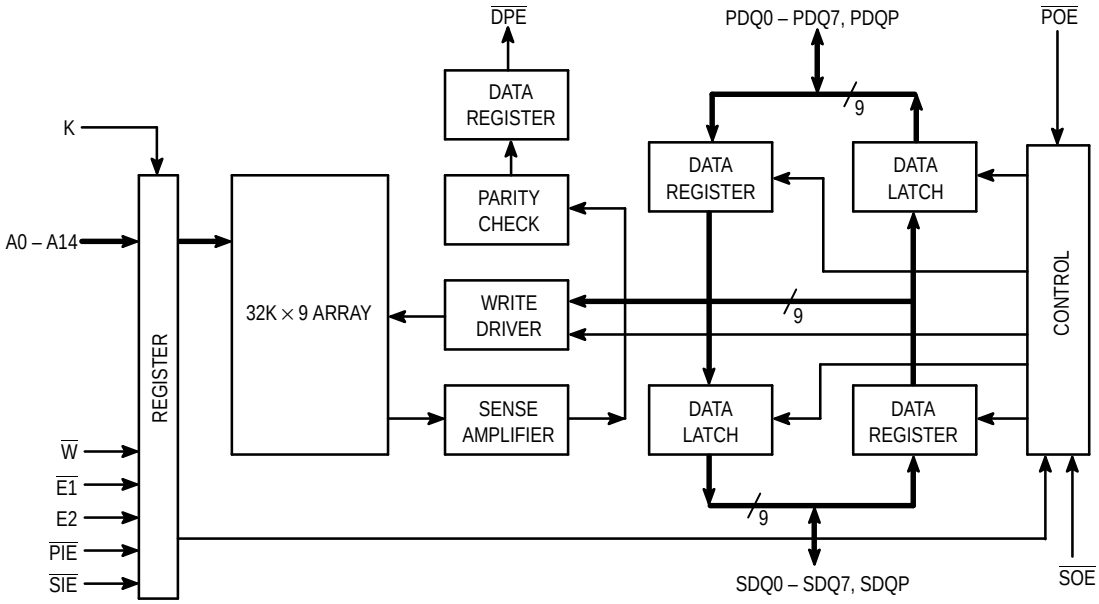
BLOCK DIAGRAM



FUNCTIONAL TRUTH TABLE (See Notes 1 and 2)

$\overline{W}$	$\overline{PIE}$	$\overline{SIE}$	$\overline{POE}$	$\overline{SOE}$	Mode	Memory Subsystem Cycle	PDQ0 – PDQ7, PDQP Output	SDQ0 – SDQ7, SDQP Output	$\overline{DPE}$	Notes
1	1	1	0	1	Read	Processor Read	Data Out	High–Z	Parity Out	3, 4
1	1	1	1	0	Read	Copy Back	High–Z	Data Out	Parity Out	3, 4
1	1	1	0	0	Read	Dual Bus Read	Data Out	Data Out	Parity Out	3, 4
1	X	X	1	1	Read	NOP	High–Z	High–Z	1	
X	0	0	X	X	N/A	NOP	High–Z	High–Z	1	2, 5
0	0	1	1	1	Write	Processor Write Hit	Data In	High–Z	1	2, 6
0	1	0	1	1	Write	Allocate	High–Z	Data In	1	2
0	0	1	1	0	Write	Write Through	Data In	Stream Data	1	2, 7
0	1	0	0	1	Write	Allocate With Stream	Stream Data	Data In	1	2, 7
1	0	1	1	0	N/A	Cache Inhibit Write	Data In	Stream Data	1	2, 7
1	1	0	0	1	N/A	Cache Inhibit Read	Stream Data	Data In	1	2, 7
0	1	1	X	X	N/A	NOP	High–Z	High–Z	1	5
X	0	1	0	0	N/A	Invalid	Data In	Stream	1	2, 8
X	0	1	0	1	N/A	Invalid	Data In	High–Z	1	2, 8
X	1	0	0	0	N/A	Invalid	Stream	Data In	1	2, 8
X	1	0	1	0	N/A	Invalid	High–Z	Data In	1	2, 8

NOTES:

1. A ‘0’ represents an input voltage ≤ V_{IL} and a ‘1’ represents an input voltage ≥ V_{IH}. All inputs must satisfy the specified setup and hold times for the falling or rising edge of K. Some entries in this truth table represent latched values. This table assumes that the chip is selected (i.e., $\overline{E1}$ = 0 and E2 = 1) and V_{CC} current is equal to I_{CCA}. If this is not true, the chip will be in standby mode, the V_{CC} current will equal I_{SB1} or I_{SB2} $\overline{DPE}$ will default to 1 and all RAM outputs will be in High–Z. Other possible combinations of control inputs not covered by this note or the table above are not supported and the RAM’s behavior is not specified.
2. If either $\overline{IE}$ signal is sampled low on the rising edge of clock, the corresponding $\overline{OE}$ is a don’t care, and the corresponding outputs are High–Z.
3. A read cycle is defined as a cycle where data is driven on the internal data bus by the RAM.
4. $\overline{DPE}$ is registered on the rising edge of K at the beginning of the following clock cycle
5. No RAM cycle is performed.
6. A write cycle is defined as a cycle where data is driven onto the internal data bus through one of the data I/O ports (PDQ0 – PDQ7 and PDQP or SDQ0 – SDQ7 and SPDQ), and written into the RAM.
7. Data is driven on the internal data bus by one I/O port through its data input register and latched into the data output latch of the other I/O port.
8. Data contention will occur.

PARITY CHECKER

Parity Scheme	$\overline{DPE}$
$\overline{E1} = V_{IH}$ and/or $E2 = V_{IL}$	1
RAMP = $\overline{RAM0 \oplus RAM1 \oplus \ldots \oplus RAM7}$	1
RAMP ≠ $\overline{RAM0 \oplus RAM1 \oplus \ldots \oplus RAM7}$	0

NOTE: RAMP, $\overline{RAM0}$, $\overline{RAM1}$ . . . , refer to the data that is present on the RAMs internal bus, not necessarily data that resides in the RAM array. $\overline{DPE}$ is always delayed one clock, and is registered on the rising edge of K at the beginning of the following clock cycle (see AC CHARACTERISTICS).

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to $V_{SS} = V_{SSQ} = 0$ V)

Rating	Symbol	Value	Unit
Power Supply	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC} and V_{CCQ}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.2	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = V_{SSQ} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Output Buffer Supply Voltage (5.0 V TTL Compatible) (3.3 V 50 Ω Compatible)	V_{CCQ}	4.5 3.0	5.5 3.6	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{POE}$, $\overline{SOE}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current (All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, I_{out} = 0 mA, Cycle Time ≥ t_{KHKH} min) MCM62110–15: t_{KHKH} = 15 ns MCM62110–17: t_{KHKH} = 17 ns MCM62110–20: t_{KHKH} = 20 ns	I_{CCA}	 — — —	 190 190 190	mA
TTL Standby Current (V_{CC} = Max, $\overline{E1}$ = V_{IH} or E2 = V_{IL})	I_{SB1}	—	40	mA
CMOS Standby Current (V_{CC} = Max, f = 0 MHz, $\overline{E1}$ = V_{IH} or E2 = V_{IL}, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V)	I_{SB2}	—	30	mA
Output Low Voltage (I_{OL} = + 8.0 mA, $\overline{DPE}$: I_{OL} = + 23.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except I/Os)	C_{in}	2	3	pF
Input/Output Capacitance (PDQ0 – PDQ7, SDQ0 – SDQ7, PDQP, SDQP)	C_{out}	6	7	pF
Data Parity Error Output Capacitance ($\overline{DPE}$)	$C_{out(DPE)}$	6	7	pF

AC SPEC LOADS

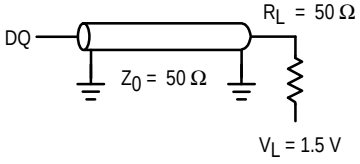


Figure 1A

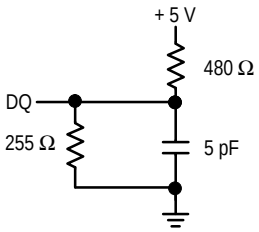


Figure 1B

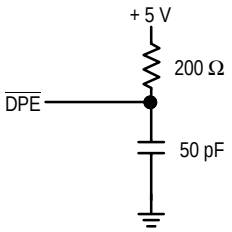


Figure 1C

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 3 ns

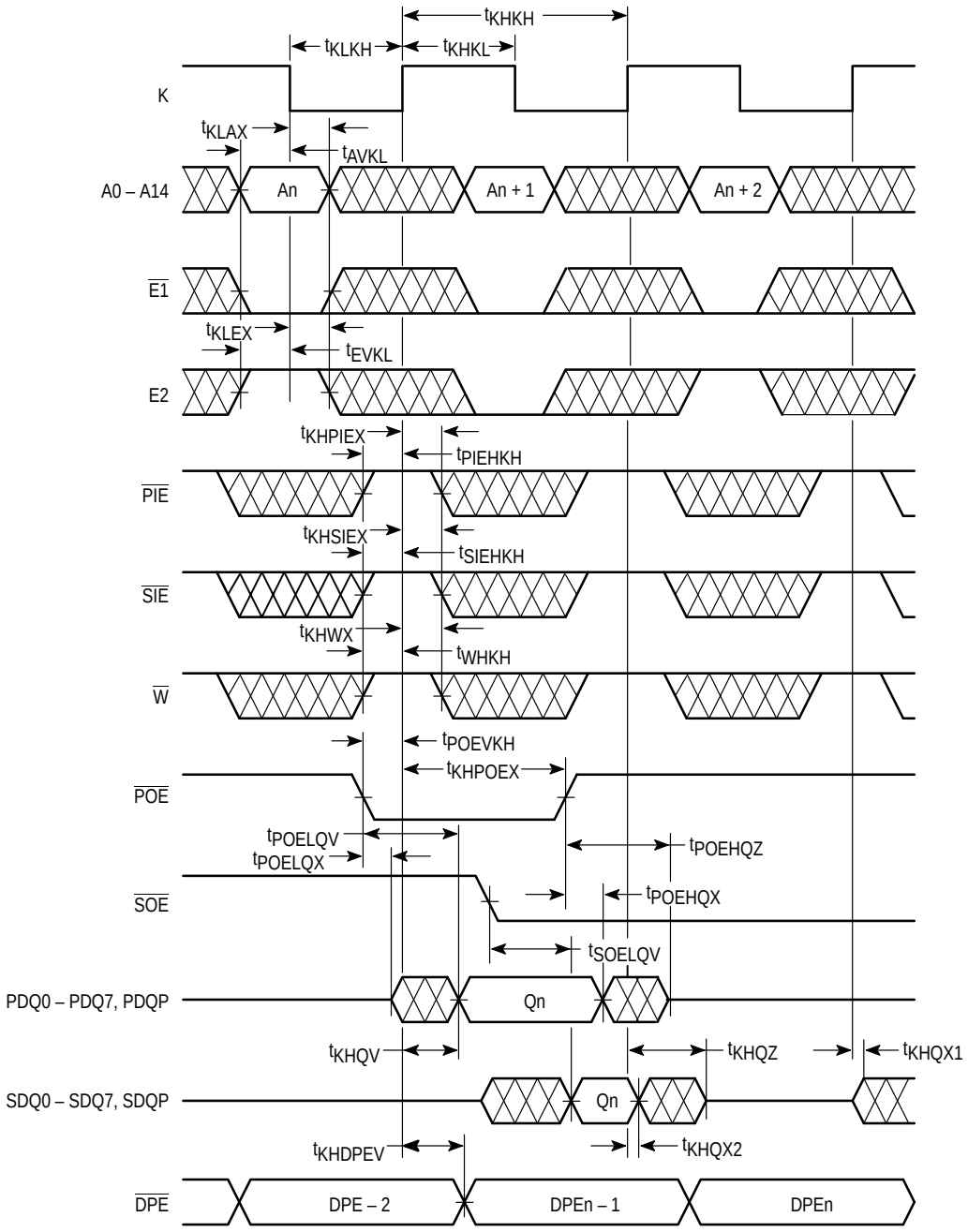
Output Measurement Timing Level . . . . . 1.5 V
Output Load . . . . . See Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

Parameter	Symbol	MCM62110–15		MCM62110–17		MCM62110–20		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time Clock High to Clock High	t_{KHKH}	15	—	17	—	20	—	ns	1, 2
Clock Low Pulse Width	t_{KLKH}	5	—	5	—	5	—	ns	
Clock High Pulse Width	t_{KHKL}	7	—	7	—	7	—	ns	
Clock High to $\overline{DPE}$ Valid	t_{KHDPEV}	—	7	—	8	—	10	ns	5
Clock High to Output Valid	t_{KHQV}	—	7	—	7.5	—	10	ns	4, 3
Clock (K) High to Output Low Z After Write	t_{KHQX1}	8	—	8	—	8	—	ns	
Output Hold from Clock High	t_{KHQX2}	5	—	5	—	5	—	ns	4, 6
Clock High to Q High–Z ($\overline{E1}$ or E2 = False)	t_{KHQZ}	—	8	—	9	—	10	ns	6
Setup TImes: A	t_{AVKL}	2.5	—	2.5	—	2.5	—	ns	
$\overline{W}$	t_{WHKH}								
$\overline{E1}$, E2	t_{EVKL}								
$\overline{PIE}$	t_{PIEHKH}								
$\overline{SIE}$	t_{SIEHKH}								
$\overline{POE}$	t_{POEVKH}								7
$\overline{SOE}$	t_{SOEVKH}								7
Hold Times: A	t_{KLAX}	2	—	2	—	2	—	ns	
$\overline{W}$	t_{KHWX}								
$\overline{E1}$, E2	t_{KLEX}								
$\overline{PIE}$	t_{KHPIEX}								
$\overline{SIE}$	t_{KHSIEX}								
$\overline{POE}$	t_{KHPOEX}								7
$\overline{SOE}$	t_{KHSOEX}								7
Output Enable High to Q High–Z	t_{POEHQZ} t_{SOEHQZ}	0	8	0	9	0	9	ns	6
Output Hold from Output Enable High	t_{POEHQX} t_{SOEHQX}	5	—	5	—	5	—	ns	6
Output Enable Low to Q Active	t_{POELQX} t_{SOELQX}	0	—	0	—	0	—	ns	6
Output Enable Low to Output Valid	t_{POELQV} t_{SOELQV}	—	5	—	6	—	8	ns	

NOTES:
1. A read is defined by $\overline{W}$ high for the setup and hold times.
2. All read cycle timing is referenced from K, $\overline{SOE}$, or $\overline{POE}$.
3. Access time is controlled by t_{KLQV} if the clock low pulse width is less than (t_{KLQV}–t_{KHQV}); otherwise it is controlled by KHQV.
4. K must be at a high level for outputs to transition.
5. $\overline{DPE}$ is valid exactly one clock cycle after the output data is valid.
6. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} is less than t_{KHQX}, t_{POEHQZ} is less than t_{POELQX} for a given device, and t_{SOEHQZ} is less than t_{SOELQX} for a given device.
7. These read cycle timings are used to guarantee proper parity operation only.

READ CYCLE (See Notes)



NOTES:
1. $\overline{DPE}$ is valid exactly one clock cycle after the output data is valid.

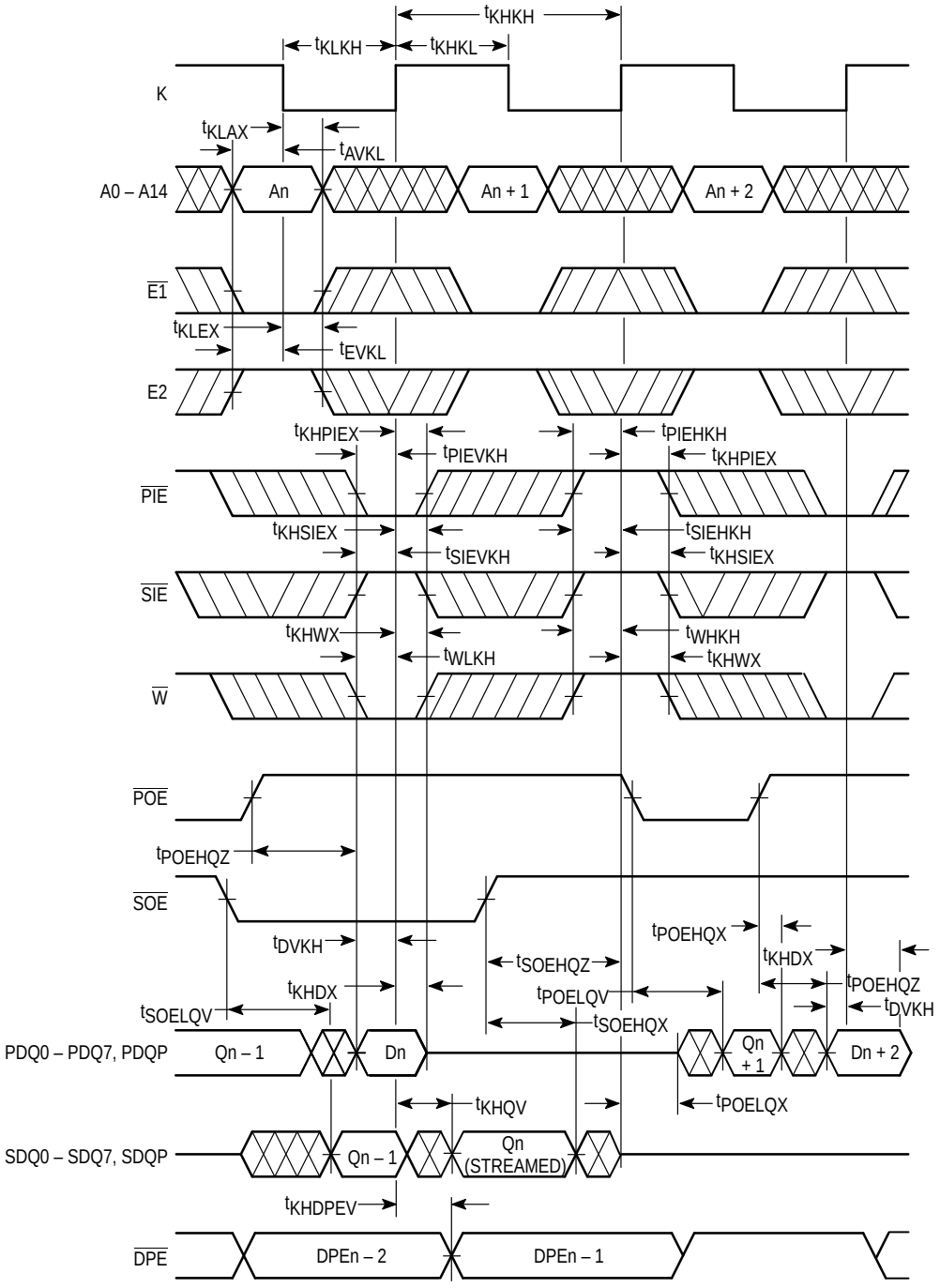
WRITE CYCLE (See Note 1)

Parameter	Symbol	MCM62110–15		MCM62110–17		MCM62110–20		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Times	t_{KHKH}	15	—	17	—	20	—	ns	1, 2
Clock Low Pulse Width	t_{KLKH}	5	—	5	—	5	—	ns	
Clock High Pulse Width	t_{KHKL}	7	—	7	—	7	—	ns	
Clock High to Output High–Z ($\overline{W}$ = V_{IL} and $\overline{SIE}$ = $\overline{PIE}$ = V_{IH})	t_{KHQZ}	—	8	—	9	—	10	ns	3, 4
Setup Times: A	t_{AVKL}	2.5	—	2.5	—	2.5	—	ns	
$\overline{W}$	t_{WLKH}								
$\overline{E1}$, E2	t_{EVKL}								
$\overline{PIE}$	t_{PIEVKH}								
$\overline{SIE}$	t_{SIEVKH}								
SDQ0 – SDQ7, SDQP, PDQ0 – PDQ7, PDQP	t_{DVKH}								
Hold Times: A	t_{KLAX}	2	—	2	—	2	—	ns	
$\overline{W}$	t_{KHWX}								
$\overline{E1}$, E2	t_{KLEX}								
$\overline{PIE}$	t_{KHPIEX}								
$\overline{SIE}$	t_{KHSIEX}								
SDQ0 – SDQ7, SDQP, PDQ0 – PDQ7, PDQP	t_{KHDX}								
Write with Streaming ($\overline{PIE}$ = $\overline{SOE}$ = V_{IL} or $\overline{SIE}$ = $\overline{POE}$ = V_{IL}) Clock High to Output Valid	t_{KHQV}	—	7	—	7.5	—	8	ns	5
Output Enable High to Q High–Z	t_{POEHQZ} t_{SOEHQZ}	0	8	0	9	0	9	ns	6
Output Hold from Output Enable High	t_{POEHQX} t_{SOEHQX}	5	—	5	—	5	—	ns	
Output Enable Low to Q Active	t_{POELQX} t_{SOELQX}	0	—	0	—	0	—	ns	6
Output Enable Low to Output Valid	t_{POELQV} t_{SOELQV}	—	5	—	6	—	8	ns	

NOTES:

1. A write is performed with $\overline{W}$ = V_{IL}, $\overline{E1}$ = V_{IL}, E2 = V_{IH} for the specified setup and hold times and either $\overline{PIE}$ = V_{IL} or $\overline{SIE}$ = V_{IL}. If both $\overline{PIE}$ = V_{IL} and $\overline{SIE}$ = V_{IL} or $\overline{PIE}$ = V_{IH} and $\overline{SIE}$ = V_{IH}, then this is treated like a NOP and no write is performed.
2. All write cycle timings are referenced from K.
3. K must be at a high level for the outputs to transition.
4. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} is less than t_{KHQX} for a given device.
5. A write with streaming is defined as a write cycle which writes data from one data bus to the array and outputs the same data onto the other data bus.
6. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} is less than t_{KHQX}, t_{POEHQZ} is less than t_{POELQX} for a given device, and t_{SOEHQZ} is less than t_{SOELQX} for a given device.

WRITE THROUGH — READ — WRITE (See Note)



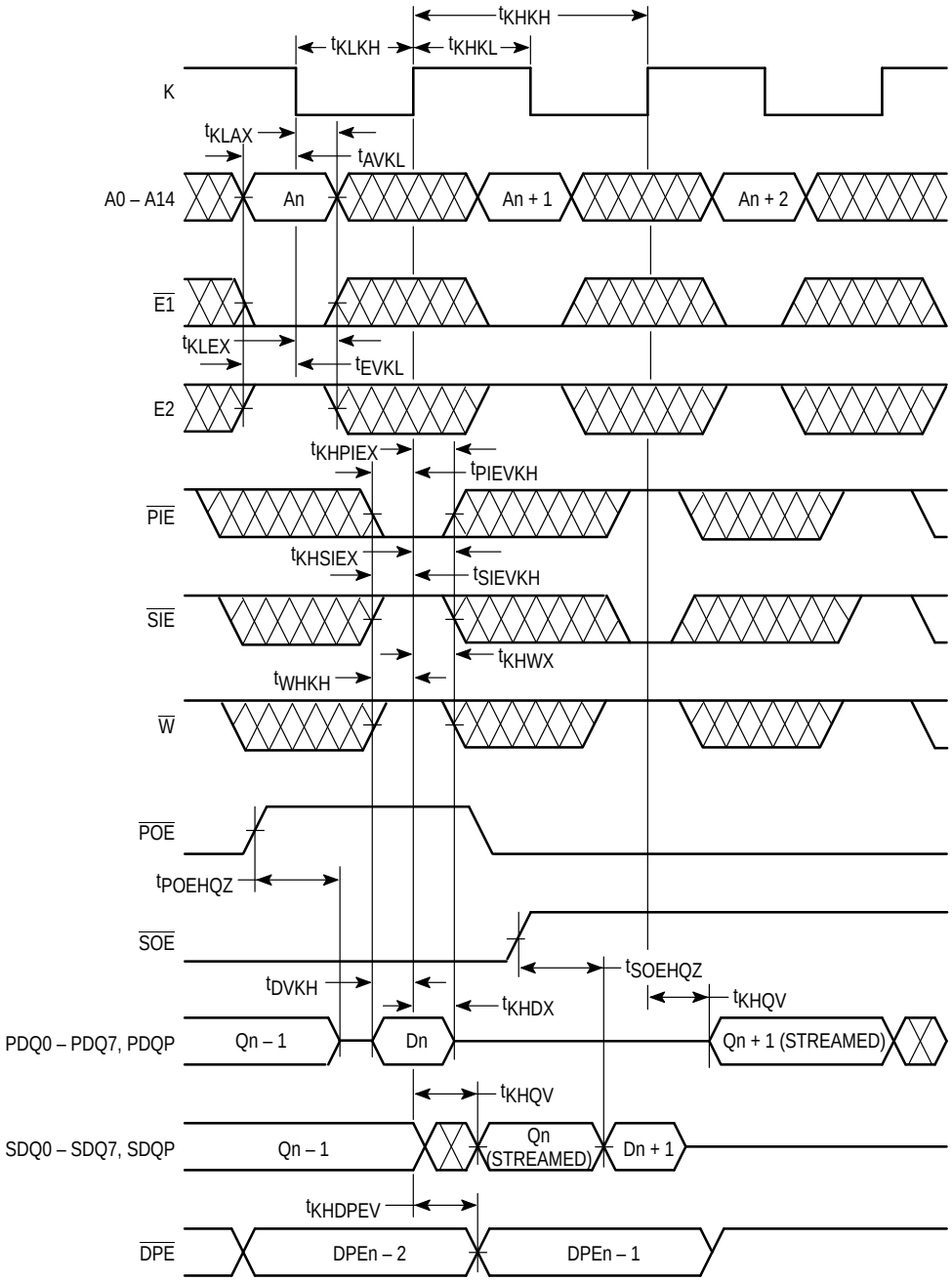
NOTE: $\overline{DPE}$ is valid exactly one clock cycle after the output data is written.

STREAM CYCLE (See Note 1)

Parameter	Symbol	MCM62110–15		MCM62110–17		MCM62110–20		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Stream Cycle Time	t_{KHKH}	15	—	17	—	20	—	ns	1, 2
Clock Low Pulse Width	t_{KLKH}	5	—	5	—	5	—	ns	
Clock High Pulse Width	t_{KHKL}	7	—	7	—	7	—	ns	
Stream Access Time	t_{KHQV}	—	7	—	7.5	—	8	ns	
Setup Times: A $\overline{W}$ $\overline{E1}$, E2 $\overline{PIE}$ $\overline{SIE}$ SDQ0 – SDQ7, SDQP, PDQ0 – PDQ7, PDQP	t_{AVKL} t_{WHKH} t_{EVKL} t_{PIEVKH} t_{SIEVKH} t_{DVKH}	2.5	—	2.5	—	2.5	—	ns	
Hold Times: A $\overline{W}$ $\overline{E1}$, E2 $\overline{PIE}$ $\overline{SIE}$ SDQ0 – SDQ7, SDQP, PDQ0 – PDQ7, PDQP	t_{KLAX} t_{KHWX} t_{KLEX} t_{KHPIEX} t_{KHSIEX} t_{KHDX}	2	—	2	—	2	—	ns	
Output Enable High to Q High–Z	t_{POEHQZ} t_{SOEHQZ}	0	8	0	9	0	9	ns	3
Output Enable Low to Q Active	t_{POELQX} t_{SOELQX}	0	—	0	—	0	—	ns	3
Output Enable Low to Output Valid	t_{POELQV} t_{SOELQV}	—	5	—	6	—	8	ns	

NOTES:
1. A stream cycle is defined as a cycle where data is passed from one data bus to the other data bus.
2. All stream cycle timing is referenced from K.
3. Transition is measured ±500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{POEHQZ} is less than t_{POELQX}, t_{SOEHQZ} is less than t_{SOELQX}, and t_{KHQZ} is less than t_{KHQX} for a given device.

STREAM CYCLE (See Note)



NOTE: $\overline{DPE}$ is valid exactly one clock cycle after the output data is valid.

ORDERING INFORMATION
(Order by Full Part Number)

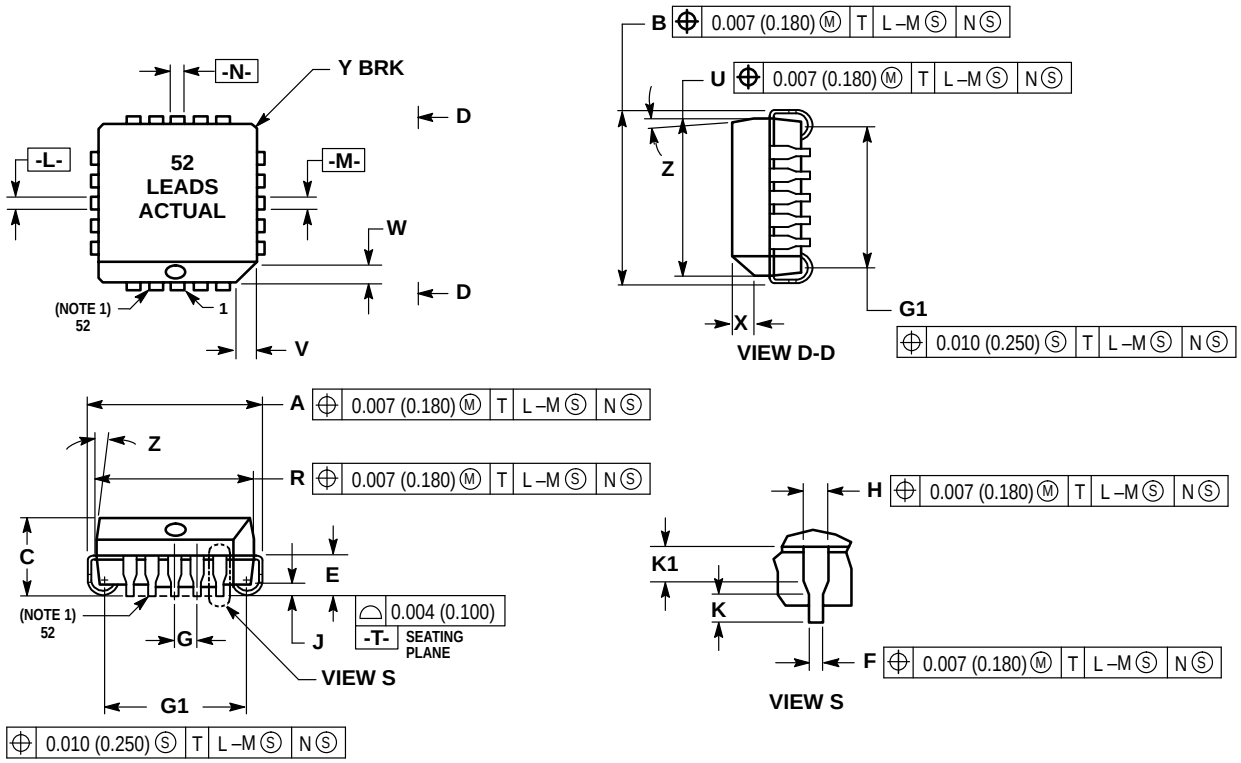
MCM 62110 FN XX

- MCM — Motorola Memory Prefix
- 62110 — Part Number
- FN — Package (FN = PLCC)
- XX — Speed (15 = 15 ns, 17 = 17 ns, 20 = 20 ns)

Full Part Numbers — MCM62110FN15 MCM62110FN17 MCM62110FN20

PACKAGE DIMENSIONS

FN PACKAGE
52–LEAD PLCC
CASE 778–02



NOTES:
1. **DUE TO SPACE LIMITATION, CASE 778-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 52 LEADS.**
2. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.
7. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
8. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.785	0.795	19.94	20.19
B	0.785	0.795	19.94	20.19
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.750	0.756	19.05	19.20
U	0.750	0.756	19.05	19.20
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.710	0.730	18.04	18.54
K1	0.040	—	1.02	—

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