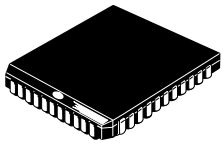
MCM62486B

32K x 9 Bit BurstRAM™ Synchronous Static RAM

With Burst Counter and Self–Timed Write



FN PACKAGE
44–LEAD PLCC
CASE 777–01

The MCM62486B is a 294,912 bit synchronous static random access memory designed to provide a burstable, high–performance, secondary cache for the i486 and Pentium™ microprocessors. It is organized as 32,768 words of 9 bits, fabricated with Motorola's high–performance silicon–gate CMOS technology. The device integrates input registers, a 2–bit counter, high speed SRAM, and high drive capability outputs onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (A0 – A14), data inputs (D0 – D8), and all control signals except output enable ($\overline{G}$) are clock (K) controlled through positive–edge–triggered noninverting registers.

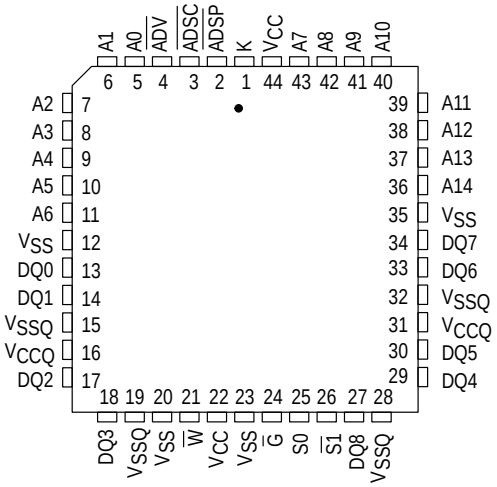
Bursts can be initiated with either address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be generated internally by the MCM62486B (burst sequence imitates that of the i486 and Pentium) and controlled by the burst address advance ($\overline{ADV}$) input pin. The following pages provide more detailed information on burst controls.

Write cycles are internally self–timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased flexibility for incoming signals.

The MCM62486B will be available in a 44–pin plastic leaded chip carrier (PLCC). Multiple power and ground pins have been utilized to minimize effects induced by output noise. Separate power and ground pins have been employed for DQ0 – DQ8 to allow user–controlled output levels of 5 volts or 3.3 volts.

- Single 5 V ± 10% Power Supply (± 5% for MCM62486BFN11)
- Choice of 5 V or 3.3 V ± 10% Power Supplies for Output Level Compatibility
- Fast Access Times:11/12/14/19 ns Max and Cycle Times:15/20/25 ns Min
- Internal Input Registers (Address, Data, Control)
- Internally Self–Timed Write Cycle
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Asynchronous Output Enable Controlled Three–State Outputs
- Common Data Inputs and Data Outputs
- High Output Drive Capability: 85 pF per I/O
- High Board Density PLCC Package
- Fully TTL–Compatible
- Active High and Low Chip Select Inputs for Easy Depth Expansion

PIN ASSIGNMENT



PIN NAMES

A0 – A14	Address Inputs
K	Clock
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
S0, $\overline{S1}$	Chip Selects
$\overline{ADV}$	Burst Address Advance
$\overline{ADSP}$, $\overline{ADSC}$	Address Status
DQ0 – DQ8	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{CCQ}	Output Buffer Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground

All power supply and ground pins must be connected for proper operation of the device. $V_{CC} \geq V_{CCQ}$ at all times including power up.

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i486 and Pentium are trademarks of Intel Corp.

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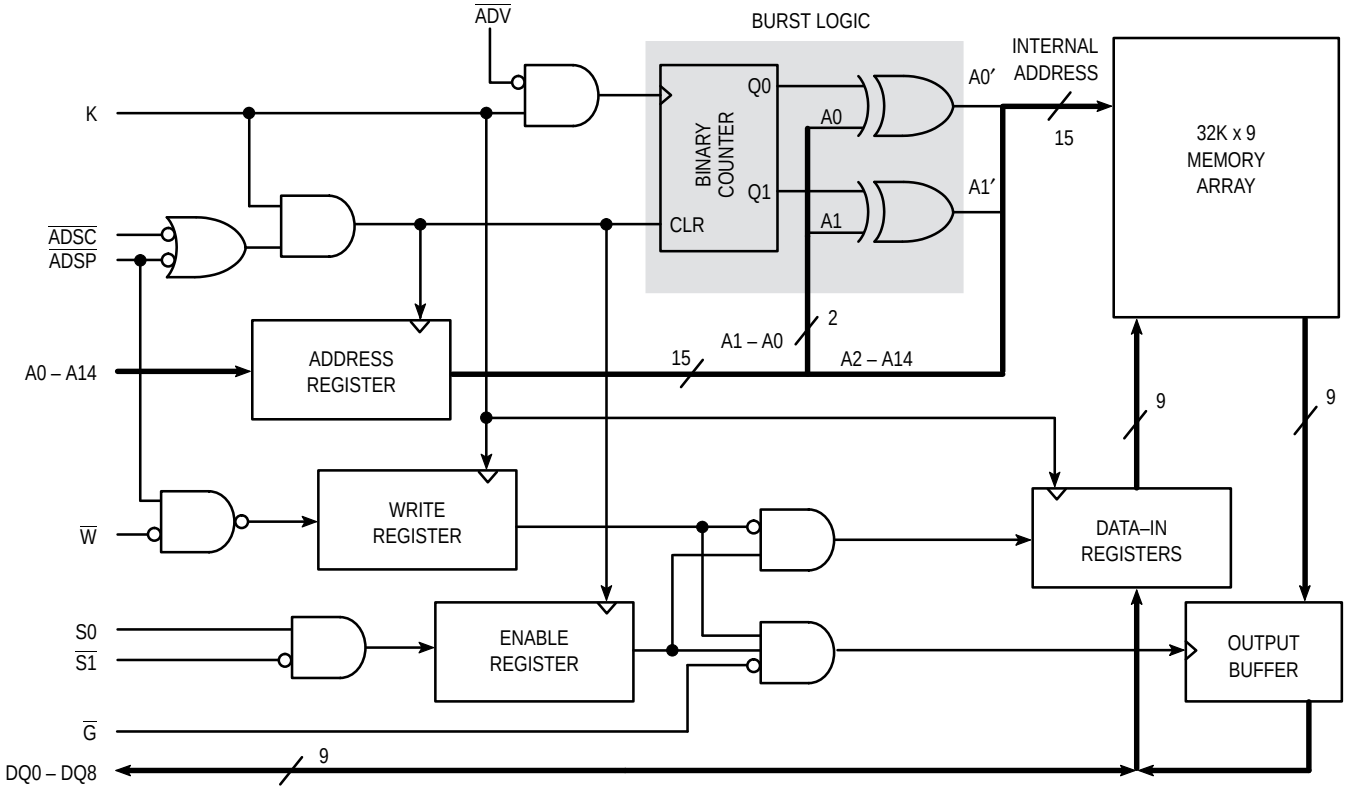
BLOCK DIAGRAM (See Note)



NOTE: All registers are positive–edge triggered. The $\overline{\text{ADSC}}$ or $\overline{\text{ADSP}}$ signals control the duration of the burst and the start of the next burst. When $\overline{\text{ADSP}}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{\text{W}}$ and $\overline{\text{ADSC}}$) is performed using the new external address. When $\overline{\text{ADSC}}$ is sampled low (and $\overline{\text{ADSP}}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{\text{W}}$) is performed using the new external address. Chip selects (S0, $\overline{\text{S1}}$) are sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{\text{ADV}}$ controls subsequent burst cycles. When $\overline{\text{ADV}}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{\text{ADV}}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**.

BURST SEQUENCE TABLE (See Note)

External Address	A14 – A2	A1	A0
1st Burst Address	A14 – A2	A1	$\overline{\text{A0}}$
2nd Burst Address	A14 – A2	$\overline{\text{A1}}$	A0
3rd Burst Address	A14 – A2	$\overline{\text{A1}}$	$\overline{\text{A0}}$

NOTE: The burst wraps around to its initial state upon completion.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, 3, and 4)

S	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{W}$	K	Address Used	Operation
F	L	X	X	X	L–H	N/A	Deselected
F	X	L	X	X	L–H	N/A	Deselected
T	L	X	X	X	L–H	External Address	Read Cycle, Begin Burst
T	H	L	X	L	L–H	External Address	Write Cycle, Begin Burst
T	H	L	X	H	L–H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low–to–high transition of clock (K).
3. S represents S0 and $\overline{S1}$. T implies $\overline{S1}$ = L and S0 = H; F implies $\overline{S1}$ = H or S0 = L.
4. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out (DQ0 – DQ8)
Read	H	High–Z
Write	X	High–Z — Data In (DQ0 – DQ8)
Deselected	X	High–Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Output Power Supply Voltage	V_{CCQ}	– 0.5 to V_{CC}	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC}, V_{CCQ} = 5.0 V ± 5%, T_A = 0 to + 70°C, for device MCM62486B–11)
(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to + 70°C, for all other devices)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Output Buffer Supply Voltage (5.0 V TTL Compatible) (3.3 V 50 Ω Compatible)	V_{CCQ}	 4.5 3.0	 5.5 3.6	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$, $\overline{S1}$ = V_{IH}, S0 = V_{IL}, V_{out} = 0 to V_{CCQ})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$, $\overline{S1}$ = V_{IL}, S0 = V_{IH}, All Inputs = V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, I_{out} = 0 mA, Cycle Time ≥ t_{KHKH} min)	I_{CCA}	—	160	mA
Standby Current ($\overline{S1}$ = V_{IH}, S0 = V_{IL}, All Inputs = V_{IL} and V_{IH}, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	50	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible i486 and Pentium bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ8)	C_{in}	2	3	pF
Input/Output Capacitance (DQ0 – DQ8)	$C_{I/O}$	7	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC}, V_{CCQ} = 5.0 V ± 5%, T_A = 0 to + 70°C, for device MCM62486B–11)
(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to + 70°C, for all other devices)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 3 ns

Output Timing Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	62486B–11		62486B–12		62486B–14		62486B–19		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	15	—	20	—	20	—	25	—	ns	
Clock Access Time	t_{KHQV}	—	11	—	12	—	14	—	19	ns	
Output Enable Access	t_{GLQV}	—	5	—	5	—	6	—	7	ns	
Clock High to Output Active	t_{KHQX1}	6	—	6	—	6	—	6	—	ns	
Clock High to Q Change	t_{KHQX2}	3	—	3	—	4	—	4	—	ns	
Output Enable to Q Active	t_{GLQX}	0	—	0	—	0	—	0	—	ns	
Output Disable to Q High–Z	t_{GHQZ}	—	6	—	6	—	6	—	7	ns	4
Clock High to Q High–Z	t_{KHQZ}	—	6	—	6	—	6	—	6	ns	
Clock High Pulse Width	t_{KHKL}	5.5	—	7	—	8	—	6	—	ns	
Clock Low Pulse Width	t_{KLKH}	5.5	—	7	—	8	—	6	—	ns	
Setup Times: Address Address Status Data In Write Address Advance Chip Select	t_{AVKH} t_{ADSVKH} t_{DVKH} t_{WVKH} t_{ADVVKH} t_{S0VKH} t_{S1VKH}	2	—	2	—	3	—	3	—	ns	5
Hold Times: Address Address Status Data In Write Address Advance Chip Select	t_{KHAX} t_{KHADSX} t_{KHDX} t_{KHWX} t_{KHADVX} t_{KHS0X} t_{KHS1X}	2	—	2	—	2	—	2	—	ns	5

NOTES:
1. A read cycle is defined by $\overline{W}$ high or $\overline{ADSP}$ low for the setup and hold times. A write cycle is defined by $\overline{W}$ low and $\overline{ADSP}$ high for the setup and hold times.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. $\overline{G}$ is a don't care when $\overline{W}$ is sampled low.
4. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX1} min for a given device and from device to device.
5. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of clock (K) whenever $\overline{ADSP}$ and $\overline{ADSC}$ are low and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is selected.Chip select must be true ($\overline{S1}$ low and S0 high) at each rising edge of clock for the device (when $\overline{ADSP}$ or $\overline{ADSC}$ is low) to remain enabled. Timings for $\overline{S1}$ and S0 are similar.

AC TEST LOADS

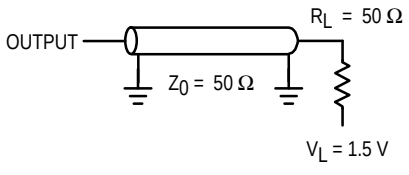


Figure 1A

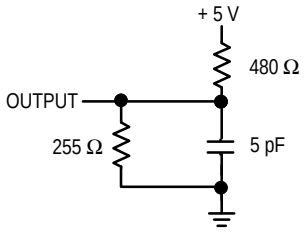
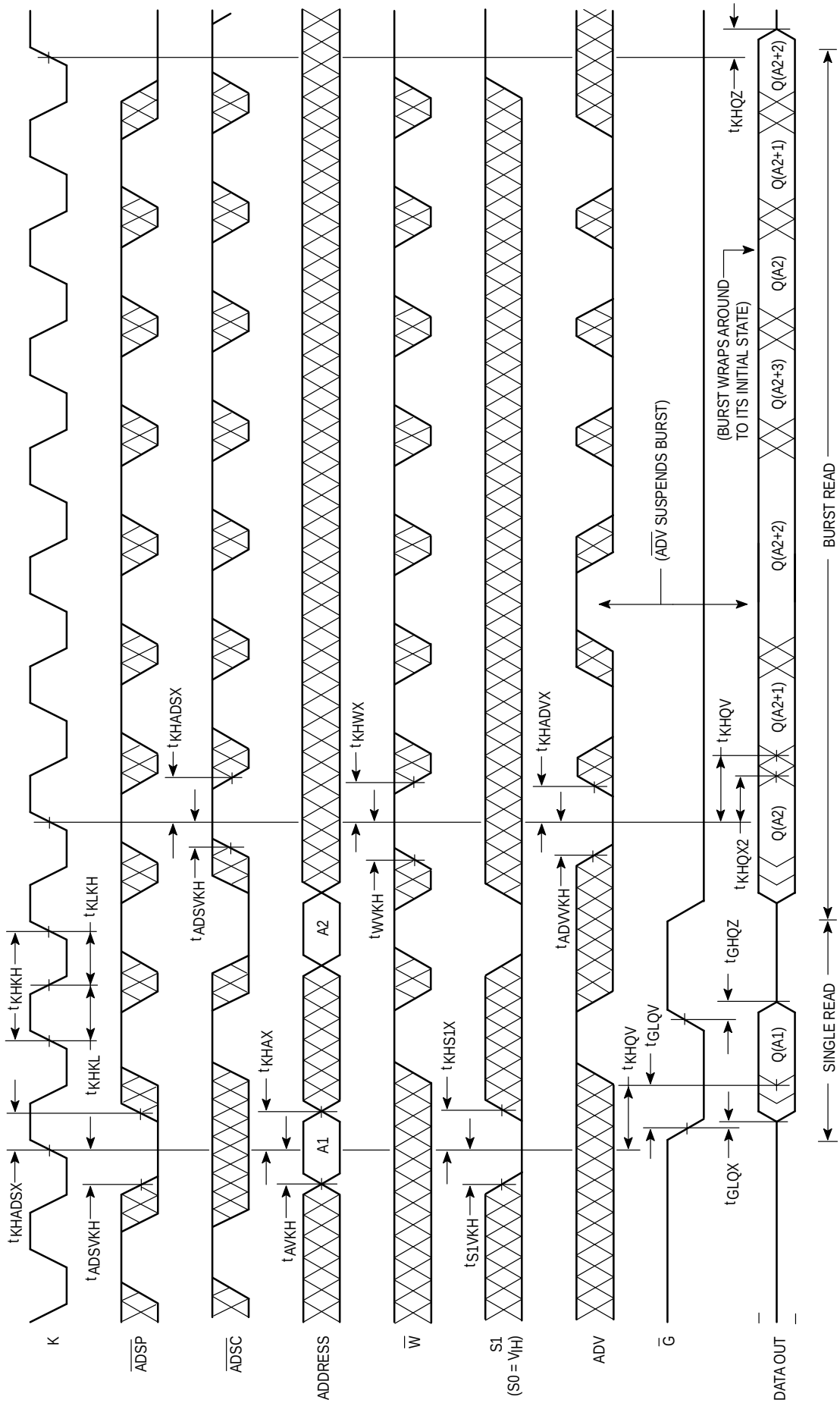


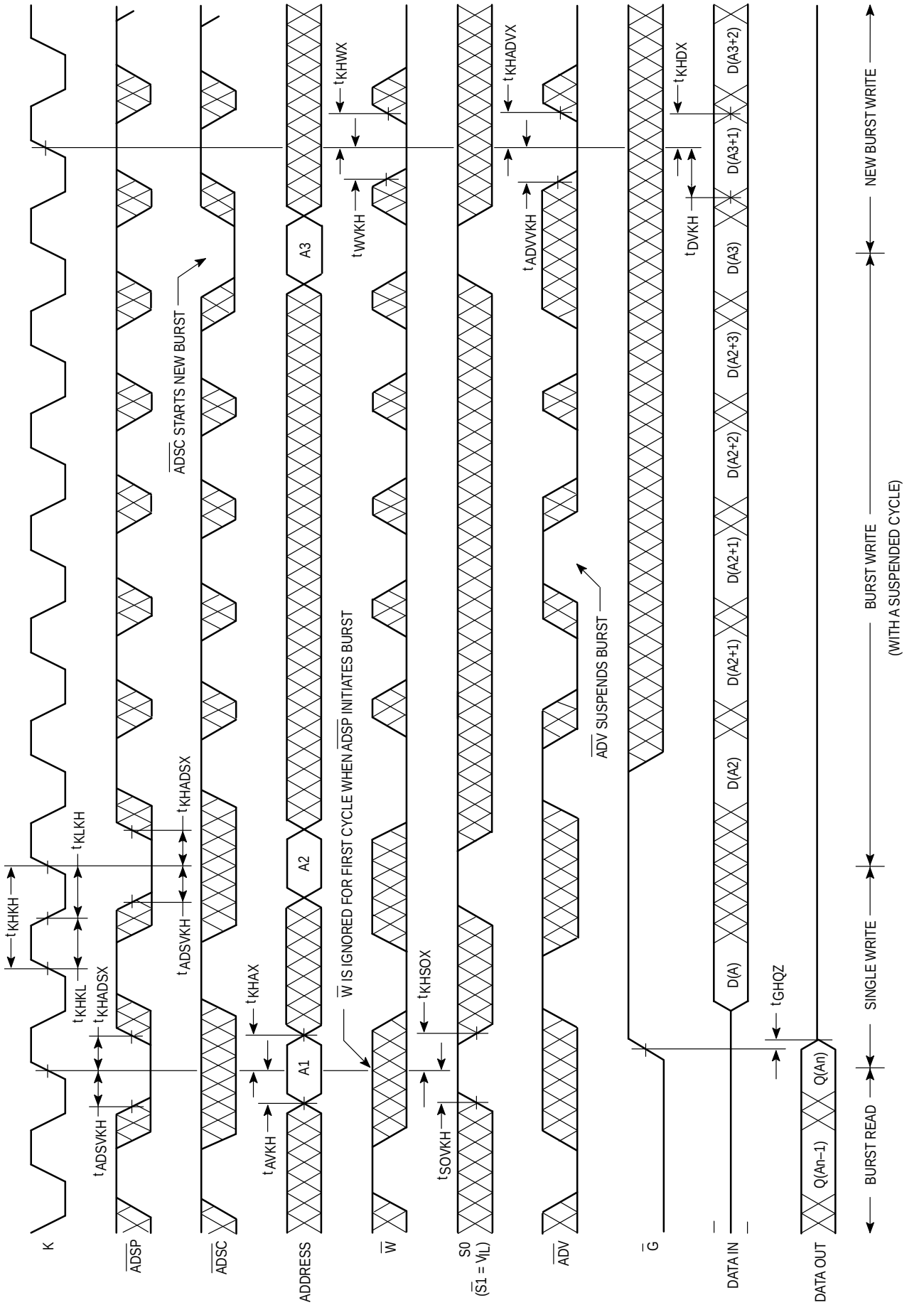
Figure 1B

READ CYCLES

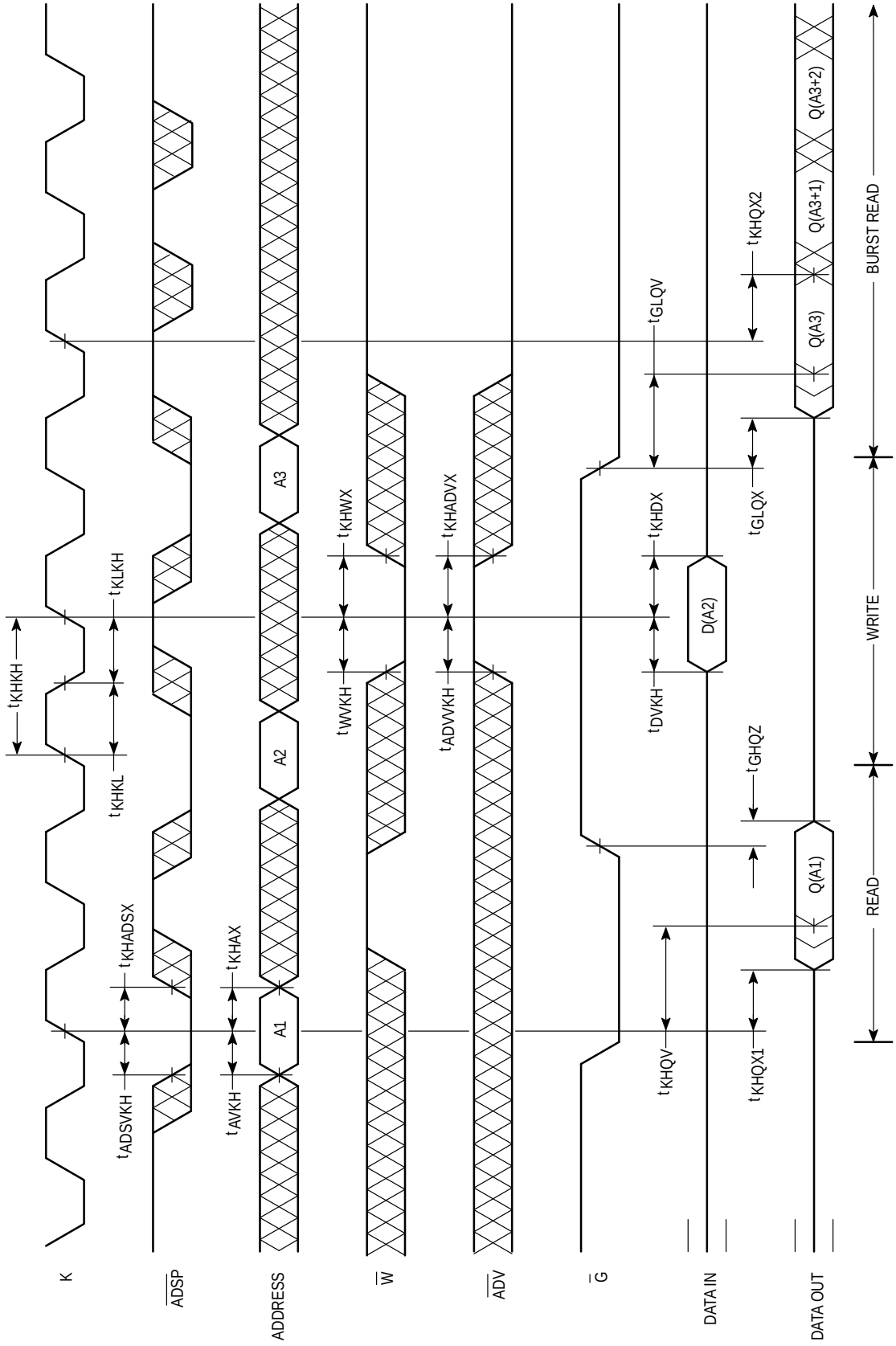


NOTE: Q(A2) represents the first output data from the base address A2; Q(A2+1) represents the next output data in the burst sequence with A2 as the base address.

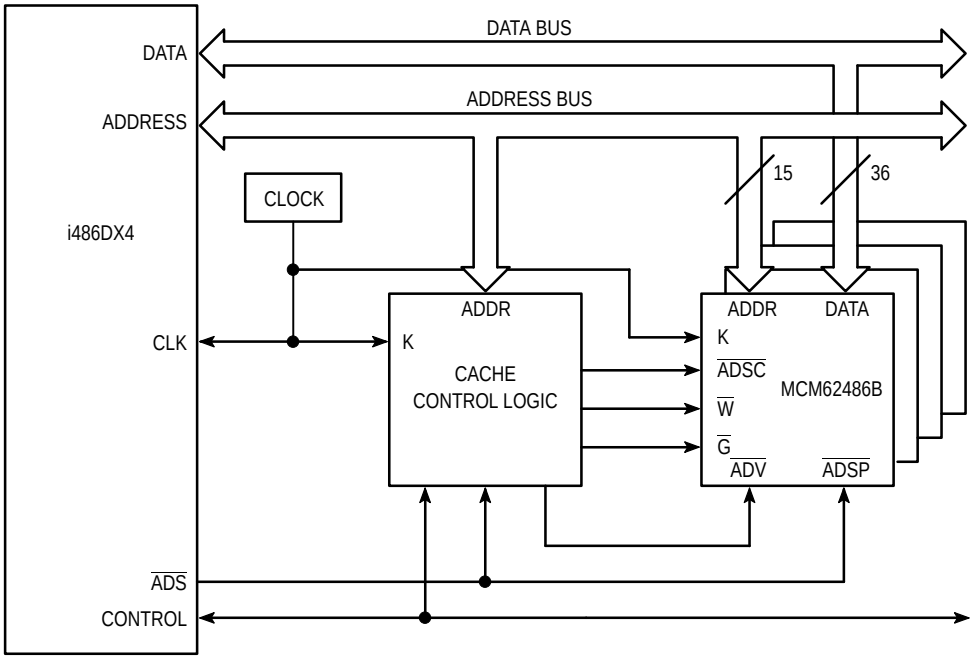
WRITE CYCLES



COMBINATION READ/WRITE CYCLE ($\overline{E}$ low, $\overline{ADSC}$ high)

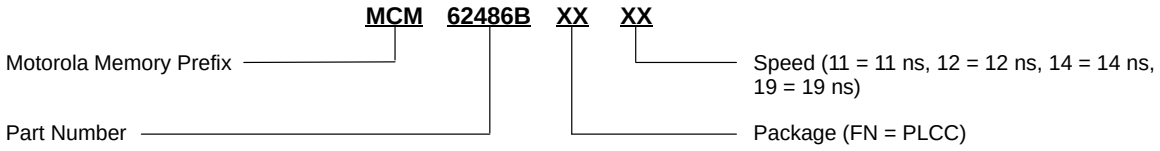


APPLICATION EXAMPLE



128K Byte Burstable, Secondary Cache Using
4 MCM62486BFN19s With a 100 MHz i486DX4

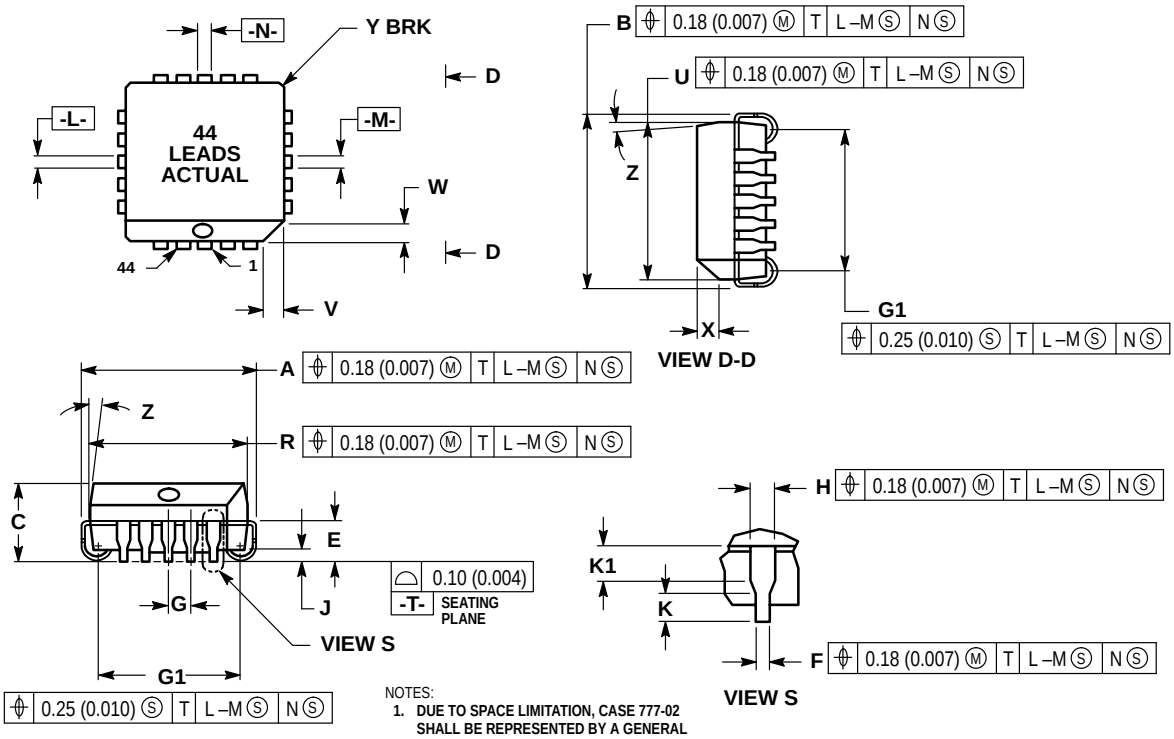
ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM62486BFN11 MCM62486BFN12 MCM62486BFN14 MCM62486BFN19

PACKAGE DIMENSIONS

FN PACKAGE
44–LEAD PLCC
CASE 777–02



NOTES:

1. **DUE TO SPACE LIMITATION, CASE 777-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 44 LEADS.**
2. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.25 (0.010) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.
7. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO .012 (.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
8. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN .037 (.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN .025 (.635).
9. 777-01 IS OBSOLETE, NEW STANDARD 777-02.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.40	17.65	0.685	0.695
B	17.40	17.65	0.685	0.695
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	16.51	16.66	0.650	0.656
U	16.51	16.66	0.650	0.656
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	15.50	16.00	0.610	0.630
K1	1.02	—	0.040	—

Literature Distribution Centers:
USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.
JAPAN: Nippon Motorola Ltd.; 4–32–1, Nishi–Gotanda, Shinagawa–ku, Tokyo 141, Japan.
ASIA PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.