MCM62973A

Product Preview

4K × 12 Bit Synchronous Static RAM

with Output Registers

FN PACKAGE
44-LEAD PLCC
CASE 777

The MCM62973A is a 49,152 bit synchronous static random access memory organized as 4096 words of 12 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS II) technology. The device integrates input registers, high speed SRAM, and high-drive capability output registers onto a single monolithic circuit for reduced parts count implementation of cache data RAM, writeable control store applications, and other applications that utilize long words.

Synchronous design allows precise cycle control with the use of an external clock (K), while CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

The address (A0-A11), data (D0-D11), write ($\overline{W}$), and chip enable ($\overline{E}$) inputs are all clock (K) controlled, positive-edge-triggered, noninverting registers.

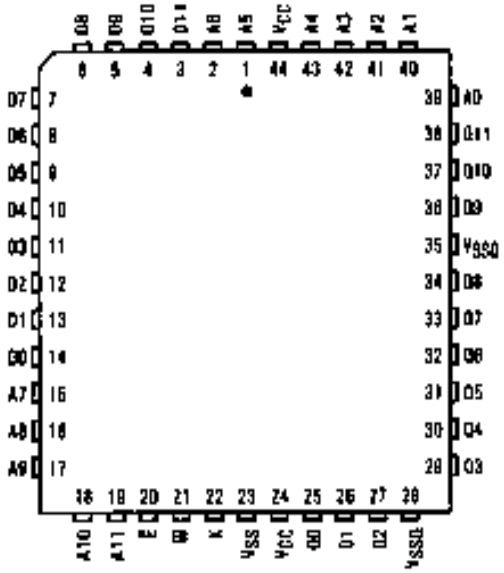
The chip enable ($\overline{E}$) input is a synchronous input clock that places the device in a low power mode when high at the rising edge of the clock (K).

The MCM62973A provides output register operation. At the rising edge of clock (K), the RAM data from the previous clock (K) high cycle is presented.

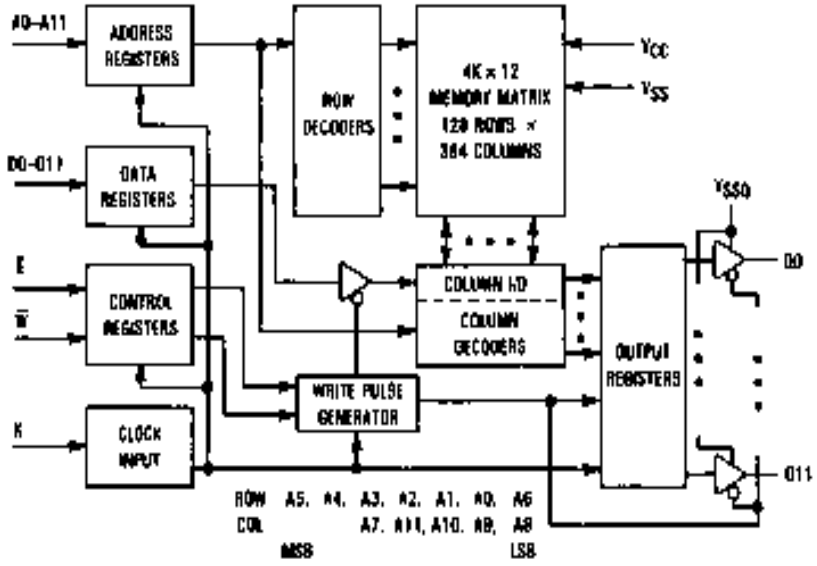
Write operations are internally self-timed and initiated by the rising edge of the clock (K) input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

- Single 5 V ±10% Power Supply
- Fast Cycle Times: 18/20 ns Max
- Fast Clock (K) Access Times: 10/10 ns Max
- Address, Data Input, $\overline{E}$, and $\overline{W}$ Registers On-Chip
- Output Registers for Fully Pipelined Applications
- High Output Drive Capability
- Internally Self-Timed Write Pulse Generation
- Separate Data Input and Data Output Pins

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES	
A0-A11	Address Inputs
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
D0-D11	Data Inputs
Q0-Q11	Data Outputs
K	Clock Input
V_{CC}	+5 V Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground

For proper operation of the device V_{SS} and both V_{SSQ} leads must be connected to ground.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

TRUTH TABLE

$\overline{E}$	$\overline{W}$	Operation	Q0-Q11	Current
L	L	Write	High Z	I_{CC}
L	H	Read	D_{out}	I_{CC}
H	X	Not Selected	High Z	I_{SB}

NOTE: The values of $\overline{E}$ and $\overline{W}$ are valid inputs for the setup and hold times relative to the K rising edge.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of the clock (K) while the device is selected.

This device contains circuitry that will ensure the output devices are in High Z at power up. Care should be taken by the user to ensure that all clocks are at V_{IL} or V_{IH} during power up to prevent spurious read cycles from occurring.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	±1.0	μA
Output Leakage Current ($\overline{E} = V_{IH}$, V_{out} = 0 to V_{CC}, Outputs must be in High Z)	$I_{lkg(O)}$	—	±1.0	μA
AC Supply Current ($\overline{E} = V_{IL}$, All Inputs = V_{IL} or V_{IH}, I_{out} = 0 mA, Cycle Time ≥ t_{KHKH} min) MCM62973A-18: t_{KHKH} = 18 ns MCM62973A-20: t_{KHKH} = 20 ns	I_{CCA}	 — —	 170 160	mA
Standby Current ($\overline{E} = V_{IH}$, $V_{IH} \geq 3.0$ V, $V_{IL} \leq 0.4$ V, I_{out} = 0 mA, Cycle Time ≥ = t_{KHKH} min)	I_{SB}	—	30	mA
Output Low Voltage (I_{OL} = 12.7 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −1.8 mA)	V_{OH}	2.8	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	3	4	pF
Output Capacitance	C_{out}	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . .See Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

Parameter	Symbol	MCM62973A–18		MCM62973A–20		Unit	Notes
		Min	Max	Min	Max		
Read Cycle Time	t_{KHKH}	18	—	20	—	ns	2
Clock Access Time	t_{KHQV}	—	10	—	10	ns	3
Output Active from Clock High	t_{KHQX}	3	—	3	—	ns	4
Clock High to Q High Z ($\overline{E}$=V_{IH})	t_{KHQZ}	—	10	—	10	ns	4
Clock Low Pulse Width	t_{KLKH}	5	—	5	—	ns	
Clock High Pulse Width	t_{KHKL}	5	—	5	—	ns	
Setup Times for: $\overline{E}$	t_{EVKH}	4	—	4	—	ns	5
A	t_{AVKH}						
$\overline{W}$	t_{WHKH}						
Hold Times for: $\overline{E}$	t_{KHEX}	2	—	2	—	ns	5
A	t_{KHAX}						
$\overline{W}$	t_{KHWX}						

NOTES:
1. A read is defined by $\overline{W}$ high and $\overline{E}$ low for the setup and hold times.
2. All read cycle timing is referenced from K.
3. Valid data from K high will be the data stored at the address of the last valid read cycle.
4. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX} min for a given device.
5. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.

AC TEST LOADS

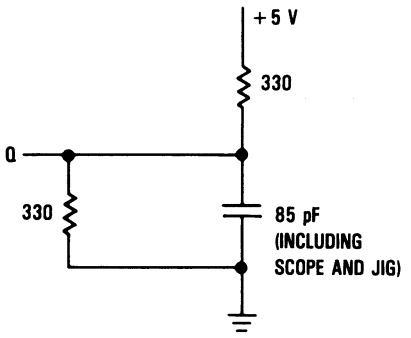


Figure 1A

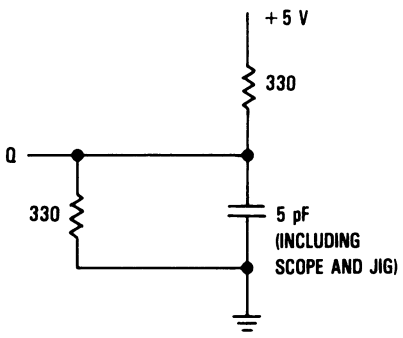
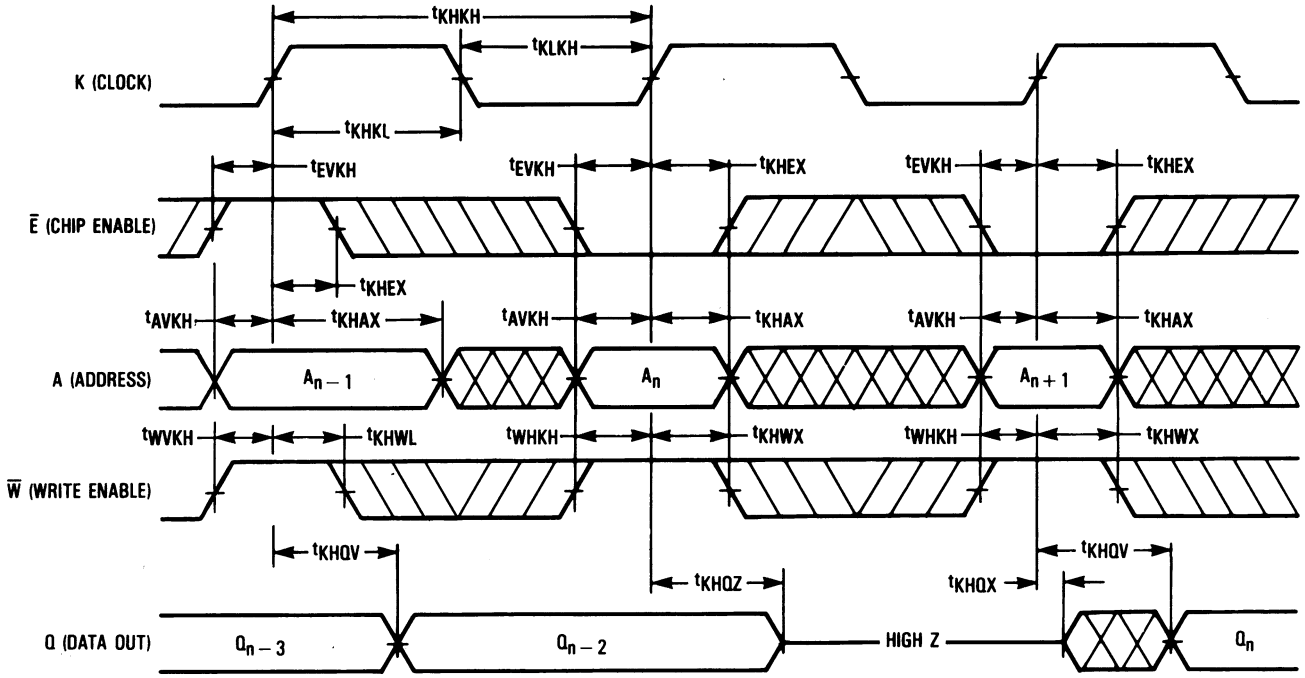
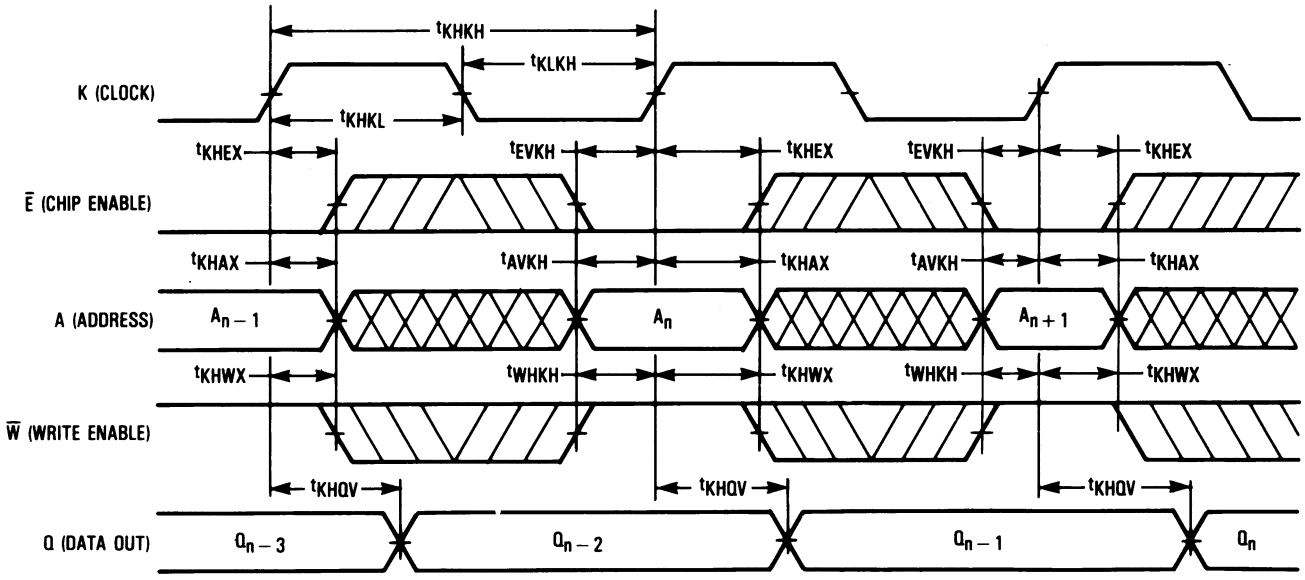


Figure 1B

READ CYCLE 1 (See Note 1)



READ CYCLE 2 (See Note 1)



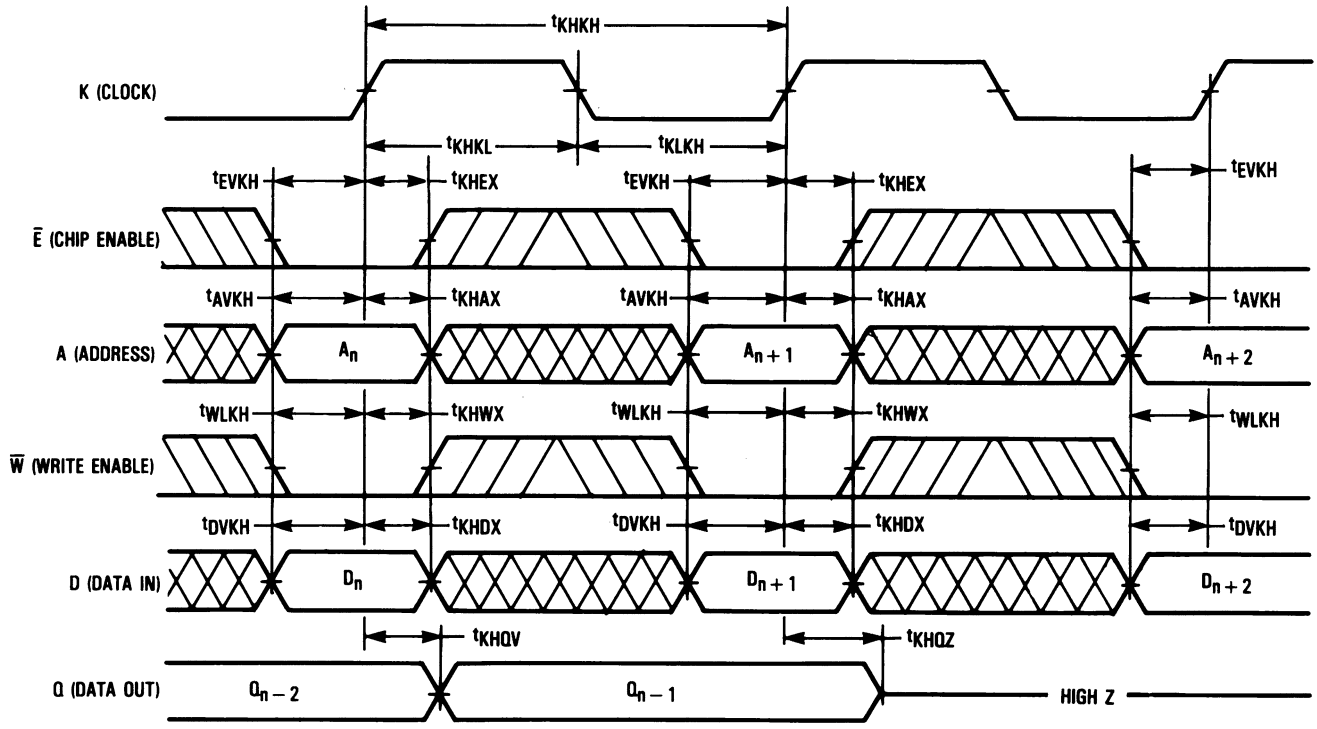
NOTE:
1. The outputs Q_{n-3} and Q_{n-2} are derived from two previous read cycles where $\overline{W} = V_{IH}$ and $\overline{E} = V_{IL}$ for those cycles.

WRITE CYCLE (W Controlled, See Note 1)

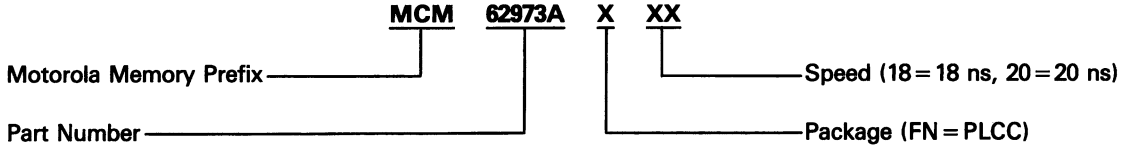
Parameter		Symbol	MCM62973A-18		MCM62973A-20		Unit	Notes
			Min	Max	Min	Max		
Write Cycle Time		t_{KHKH}	18	—	20	—	ns	2
Clock High to Output High Z ($\overline{W} = V_{IL}$)		t_{KHQZ}	—	10	—	10	ns	3
Setup Times for:	$\overline{E}$	t_{EVKH}	4	—	4	—	ns	4
	A	t_{AVKH}						
	$\overline{W}$	t_{WLKH}						
	D	t_{DVKH}						
Hold Times for:	$\overline{E}$	t_{KHEX}	2	—	2	—	ns	4
	A	t_{KHAX}						
	$\overline{W}$	t_{KHWX}						
	D	t_{KHDX}						

NOTES:
1. A write is performed when $\overline{W}$ and $\overline{E}$ are both low for the specified setup and hold times.
2. All write cycle timing is referenced from K.
3. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX} min for a given device.
4. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.

WRITE CYCLE



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers—MCM62973AFN18 MCM62973AFN20