Advance Information
64K x 36 Bit Pipelined BurstRAM Synchronous Fast Static RAM

MCM63P636

ZP PACKAGE
PBGA
CASE 1107–01

TQ PACKAGE
TQFP
CASE 983A–01

The MCM63P636 is a 2M–bit synchronous fast static RAM designed to provide burstable, high performance, secondary cache for advanced microprocessors. It is organized as 64K words of 36 bits each. This device integrates input registers, an output register, a 2–bit address counter, and a high speed SRAM onto a single monolithic circuit for reduced parts count in cache data RAM applications. Synchronous design allows for precise cycle control with the use of an external clock (K) and external strobe clock (SK).

Addresses (SA), data inputs (DQx), and all control signals are clock (K) controlled through positive–edge–triggered noninverting registers. Data strobes STRBA, STRBA, STRBB, and STRBB are strobe clock (SK) controlled through positive–edge–triggered non–inverting registers. Strobe clock, 180 degrees out of phase with clock (K), is only used with the data strobes such that they are centered with data output on read cycles.

Burst sequences are initiated with ADS input pin, and subsequent burst addresses are generated internally by MCM63P636.

Write cycles are internally self–timed and are initiated with address and control logic by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased timing flexibility for incoming signals. Special logic enables the memory to accept data on the rising edge of clock (K) a cycle after address and control signals.

For read cycles, the SRAMs output data is temporarily stored by an edge–triggered output register and then released to the output buffers at the second rising edge of clock (K) for a read latency of three cycles. Data strobes rise and fall with SRAM output to help external devices receiving the data to latch the data.

The MCM63P636 operates from a 3.3 V core power supply, a 2.0 V input power supply, and a 2.0 V I/O power supply. These power supplies are designed so that power sequencing is not required.

- MCM63P636–250 = 3.9 ns Access/4 ns Cycle (250 MHz)
  MCM63P636–225 = 4.3 ns Access/4.4 ns Cycle (225 MHz)
  MCM63P636–200 = 4.9 ns Access/5 ns Cycle (200 MHz)
- 3.3 V $\pm$ 200 mV V_{DD} Supply, 2.0 V V_{DDI} and V_{DDQ} Supply
- Internally Self–Timed Late Write Cycle
- Three–Cycle Single–Read Latency
- Strobe Clock Input and Data Strobe Output Pins
- On–Chip Output Enable Control
- On–Chip Burst Advance Control
- Four–Tick Burst
- Power–On Reset Pin
- Low Power Stop Clock Operation
- Boundary Scan (PBGA Only)
- JEDEC Standard 153–Pin PBGA and 100–Pin TQFP Packages
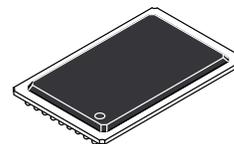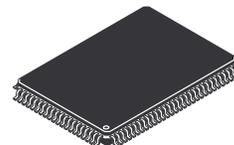
This document contains information on a new product. Specifications and information herein are subject to change without notice.

MOTOROLA

**PBGA
PIN ASSIGNMENT**

	1	2	3	4	5	6	7	8	9
A	V_{SS}	V_{DDQ}	SA	$\overline{SE1}$	SE2	NC	SA	V_{DDQ}	V_{SS}
B	DQa	DQa	SA	$\overline{SE3}$	NC	NU/V_{DD}	SA	DQb	DQb
C	V_{SS}	V_{DDQ}	V_{SS}	NU/V_{SS}	$\overline{W}$	$\overline{RESET}$	V_{SS}	V_{DDQ}	V_{SS}
D	DQa	DQa	DQa	V_{DD}	$\overline{ADS}$	V_{DD}	DQb	DQb	DQb
E	V_{SS}	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	V_{SS}
F	DQa	DQa	V_{DDI}	V_{DD}	K	V_{DD}	V_{DDI}	DQb	DQb
G	V_{SS}	V_{DDQ}	V_{DD}	V_{SS}	SK	V_{SS}	V_{DD}	V_{DDQ}	V_{SS}
H	DQa	DQa	$\overline{STRBA}$	V_{DD}	V_{SS}	V_{DD}	$\overline{STRBB}$	DQb	DQb
J	V_{SS}	V_{DDQ}	V_{SS}	V_{SS}	NU/V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	V_{SS}
K	DQa	DQa	STRBA	V_{DD}	NC	V_{DD}	STRBB	DQb	DQb
L	V_{SS}	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	V_{SS}
M	DQa	DQa	V_{DDI}	V_{DD}	SA	V_{DD}	V_{DDI}	DQb	DQb
N	V_{SS}	V_{DDQ}	V_{DD}	V_{SS}	SA	V_{SS}	V_{DD}	V_{DDQ}	V_{SS}
P	DQa	DQa	DQa	SA	SA	SA	DQb	DQb	DQb
R	V_{SS}	V_{DDQ}	V_{SS}	SA	SA1	SA	V_{SS}	V_{DDQ}	V_{SS}
T	DQa	DQa	SA	SA	SA0	SA	NC	DQb	DQb
U	V_{SS}	V_{DDQ}	TDI	TMS	TCK	$\overline{TRST}$	TDO	V_{DDQ}	V_{SS}

**153–BUMP PBGA
TOP VIEW**

TQFP
PIN ASSIGNMENT

Top pins (left to right, 100–81):
SA, SA, $\overline{SE1}$, SE2, NU/V$_{SS}$, NU/V$_{SS}$, V$_{DDI}$, SK, $\overline{SE3}$, V$_{DD}$, V$_{SS}$, K, $\overline{W}$, V$_{DDI}$, NC, $\overline{ADS}$, $\overline{RESET}$, NU/V$_{DD}$, SA, SA

Left side (pins 1–30):

Pin	Signal
1	DQa
2	DQa
3	DQa
4	V$_{DDQ}$
5	V$_{SS}$
6	DQa
7	DQa
8	DQa
9	DQa
10	V$_{SS}$
11	V$_{DDQ}$
12	DQa
13	DQa
14	STRBA
15	V$_{DD}$
16	STRBA
17	V$_{SS}$
18	DQa
19	DQa
20	V$_{DDQ}$
21	V$_{SS}$
22	DQa
23	DQa
24	DQa
25	DQa
26	V$_{SS}$
27	V$_{DDQ}$
28	DQa
29	DQa
30	DQa

Right side (pins 80–51):

Pin	Signal
80	DQb
79	DQb
78	DQb
77	V$_{DDQ}$
76	V$_{SS}$
75	DQb
74	DQb
73	DQb
72	DQb
71	V$_{SS}$
70	V$_{DDQ}$
69	DQb
68	DQb
67	V$_{SS}$
66	STRBB
65	V$_{DD}$
64	STRBB
63	DQb
62	DQb
61	V$_{DDQ}$
60	V$_{SS}$
59	DQb
58	DQb
57	DQb
56	DQb
55	V$_{SS}$
54	V$_{DDQ}$
53	DQb
52	DQb
51	DQb

Bottom pins (left to right, 31–50):
NC, SA, SA, SA, SA, SA1, SA0, V$_{DDI}$, NC, V$_{SS}$, V$_{DD}$, NC, V$_{DDI}$, SA, SA, SA, SA, SA, SA, NC

PBGA PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
5D	ADS	Input	Synchronous Address Status: Active low, used to initiate read or write state machines latch in external addresses, or deselect chip.
(a) 1B, 2B, 1D, 2D, 3D, 1F, 2F, 1H, 2H, 1K, 2K, 1M, 2M, 1P, 2P, 3P, 1T, 2T (b) 8B, 9B, 7D, 8D, 9D, 8F, 9F, 8H, 9H, 8K, 9K, 8M, 9M, 7P, 8P, 9P, 8T, 9T	DQx	I/O	Synchronous Data I/O: "x" refers to the word being read or written (I/Os a and b).
5F	K	Input	Clock: This signal registers the address, data in, and all control signals.
6C	RESET	Input	Asynchronous Power–On Reset: Active low at power up, resets internal state machines.
3A, 7A, 3B, 7B, 5M, 5N, 4P, 5P, 6P, 4R, 6R, 3T, 4T, 6T	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
5R, 5T	SA1, SA0	Input	Synchronous Address Inputs: These pins must be wired to the two LSBs of the address bus for proper burst operation. These inputs are registered and must meet setup and hold times.
4A	SE1	Input	Synchronous Chip Enable: Active low to enable chip.
5A	SE2	Input	Synchronous Chip Enable: Active high to enable chip.
4B	SE3	Input	Synchronous Chip Enable: Active low to enable chip.
5G	SK	Input	Data Strobe Clock: 180 degrees out–of–phase with K. Used only with data strobes.
3K	STRBA	Output	Data Strobe: Used in reference to DQa I/Os.
3H	STRBA	Output	Data Strobe: Used in reference to DQa I/Os.
7K	STRBB	Output	Data Strobe: Used in reference to DQb I/Os.
7H	STRBB	Output	Data Strobe: Used in reference to DQb I/Os.
5U	TCK	Input	Boundary Scan Pin, Test Clock: If boundary scan is not used, TCK must be tied to V_{DD} or V_{SS}.
3U	TDI	Input	Boundary Scan Pin, Test Data In.
7U	TDO	Output	Boundary Scan Pin, Test Data Out.
4U	TMS	Input	Boundary Scan Pin, Test Mode Select.
6U	TRST	Input	Boundary Scan Pin, Asynchronous Test Reset. If boundary scan is not used, TRST must be tied to V_{SS}.
5C	W	Input	Synchronous Write.
4D, 6D, 3E, 7E, 4F, 6F, 3G, 7G, 4H, 6H, 4K, 6K, 3L, 7L, 4M, 6M, 3N, 7N	V_{DD}	Supply	Core Power Supply.
3F, 7F, 3M, 7M	V_{DDI}	Supply	Input Power Supply.
2A, 8A, 2C, 8C, 2E, 8E, 2G, 8G, 2J, 8J, 2L, 8L, 2N, 8N, 2R, 8R, 2U, 8U	V_{DDQ}	Supply	I/O Power Supply.
1A, 9A, 1C, 3C, 7C, 9C, 1E, 4E, 5E, 6E, 9E, 1G, 4G, 6G, 9G, 5H, 1J, 3J, 4J, 6J, 7J, 9J, 1L, 4L, 5L, 6L, 9L, 1N, 4N, 6N, 9N, 1R, 3R, 7R, 9R, 1U, 9U	V_{SS}	Supply	Ground.
6A, 5B, 5K, 7T	NC	—	No Connection: There is no connection to the chip.
6B	NU/V_{DD}	—	Not Usable: There is an internal connection to the chip. This pin may be left unconnected or tied to V_{DD}.
4C, 5J	NU/V_{SS}	—	Not Usable: There is an internal connection to the chip. This pin may be left unconnected or tied to V_{SS}.

TQFP PIN DESCRIPTIONS

| Pin Locations	Symbol	Type	Description
85	ADS	Input	Synchronous Address Status: Active low, used to initiate read or write state machines latch in external addresses, or deselect chip.
(a) 1, 2, 3, 6, 7, 8, 9, 12, 13, 18, 19, 22, 23, 24, 25, 28, 29, 30 (b) 51, 52, 53, 56, 57, 58, 59, 62, 63, 68, 69, 72, 73, 74, 75, 78, 79, 80	DQx	I/O	Synchronous Data I/O: "x" refers to the word being read or written (I/Os a and b).
89	K	Input	Clock: This signal registers the address, data in, and all control signals.
84	RESET	Input	Asynchronous Power–On Reset: Active low at power up, resets internal state machines.
32, 33, 34, 35, 44, 45, 46, 47, 48, 49, 81, 82, 99, 100	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
36, 37	SA1, SA0	Input	Synchronous Address Inputs: These pins must be wired to the two LSBs of the address bus for proper burst operation. These inputs are registered and must meet setup and hold times.
98	SE1	Input	Synchronous Chip Enable: Active low to enable chip.
97	SE2	Input	Synchronous Chip Enable: Active high to enable chip.
92	SE3	Input	Synchronous Chip Enable: Active low to enable chip.
93	SK	Input	Data Strobe Clock: 180 degrees out–of–phase with K. Used only with data strobes.
16	STRBA	Output	Data Strobe: Used in reference to DQa I/Os.
14	STRBA	Output	Data Strobe: Used in reference to DQa I/Os.
64	STRBB	Output	Data Strobe: Used in reference to DQb I/Os.
66	STRBB	Output	Data Strobe: Used in reference to DQb I/Os.
88	W	Input	Synchronous Write.
15, 41, 65, 91	V_{DD}	Supply	Core Power Supply.
38, 43, 87, 94	V_{DDI}	Supply	Input Power Supply.
4, 11, 20, 27, 54, 61, 70, 77	V_{DDQ}	Supply	I/O Power Supply.
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	Supply	Ground.
31, 39, 42, 50, 86	NC	—	No Connection: There is no connection to the chip.
83	NU/V_{DD}	—	Not Usable: There is an internal connection to the chip. This pin may be left unconnected or tied to V_{DD}.
95, 96	NU/V_{SS}	—	Not Usable: There is an internal connection to the chip. This pin may be left unconnected or tied to V_{SS}.

TRUTH TABLE (See Notes 1 and 2)

K	E	ADS	W	Next Cycle (n)	Input Command Code	DQ (n + 1)	DQ (n+2)
L – H	False	0	X	Deselect	D	High–Z	—
L – H	True	0	0	Load Address, Begin Write	BW	Data In	—
L – H	True	0	1	Load Address, Begin Read	BR	—	Data Out
L – H	X	1	0	Continue Write	CW	Data In	—
L – H	X	1	1	Continue Read Mask Write	CR MW	— High–Z	Data Out —

NOTES:
   1. X = don't care, 1 = logic high, 0 = logic low.
   2. E = true if SE1 and SE3 = 0, and SE2 = 1.

BURST ADDRESS TABLE

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X00	X . . . X11	X . . . X10
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X10	X . . . X01	X . . . X00
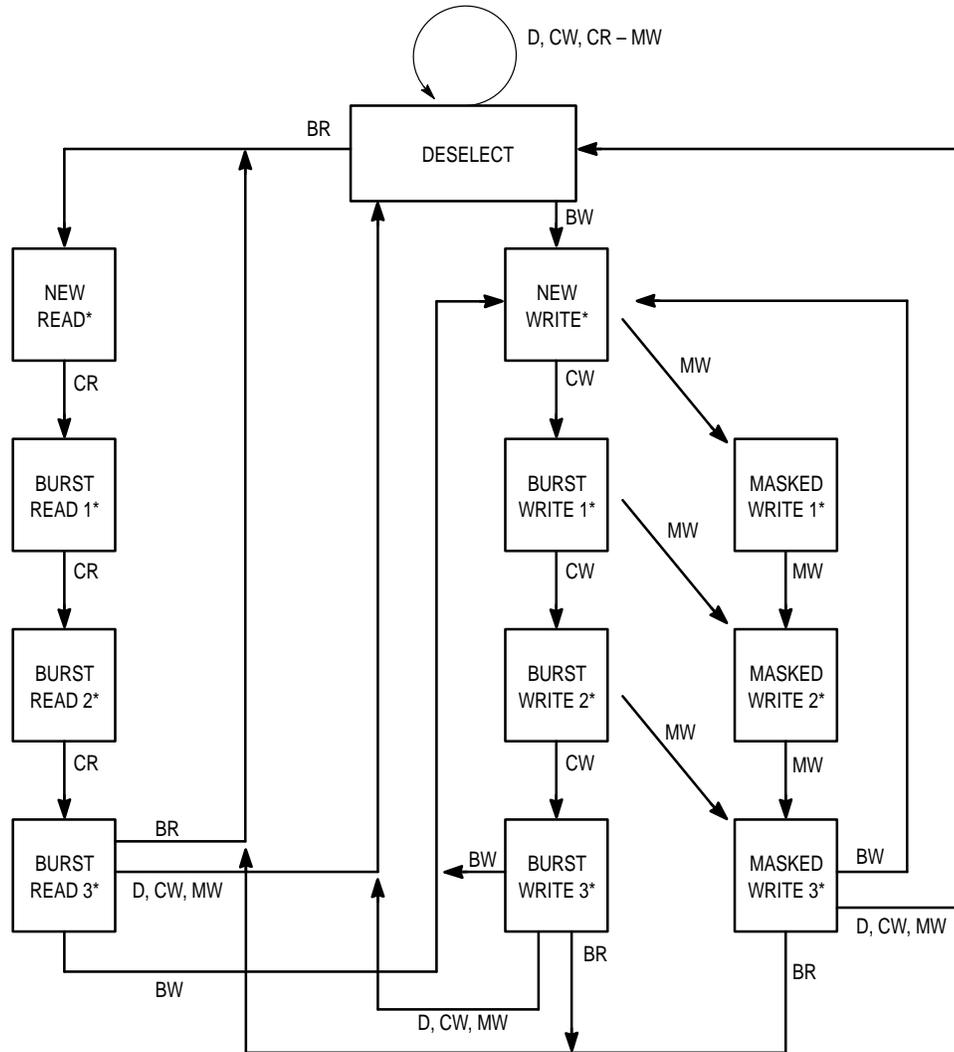
* Command code inputs not shown from this state are not valid.

Figure 1. Functional State Diagram

Figure 2. Data I/O State Diagram

D, CW, CR – MW

HIGH–Z[4]

BR   BW

INTERMEDIATE HIGH–Z[1, 4]

DATA–IN (1)/ HIGH–Z[1, 4]   MW

CR   CW

INTERMEDIATE HIGH–Z[1, 4]

MASK (2)/ HIGH–Z[1, 4]

DATA–IN (2)/ HIGH–Z[1, 4]   MW   MW

CR   CW

DATA–OUT/ Q(1)VALID[1, 2]

MASK (3)/ HIGH–Z[1, 4]

DATA–IN (3)/ HIGH–Z[1, 4]   MW   MW

CR   CW

DATA–OUT/ Q(2)VALID[1, 3]

MASK (4)/ HIGH–Z[1, 4]

DATA–IN (4)/ HIGH–Z[1, 4]

CR   CW

DATA–OUT/ Q(3)VALID[1, 2]   CR

HIGH–Z[1, 4]   MW

CW, MW

BR   MW

CR   DATA–OUT/ Q(4)VALID[1, 3]

DATA–OUT/ Q(4)VALID[1, 3]   BR

HIGH–Z[1, 4]

CW, MW

D, CW, CR

NOTES:
1. Command code inputs not shown from this state are not valid.
2. STRBA and STRBB transition from logic 1 to 0. STRBA and STRBB transition from logic 0 to 1.
3. STRBA and STRBB transition from logic 0 to 1. STRBA and STRBB transition from logic 1 to 0.
4. Data strobes are driven to High–Z.

Figure 2. Data I/O State Diagram

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit	Notes
Power Supply Voltage	V_{DD}	V_{SS} – 0.5 to + 4.0	V	
I/O Supply Voltage	V_{DDQ}	V_{SS} – 0.5 to 2.5	V	2, 3
Input Supply Voltage	V_{DDI}	V_{SS} – 0.5 to 2.5	V	2, 3
Voltage Relative to V_{SS} for Any Pin Except V_{DD}	V_{in}	V_{SS} – 0.5 to V_{DDI} + 0.5	V	2, 4
Input Voltage (Three–State I/O)	V_{IT}	V_{SS} – 0.5 to V_{DDQ} + 0.5	V	2, 4
Output Current (per I/O)	I_{out}	± 20	mA	
Package Power Dissipation	P_D	2.75	W	5
Temperature Under Bias	T_{bias}	– 10 to 85	°C	
Storage Temperature	T_{stg}	– 55 to 125	°C	

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPER- ATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. This is a steady–state DC parameter that is in effect after the power supply has achieved its nominal operating level. Power sequencing is not necessary.
3. V_{DDI} = V_{DDQ}.
4. Max V_{in} and V_{IT} are not to exceed Max V_{DD}.
5. Power dissipation capability is dependent upon package characteristics and use environment. See Package Thermal Characteristics.

This device contains circuitry to protect the inputs against damage due to high static volt- ages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maxi- mum rated voltages to this high–impedance circuit.

PACKAGE THERMAL CHARACTERISTICS — PBGA

Rating	Symbol	Max	Unit	Notes
Junction to Ambient (@ 200 lfm)	$R_{\theta JA}$	25	°C/W	1, 2
Junction to Board (Bottom)	$R_{\theta JB}$	12	°C/W	3
Junction to Case (Top)	$R_{\theta JC}$	10	°C/W	4

PACKAGE THERMAL CHARACTERISTICS — TQFP

Rating	Symbol	Max	Unit	Notes
Junction to Ambient (@ 200 lfm)	$R_{\theta JA}$	25	°C/W	1, 2
Junction to Board (Bottom)	$R_{\theta JB}$	17	°C/W	3
Junction to Case (Top)	$R_{\theta JC}$	9	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V ± 200 mV, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS AND DC CHARACTERISTICS (Voltage Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.1	3.3	3.5	V
Input Supply Voltage	V_{DDI}	1.8	—	2.2	V
I/O Supply Voltage	V_{DDQ}	1.8	—	2.2	V
Input Low Voltage (V_{DDI} = V_{DDQ})	V_{IL}	− 0.5	—	0.35 x V_{DDI}	V
Input High Voltage (V_{DDI} = V_{DDQ})	V_{IH}	0.65 x V_{DDI}	—	V_{DDI} + 0.5	V
Input Leakage Current (0 V ≤ V_{in} ≤ V_{DD})	$I_{lkg(I)}$	—	—	± 1	μA
Output Leakage Current (0 V ≤ V_{in} ≤ V_{DDQ})	$I_{lkg(O)}$	—	—	± 1	μA
Output Low Voltage (I_{OL} = 1 mA)	V_{OL}	− 0.5	—	0.4	V
Output High Voltage (I_{OL} = − 1 mA)	V_{OH}	V_{DDQ} − 0.4	—	V_{DDQ} + 0.5	V
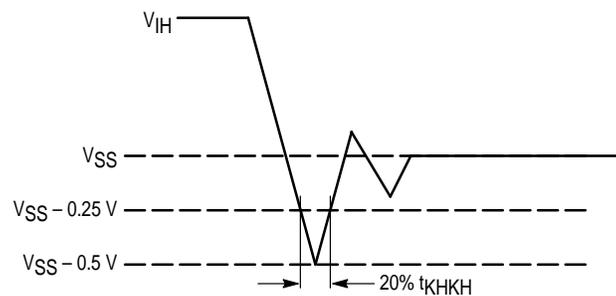
Figure 3. Undershoot Voltage

SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit	Notes
AC Supply Current (Device Selected, All Outputs Open, Freq = Max, V_{DD} = Max)	I_{DDA} − 250 I_{DDA} − 225 I_{DDA} − 200	—	TBD	mA	1, 2, 3, 4
Input and I/O Supply Current – Desktop (All 40 Outputs Toggling, Freq = Max, V_{DDI} = Max, V_{DDQ} = Max, V_{DDI} = V_{DDQ}, C_{dt} = 24 pF)	I_{DDQ} − 250 I_{DDQ} − 225 I_{DDQ} − 200	—	311 280 249	mA	2, 5
Static Standby Supply Current (Device Deselected, Freq = Max, V_{DD} = Max, ADS ≥ (V_{DDI} − 0.2 V), W Static ≤ (V_{SS} + 0.2 V) or ≥ (V_{DDI} − 0.2 V), SA and DQx Inputs Static ≤ (V_{SS} + 0.2 V), Outputs Disabled)	I_{SB1} − 250 I_{SB1} − 225 I_{SB1} − 200	—	63 57 50	mA	1, 2, 4
Idle Standby Supply Current (Device Deselected, Freq = 0, V_{DD} = Max, ADS ≥ (V_{DDI} − 0.2 V), W Static ≤ (V_{SS} + 0.2 V) or ≥ (V_{DDI} − 0.2 V), SA and DQx Inputs Static ≤ (V_{SS} + 0.2 V), Outputs Disabled)	I_{SB2A}	—	TBD	mA	1, 3, 4
Idle Input Standby Supply Current (Device Deselected, Freq = 0, V_{DD} = Max, ADS ≥ (V_{DDI} − 0.2 V), W Static ≤ (V_{SS} + 0.2 V) or ≥ (V_{DDI} − 0.2 V), SA and DQx Inputs Static ≤ (V_{SS} + 0.2 V), Outputs Disabled)	I_{SB2B}	—	TBD	mA	1, 3, 5

NOTES:
1. Device is selected and deselected as defined by the Truth Table.
2. Reference AC Operating Conditions and Characteristics for input and timing.
3. Data states are all zero.
4. Includes supply current for V_{DD} only.
5. Includes supply currents for V_{DDI} and V_{DDQ} only.

CAPACITANCE AND INDUCTANCE (See Notes 1, 2, and 3)

	TQFP				PBGA			
	Capacitance (pF)		Inductance (nH)		Capacitance (pF)		Inductance (nH)	
Pin Description	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
I/O Pins	5	7	2	10	5.5	7.5	2.5	4.5
Data Strobe Pins	5	7	2	10	5.5	7.5	2.5	4.5
Input Pins	3	5	2	10	3.5	5.5	2.5	4
ADS Pin	5	7	2	10	5.5	7.5	2.5	4.5
K and SK Pins	3.5	4.5	2	10	4	5	1.5	3
TCK Boundary Scan Pin	—	—	—	—	—	5	—	—
Boundary Scan Input Pins	—	—	—	—	—	8	—	—
TDO Boundary Scan Pin	—	—	—	—	—	8	—	—

NOTES:
1. Parameters are periodically sampled rather than 100% tested.
2. Capacitance variation part to part on the same pin is $\pm$ 0.25 pF.
3. Inductance variation part to part on the same pin is $\pm$ 1 nH.

AC OPERATING CONDITIONS AND CHARACTERISTICS
(V_{DD} = 3.3 V $\pm$ 200 mV, Unless Otherwise Noted)

AC TEST CONDITIONS

Parameter	Value	Unit
Input Timing Reference Level	V_{DDQ}/2	V
Input Pulse Levels	0 to 2.0	V
Input Rise/Fall Time (20 to 80%)	1	V/ns
Output Timing Reference Level	V_{DDQ}/2	V
Die Temperature $\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad T_J$–250 T_J–225 T_J–200	115 115 115	°C
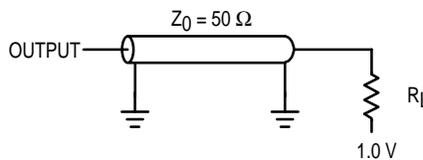
Figure 4. AC Output Test Load

(TBD)

Figure 5. Lumped Capacitive Load and Typical Derating Curve

READ/WRITE CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM63P636–250 Min	MCM63P636–250 Max	MCM63P636–225 Min	MCM63P636–225 Max	MCM63P636–200 Min	MCM63P636–200 Max	Unit	Notes
Clock Cycle Time	t_{KHKH}	4	—	4.4	—	5	—	ns	3, 4
Clock High Time	t_{KH}	1.06	—	1.24	—	1.46	—	ns	4
Clock Low Time	t_{KL}	1.06	—	1.24	—	1.46	—	ns	4
Strobe Clock Cycle Time	t_{SKHSKH}	4	—	4.4	—	5	—	ns	3, 4
Strobe Clock High Time	t_{SKH}	1.06	—	1.24	—	1.46	—	ns	4
Strobe Clock Low Time	t_{SKL}	1.06	—	1.24	—	1.46	—	ns	4
Rising K to Rising SK	t_{KHSKH}	1.6	2.4	1.8	2.6	2.1	2.9		3
Clock Access Time	t_{KHQV}	—	3.9	—	4.3	—	4.9	ns	3
Clock to Output Low–Z	t_{KHQX}	0	—	0	—	0	—	ns	5, 6
Clock to Output High–Z	t_{KHQZ}	—	3.9	—	4.3	—	4.9	ns	5, 6
Strobe Clock Access Time	t_{SKHSTV}	—	3.9	—	4.3	—	4.9	ns	3
Setup Times: Address ADS Chip Enable Data In Data Out Write	t_{AVKH} t_{SVKH} t_{EVKH} t_{DVKH} t_{QVSTV} t_{WVKH}	0.5 1.2 0.5 1.2 1 1.2	— 	0.5 1.5 0.5 1.5 1.1 1.5	— 	0.5 1.5 0.5 1.5 1.15 1.5	— 	ns	3
Hold Times: Address ADS Chip Enable Data In Data Out Write	t_{KHAX} t_{KHSX} t_{KHEX} t_{KHDX} t_{STVQX} t_{KHWX}	4 0.5 4 0.5 1 0.5	— 	4.4 0.5 4.4 0.5 1.1 0.5	— 	5 0.5 5 0.5 1.15 0.5	— 	ns	3

NOTES:
1. Reads and writes are as defined in the Truth Table.
2. All read and write cycle timings are referenced from K, SK, or data strobes.
3. In order to reduce test correlation issues and to reduce the effects of application specific input edge rate variations on correlation between data sheet parameters and actual system performance, FSRAM AC parametric specifications are always specified at $V_{DDQ}/2$. In some design exercises, it is desirable to evaluate timing using other reference levels. Since the maximum test input edge rate is known and is given in the AC Test Conditions section of the data sheet as 1 V/ns, one can easily interpolate timing values to other reference levels.
4. Refer to Figure 5 for input reference levels.
5. This parameter is sampled and not 100% tested.
6. Measured at $\pm$ 200 mV from steady state.
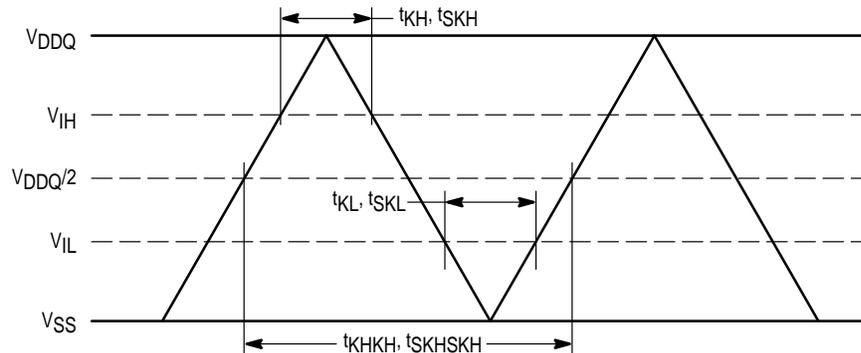
Figure 6. AC Timing Diagram Clock Reference

PULL–UP		
VOLTAGE (V)	I (mA) MIN	I (mA) MAX
– 0.5	– 32	– 72
0	– 32	– 72
0.2	– 32	– 72
0.4	– 28	– 72
0.6	– 24	– 64
0.8	– 20	– 56
1	– 16	– 48
1.2	– 12	– 40
1.4	– 8	– 32
1.6	– 4	– 24
1.8	0	– 16
2	4	– 8
2.2	8	0
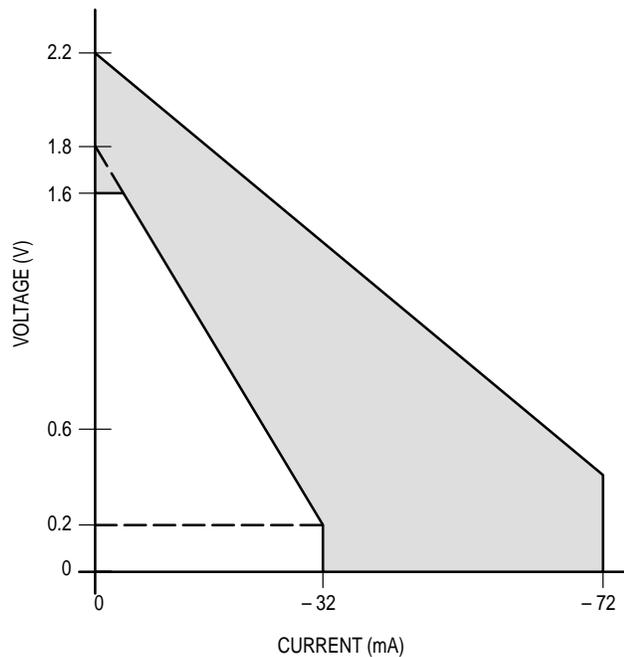
(a) Pull–Up

PULL–UP		
VOLTAGE (V)	I (mA) MIN	I (mA) MAX
– 0.5	– 10	– 20
0	0	0
0.2	4	8
0.4	8	16
0.6	12	24
0.8	16	32
1	20	40
1.2	24	48
1.4	28	56
1.6	28	64
1.8	28	72
2	28	72
2.2	28	72
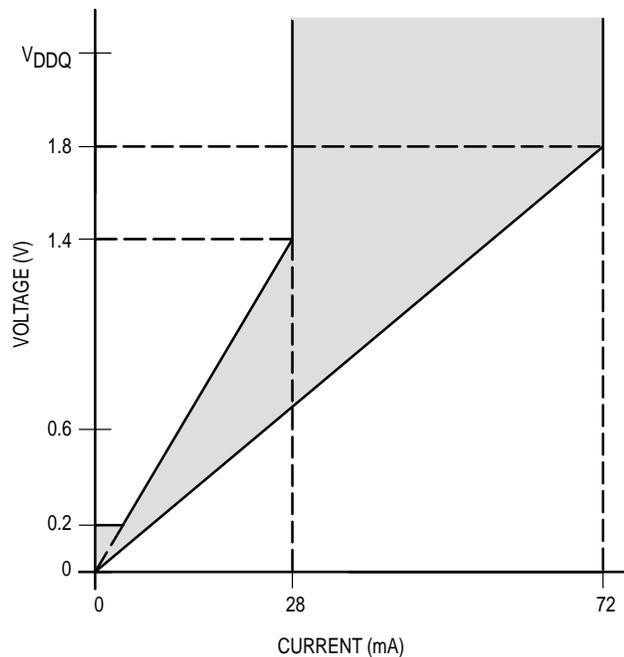
(b) Pull–Down

Figure 7. Typical Output Buffer Characteristics – PBGA Only

PULL–UP		
VOLTAGE (V)	I (mA) MIN	I (mA) MAX
− 0.5	− 23	− 60
0	− 23	− 60
0.2	− 23	− 60
0.4	− 20	− 60
0.6	− 17	− 53
0.8	− 14	− 47
1	− 11	− 40
1.2	− 9	− 33
1.4	− 6	− 27
1.6	− 3	− 20
1.8	0	− 13
2	3	− 7
2.2	6	0
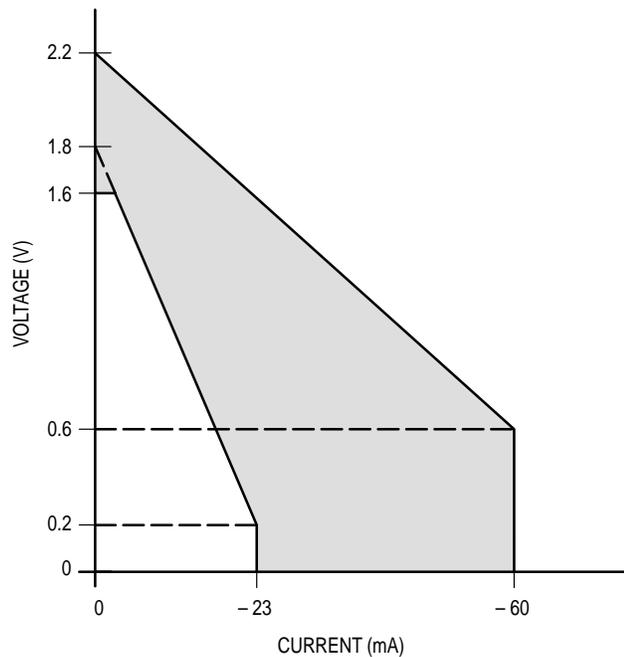
(a) Pull–Up

PULL–UP		
VOLTAGE (V)	I (mA) MIN	I (mA) MAX
− 0.5	− 7	− 17
0	0	0
0.2	3	7
0.4	6	13
0.6	9	20
0.8	11	27
1	14	33
1.2	17	40
1.4	20	47
1.6	20	53
1.8	20	60
2	20	60
2.2	20	60
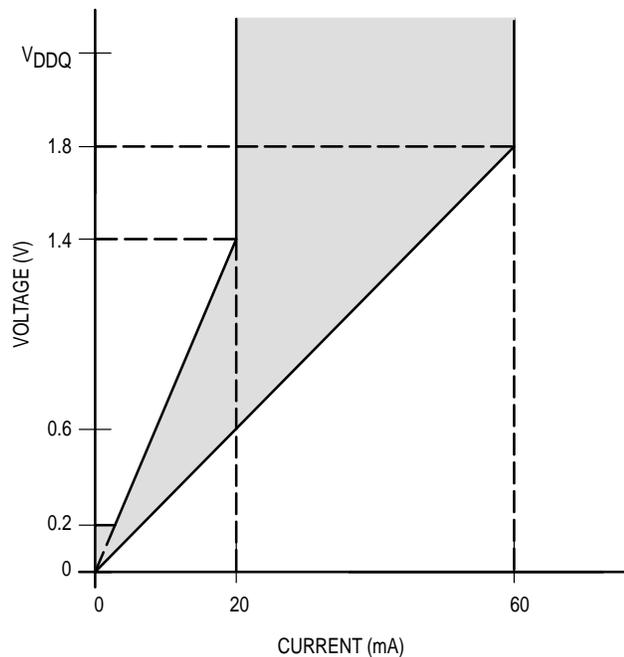
(b) Pull–Down

Figure 8. Typical Output Buffer Characteristics – TQFP Only

READ CYCLES

Waveform signals (top to bottom): K, SA, $\overline{\text{ADS}}$, $\overline{\text{W}}$, $\overline{\text{E}}$, DQx, SK, STRBA/B, $\overline{\text{STRBA/B}}$

Timing parameters shown: t_{AVKH}, t_{KHAX}, t_{SVKH}, t_{KHSX}, t_{WVKH}, t_{KHWX}, t_{EVKH}, t_{KHEX}, t_{KHQX}, t_{KHQV}, t_{KHQZ}, t_{SKHSTV}, t_{QVSTV}, t_{STVQX}

Data signals: Q(A), Q(A+1), Q(A + 2), Q(A + 3), Q(B), Q(B + 1), Q(B + 2), Q(B + 3)

Address signals: A, B
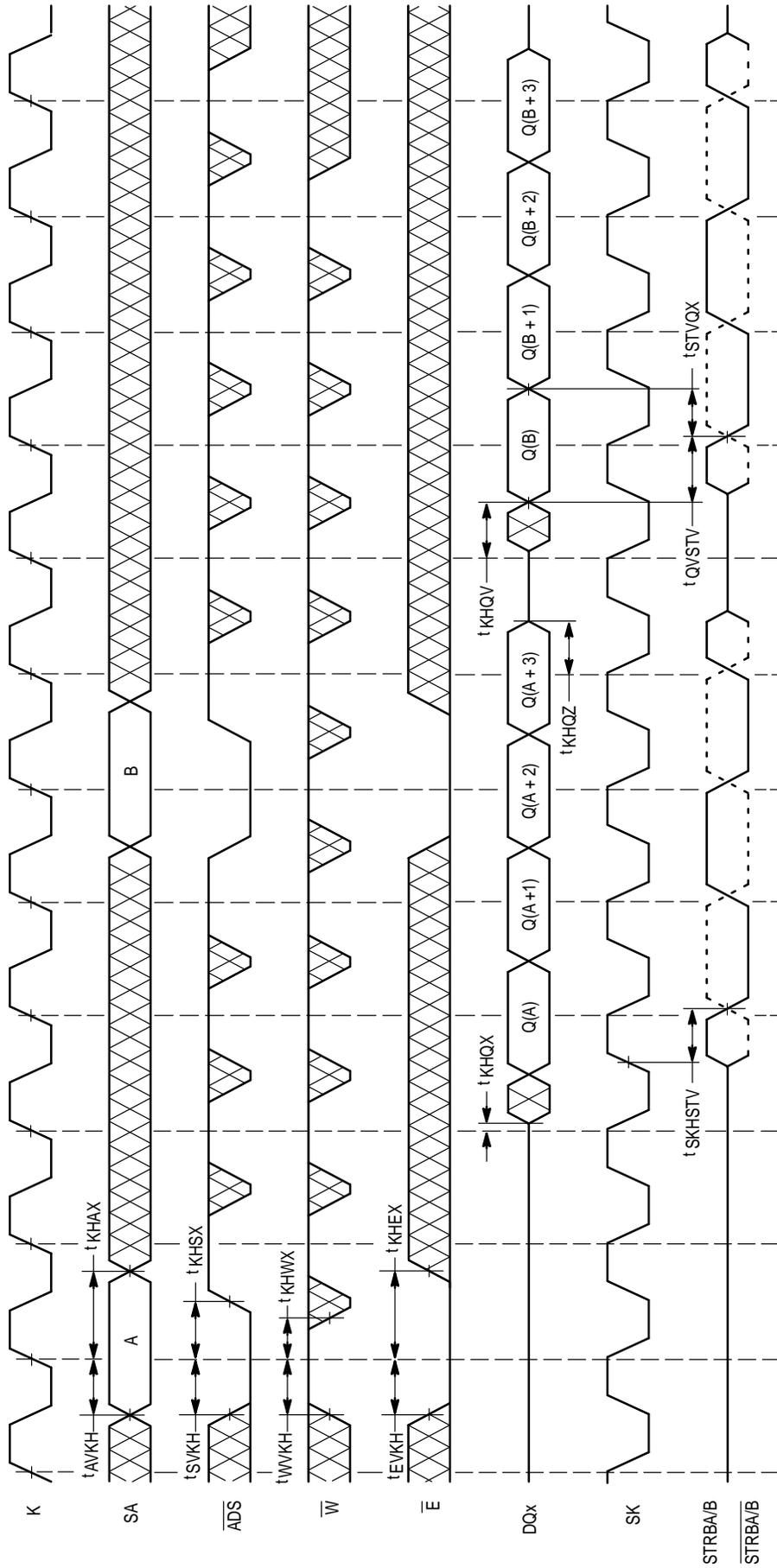
NOTE: $\overline{\text{E}}$ low = $\overline{\text{SE1}}$ and $\overline{\text{SE3}}$ low and SE2 high.

WRITE CYCLES

Signal labels (top to bottom): K, SA, $\overline{ADS}$, $\overline{W}$, $\overline{E}$, DQx, SK, STRBA/B, $\overline{STRBA/B}$

Data values: D(A), D(A + 1), D(A + 2), D(A + 3), D(B), D(B + 1)

Address values: A, B

Timing parameters: t_{DVKH}, t_{KHDX}, t_{KHSKH}

HIGH–Z

READ/WRITE CYCLES

Timing diagram signals (top to bottom): K, SA, $\overline{ADS}$, $\overline{W}$, $\overline{E}$, DQx, SK, STRBA/B, $\overline{STRBA/B}$

SA values: A, B, C

DQx values: Q(A), Q(A+1), Q(A+2), Q(A+3), D(B), D(B+1), D(B+2), D(B+3), Q(C), Q(C+1), Q(C+2), Q(C+3)

Cycle labels: BURST READ, BURST WRITE, BURST READ, DESELECT
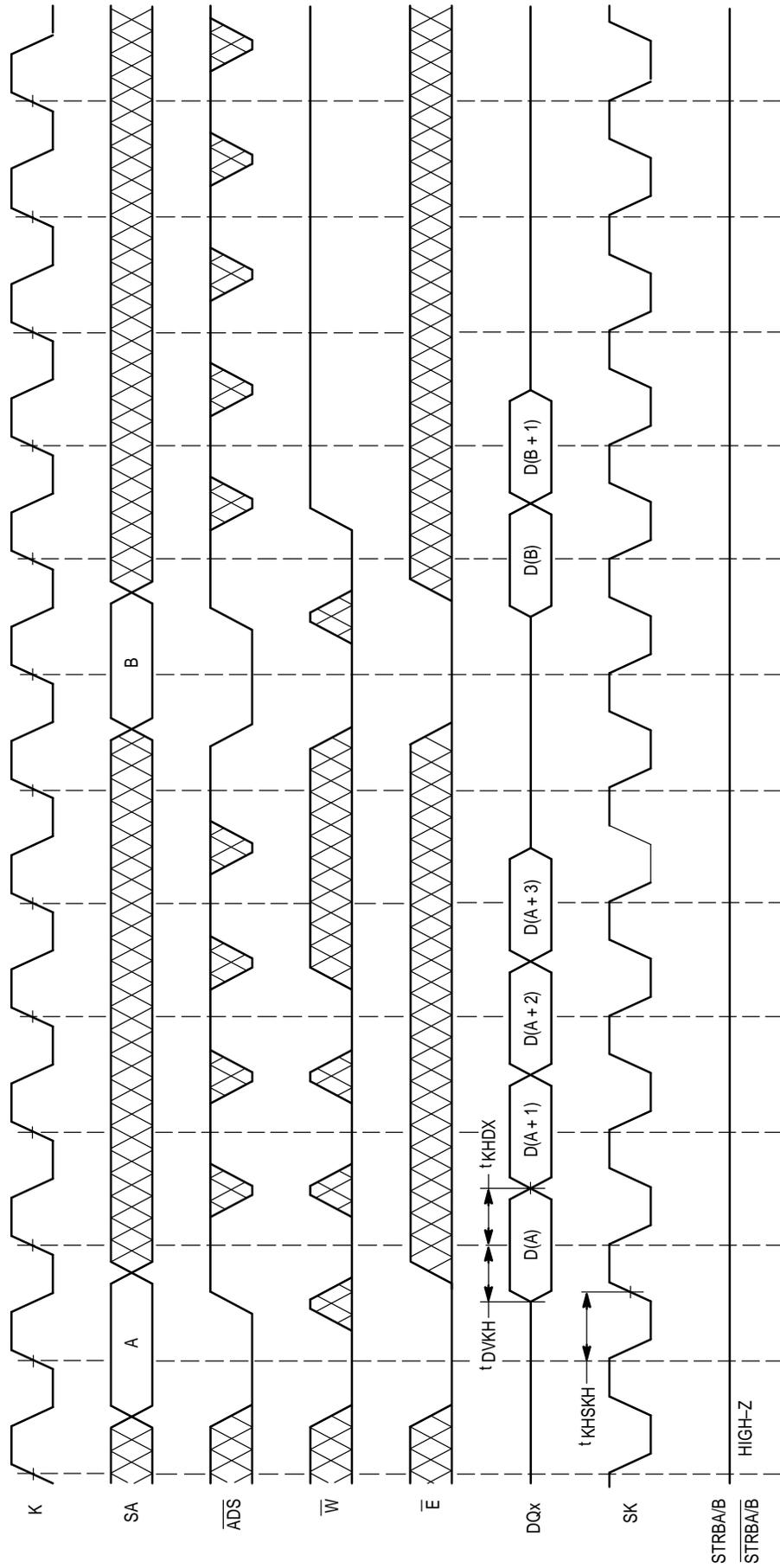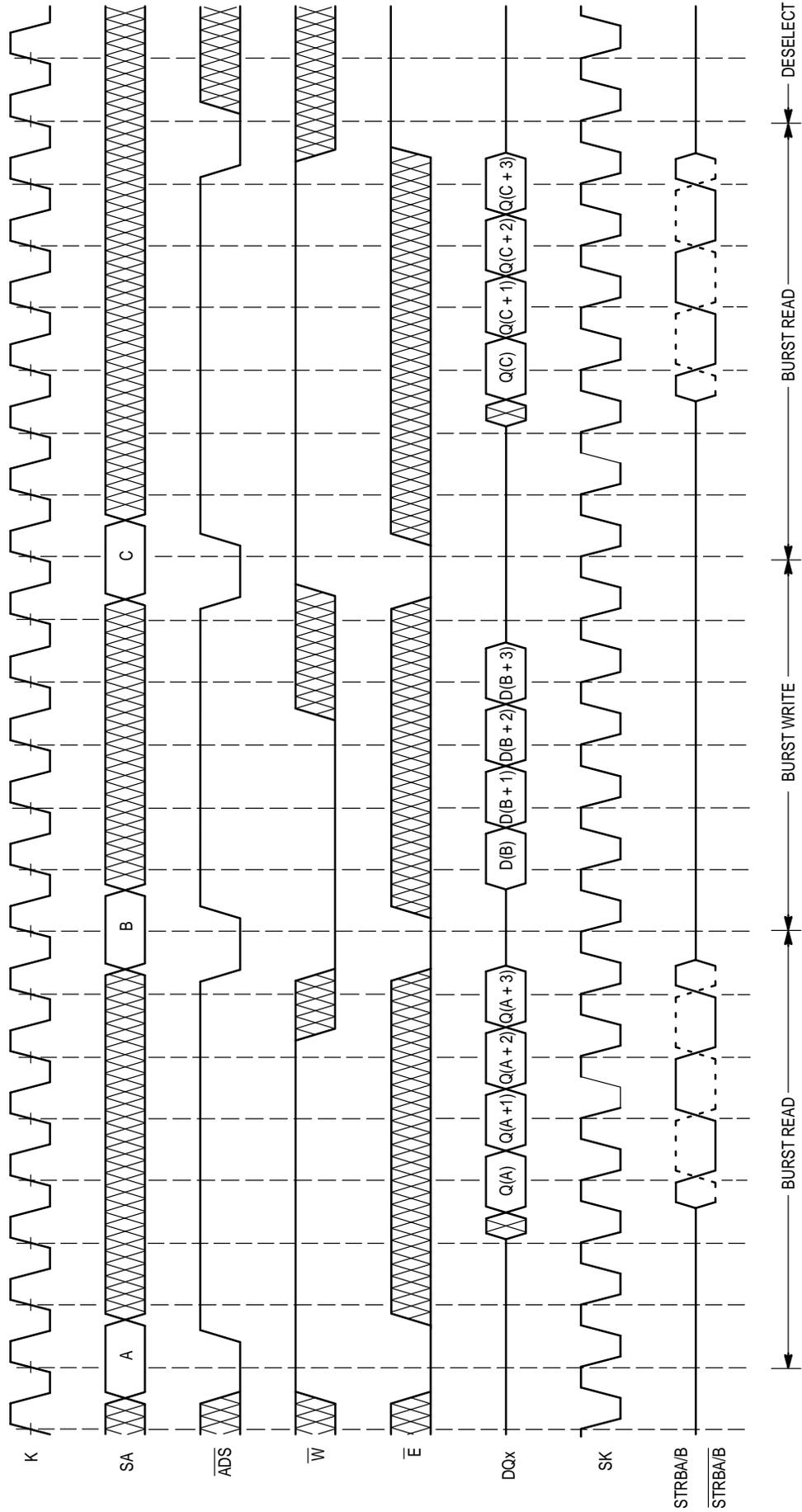
FUNCTIONAL OPERATION

POWER UP AND INITIALIZATION

The $\overline{\text{RESET}}$ input is used to reset the SRAM internal logic at power on. At power on, this pin is held low and then driven high at some later time. Eight cycles after the RESET is asserted high, standard SRAM functionality may begin.

DATA STROBES

The data strobes STRBA, $\overline{\text{STRBA}}$, STRBB, and $\overline{\text{STRBB}}$ are driven by the SRAM to be used by the device receiving the output data. The data strobes toggle only at the approximate center of each output data valid window such that the external device can reliably latch in this data. Following a burst read, the data strobes will be driven to High–Z.

WRITE CYCLES

The address is sampled on the first rising edge of clock of each burst write sequence, and the write data is sampled on the subsequent rising clock edges. During a burst write the last, last two, or last three addresses may be blocked from being written by asserting the W synchronous write pin high. However, once W is asserted high, it must remain in this state through the remainder of the burst write sequence. All

burst write (and masked write) sequences must be followed by an inactive cycle to reset internal state machines.

LOW POWER STOP–CLOCK OPERATION

In the stop–clock mode of operation, the SRAM will hold all state and data values even though the clock is not running (full static operation). The SRAM design allows the clock to start with ADS, and stops the clock after the last write data is latched, or the last read data is driven out.

When starting and stopping the clock, the initial clocks being driven may not meet the AC clock timing parametrics, but will meet those parametrics at least two clocks prior to ADS being asserted low.

To achieve the lowest power operation for all three stop clock modes, stop read, stop write, and stop deselect:

- Force the clock to a low state.

- Force the control signals to an inactive state (this guarantees any potential source of noise on the clock input will not start an unplanned on activity).

- Force the address inputs to a low state (V_{IL}), preferably < 0.2 V.

STOP–CLOCK WITH READ TIMING
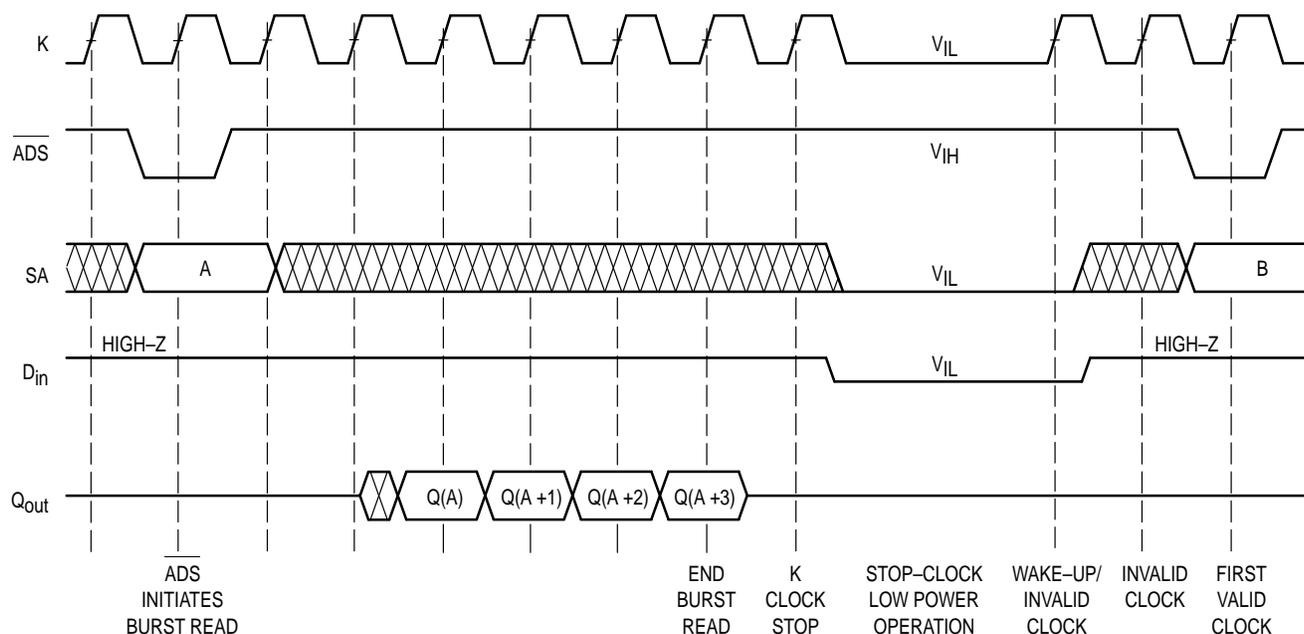
STOP–CLOCK WITH WRITE TIMING

K   V_{IL}

$\overline{ADS}$ V_{IH}

SA   A   V_{IL}   B

$\overline{W}$ V_{IH}

D$_{in}$ D(A)   D(A +1)   D(A +2)   D(A +3)   V_{IL}   HIGH–Z

Q$_{out}$ HIGH–Z

$\overline{ADS}$ INITIATES BURST WRITE   END BURST WRITE   K CLOCK STOP   STOP–CLOCK LOW POWER OPERATION   WAKE–UP/ INVALID CLOCK   INVALID CLOCK   FIRST VALID CLOCK
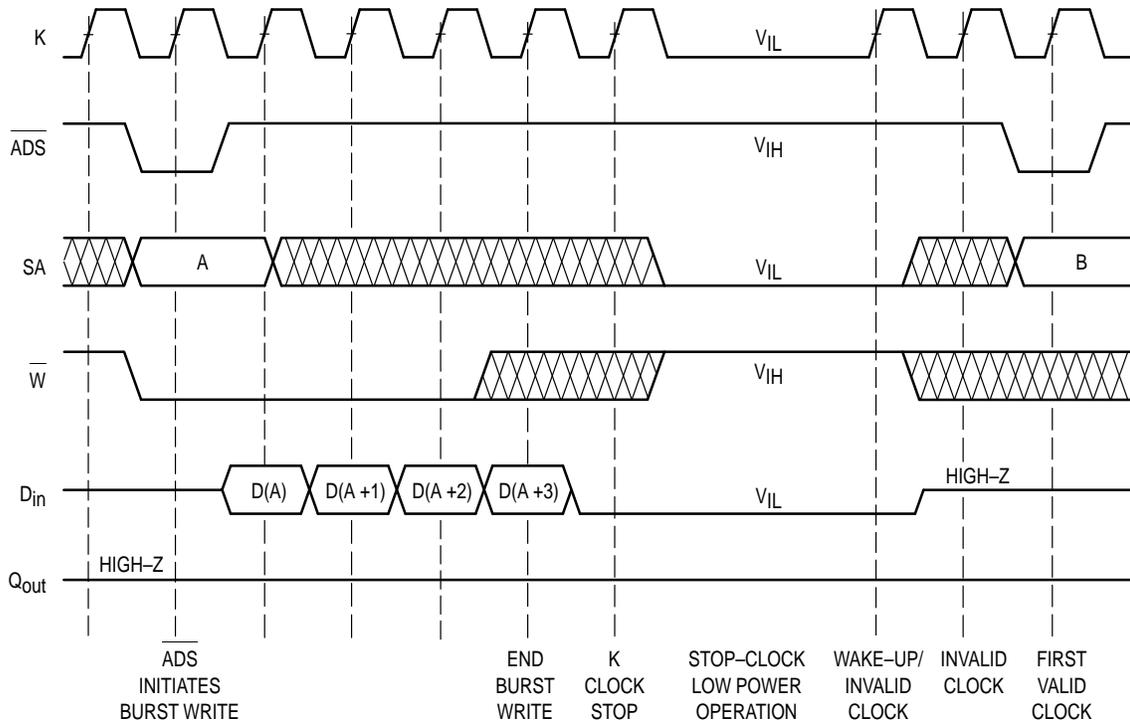
STOP–CLOCK WITH DESELECT TIMING

K   V_{IL}

$\overline{ADS}$ V_{IH}

SA   V_{IL}   A

$\overline{E}$

D$_{in}$ HIGH–Z   V_{IL}

Q$_{out}$ Q(3)   Q(4)

CONTINUE BURST READ   END READ/ DESELECT   K CLOCK STOP   STOP–CLOCK LOW POWER OPERATION   WAKE–UP/ INVALID CLOCK   INVALID CLOCK   FIRST VALID CLOCK
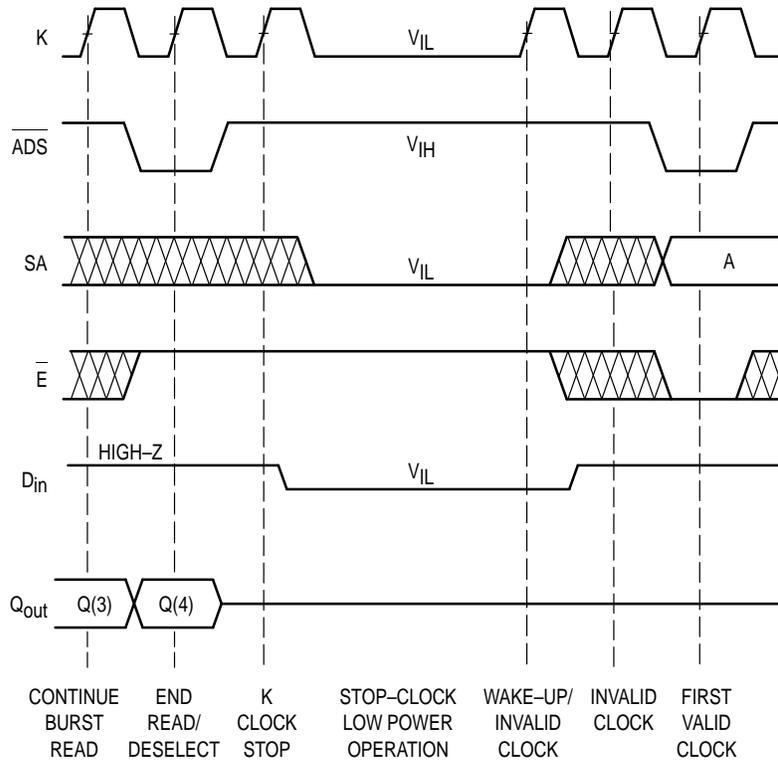
SERIAL BOUNDARY SCAN TEST ACCESS PORT OPERATION

OVERVIEW

The serial boundary scan test access port (TAP) on this RAM is designed to operate in a manner consistent with IEEE Standard 1149.1–1990 (commonly referred to as JTAG), but does not implement all of the functions required for IEEE 1149.1 compliance. Certain functions have been modified or eliminated because their implementation places extra delays in the RAMs critical speed path. Nevertheless, the RAM supports the standard TAP controller architecture (the TAP controller is the state machine that controls the TAPs operation) and can be expected to function in a manner that does not conflict with the operation of devices with IEEE Standard 1149.1 compliant TAPs. The TAP operates using a 2.5 V tolerant logic level signaling.

DISABLING THE TEST ACCESS PORT

It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfering with normal operation of the device, TRST should be tied low and TCK, TDI, and TMS should be pulled through a resistor to 2.0 V. TDO should be left unconnected.

TAP DC OPERATING CHARACTERISTICS
(T_A = 0 to 70°C, Unless Otherwise Noted)

Parameter	Symbol	Min	Max	Unit	Notes
Input Logic Low	$V_{IL}1$	-0.5	$0.35 \times V_{DDQ}$	V	
Input Logic High	$V_{IH}1$	$0.65 \times V_{DDQ}$	2.5	V	
Input Leakage Current	I_{lkg}	—	± 10	µA	1
Output Logic Low	$V_{OL}1$	$V_{SS} - 0.5$	0.4	V	2
Output Logic High	$V_{OH}1$	$V_{DDQ} - 0.4$	$V_{DDQ} + 0.5$	V	

NOTES:
1. $0\ V \leq V_{in} \leq V_{DDQ}$ for all logic input pins.
2. For V_{OL} = 0.4 V, 14 mA $\leq I_{OL} \leq$ 28 mA.

TAP AC OPERATING CONDITIONS AND CHARACTERISTICS

(T_A = 0 to 70°C, Unless Otherwise Noted)

AC TEST CONDITIONS

Parameter	Value	Unit
Input Timing Reference Level	$V_{DDQ}/2$	V
Input Pulse Levels	0 to 2.0	V
Input Rise/Fall Time (20 to 80%)	1	V/ns
Output Timing Reference Level	$V_{DDQ}/2$	V
Output Load (See Figure 4 Unless Otherwise Noted)	—	—

TAP CONTROLLER TIMING

Parameter		Symbol	Min	Max	Unit	Notes
TCK Cycle Time		t_{THTH}	60	—	ns	
TCK Clock High Time		t_{TH}	25	—	ns	
TCK Clock Low Time		t_{TL}	25	—	ns	
TDO Access Time		t_{TLQV}	1	10	ns	
TRST Pulse Width		t_{TSRT}	40	—	ns	
Setup Times	Capture TDI TMS	t_{CS} t_{DVTH} t_{MVTH}	5 5 5	—	ns	1
Hold Times	Capture TDI TMS	t_{CH} t_{THDX} t_{THMX}	13 14 14	—	ns	1

NOTE:
1. t_{CS} and t_{CH} define the minimum pauses in RAM I/O transitions to assure accurate pad data capture.

TAP CONTROLLER TIMING DIAGRAM
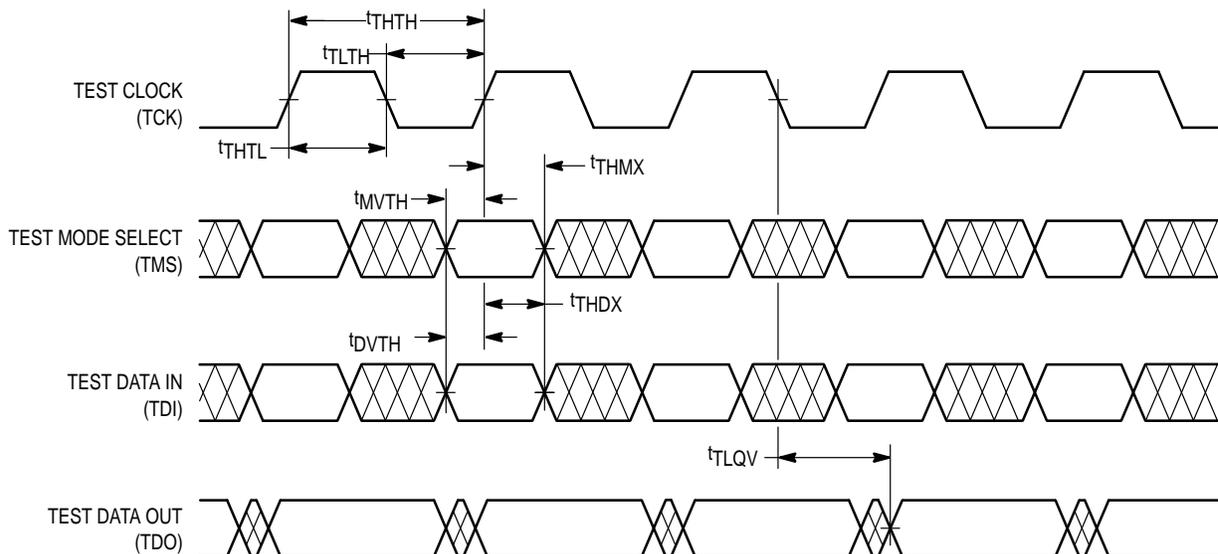
Boundary Scan Order

Bit No.	Signal Name	Bump ID		Bit No.	Signal Name	Bump ID
1	DQa	3D		34	DQb	7P
2	DQa	1B		35	DQb	8T
3	DQa	2B		36	DQb	9T
4	DQa	1D		37	DQb	9P
5	DQa	2D		38	DQb	8P
6	DQa	1F		39	DQb	9M
7	DQa	2F		40	DQb	8M
8	DQa	1H		41	DQb	9K
9	DQa	2H		42	DQb	8K
10	STRBA*	3H		43	STRBB*	7K
11	STRBA*	3K		44	STRBB	7H
12	DQa	2K		45	DQb	8H
13	DQa	1K		46	DQb	9H
14	DQa	2M		47	DQb	8F
15	DQa	1M		48	DQb	9F
16	DQa	2P		49	DQb	8D
17	DQa	1P		50	DQb	9D
18	DQa	2T		51	DQb	8B
19	DQa	1T		52	DQb	9B
20	DQa	3P		53	DQb	7D
21	SA	3T		54	SA	7A
22	SA	4P		55	SA	7B
23	SA	4R		56	RESET	6C
24	SA	4T		57	ADS	5D
25	SA1	5R		58	W	5C
26	SA0	5T		59	K	5F
27	SA	5M		60	SE3	4B
28	SA	5N		61	SK	5G
29	SA	5P		62	NU/V$_{SS}$	5J
30	SA	6P		63	SE2	5A
31	SA	6R		64	SE1	4A
32	SA	6T		65	SA	3A
33	NC*	7T		66	SA	3B

* Scans as logic 0.

TEST ACCESS PORT PINS

TCK — TEST CLOCK (INPUT)

Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.

TMS — TEST MODE SELECT (INPUT)

The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will not produce the same result as a logic one input level (not IEEE 1149.1 compliant).

TDI — TEST DATA IN (INPUT)

The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction register (refer to Figure 10, TAP Controller State Diagram). An undriven TDI pin will not produce the same result as a logic one input level (not IEEE 1149.1 compliant).

TDO — TEST DATA OUT (OUTPUT)

Output that is active depending on the state of the TAP state machine (refer to Figure 10, TAP Controller State Diagram). Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

TRST — TAP RESET

The TRST is an asynchronous input that resets the TAP controller and pre–loads the instruction register with the IDCODE command. This type of reset does not affect the operation of the system logic. The reset affects test logic only.

TEST ACCESS PORT REGISTERS

OVERVIEW

The various TAP registers are selected (one at a time) via the sequences of ones and zeros input to the TMS pin as the TCK is strobed. Each of the TAPs registers are serial shift registers that capture serial input data on the rising edge of TCK and push serial data out on subsequent falling edge of TCK. When a register is selected it is "placed" between the TDI and TDO pins.

INSTRUCTION REGISTER

The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run test/idle or the various data register states. The instructions are three bits long. The register can be loaded when it is placed between the TDI and TDO pins. The parallel outputs of the instruction register are automatically preloaded with the IDCODE instruction when TRST is asserted or whenever the controller is placed in the test–logic–reset state. The two least significant bits of the serial instruction register are loaded with a binary "or" pattern in the capture–IR state.

BYPASS REGISTER

The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible.

BOUNDARY SCAN REGISTER

The boundary scan register is identical in length to the number of active input and I/O connections on the RAM (not counting the TAP pins). This also includes a number of place holder locations (always set to a logic 0) reserved for density upgrade address pins. There are a total of 66 bits in the case of the x36 device. The boundary scan register, under the control of the TAP controller, is loaded with the contents of the RAMs I/O ring when the controller is in capture–DR state and then is placed between the TDI and TDO pins when the controller is moved to shift–DR state.

The Bump/Bit Scan Order table describes which device bump connects to each boundary scan register location. The first column defines the bit's position in the boundary scan register. The shift register bit nearest TDO (i.e., first to be shifted out) is defined as bit 1. The second column is the name of the input or I/O at the bump and the third column is the bump number.

IDENTIFICATION (ID) REGISTER

The ID Register is a 32–bit register that is loaded with a device and vendor specific 32–bit code when the controller is put in capture–DR state with the IDCODE command loaded in the instruction register. The code is loaded from a 32–bit on–chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into shift–DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID Register Presence Indicator

Bit #	0
Value	1

Motorola JEDEC ID Code (Compressed Format, per IEEE Standard 1149.1–1990

Bit #	11	10	9	8	7	6	5	4	3	2	1
Value	0	0	0	0	0	0	0	1	1	1	0

Reserved For Future Use

Bit #	16	15	14	13	12
Value	0	0	0	1	0

Device Width

Bit #	20	19	18	17
Value	0	0	1	1

Device Depth

Bit #	24	23	22	21
Value	0	0	1	0

Revision Number

Bit #	31	30	29	28	27	26	25
Value	0	0	0	0	0	0	1

Figure 9. ID Register Bit Meanings

TAP CONTROLLER INSTRUCTION SET

OVERVIEW

There are two classes of instructions defined in the IEEE Standard 1149.1–1990; the standard (public) instructions and device specific (private) instructions. Some public instructions, are mandatory for IEEE 1149.1 compliance. Optional public instructions must be implemented in prescribed ways.

Although the TAP controller in this device follows the IEEE 1149.1 conventions, it is not IEEE 1149.1 compliant because some of the mandatory instructions are not fully implemented. The TAP on this device may be used to monitor all input and I/O pads, but can not be used to load address, data, or control signals into the RAM or to preload the I/O buffers. In other words, the device will not perform IEEE 1149.1 EXTEST, INTEST, or the preload portion of the SAMPLE/PRELOAD command.

When the TAP controller is placed in capture–IR state, the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the shift–IR state the instruction register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to update–IR state. The TAP instruction sets for this device are listed in the following tables.

STANDARD (PUBLIC) INSTRUCTIONS

BYPASS

The BYPASS instruction is loaded in the instruction register when the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift–DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is an IEEE 1149.1 mandatory public instruction. When the SAMPLE/PRELOAD instruction is loaded in the Instruction register, moving the TAP controller out of the capture–DR state loads the data in the RAMs input and I/O buffers into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK), it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e., in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results can not be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture setup, plus hold time (t_{CS} plus t_{CH}). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register.

Moving the controller to shift–DR state then places the boundary scan register between the TDI and TDO pins. Because the PRELOAD portion of the command is not implemented in this device, moving the controller to the update–DR state with the SAMPLE/PRELOAD instruction loaded in the instruction register has the same effect as the pause–DR command. This functionality is not IEEE 1149.1 compliant.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register, whatever length it may be in the device, is loaded with all logic 0s. EXTEST is not implemented in this device.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture–DR mode and places the ID register between the TDI and TDO pins in shift–DR mode. The IDCODE instruction is the default instruction loaded in at TRST assertion and any time the controller is placed in the test–logic–reset state.

THE DEVICE SPECIFIC (PUBLIC) INSTRUCTION

SAMPLE–Z

If the HIGH–Z instruction is loaded in the instruction register, all DQ pins are forced to an inactive drive state (High–Z) and the bypass register is connected between TDI and TDO when the TAP controller. is moved to the shift–DR state.

THE DEVICE SPECIFIC (PRIVATE) INSTRUCTION

NO OP

Do not use these instructions; they are reserved for future use.

## STANDARD AND DEVICE SPECIFIC (PUBLIC) INSTRUCTION CODES

Instruction	Code*	Description
IDCODE	001**	Preloads ID register and places it between TDI and TDO. Does not affect RAM operation.
HIGH–Z	010	Captures I/O ring contents. Places the bypass register between TDI and TDO. Forces all DQ pins to High–Z. **NOT IEEE 1149.1 COMPLIANT.**
BYPASS	011	Places bypass register between TDI and TDO. Does not affect RAM operation. **NOT IEEE 1149.1 COMPLIANT.**
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect RAM operation. Does not implement IEEE 1149.1 Preload function. **NOT IEEE 1149.1 COMPLIANT.**

 * Instruction codes expressed in binary, MSB on left, LSB on right.
 ** Default instruction automatically loaded when TRST asserted or in test–logic–reset state.

STANDARD (PRIVATE) INSTRUCTION CODES

Instruction	Code*	Description
NO OP	000	Do not use these instructions; they are reserved for future use.
NO OP	101	Do not use these instructions; they are reserved for future use.
NO OP	110	Do not use these instructions; they are reserved for future use.
NO OP	111	Do not use these instructions; they are reserved for future use.

* Instruction codes expressed in binary, MSB on left, LSB on right.
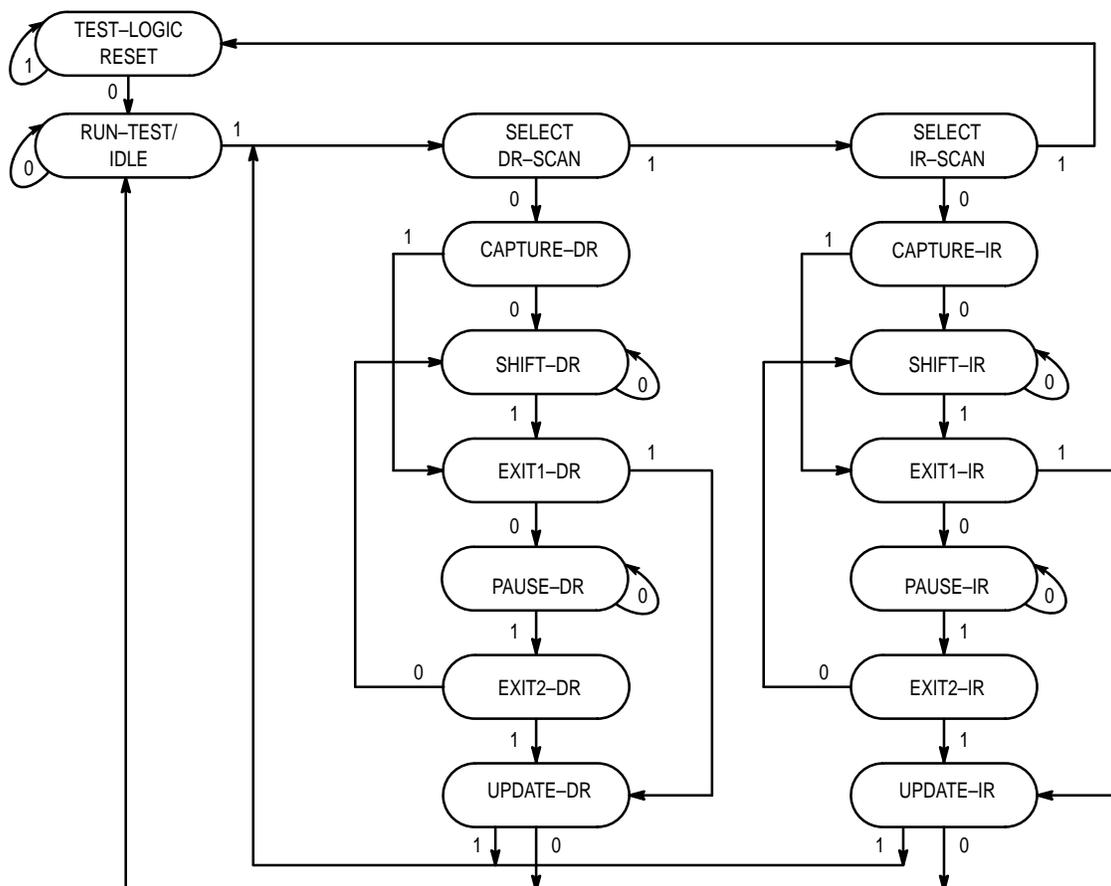
NOTE: The value adjacent to each state transition represents the signal present at TMS at the rising edge of TCK.

Figure 10. TAP Controller State Diagram

ORDERING INFORMATION
(Order by Full Part Number)

MCM   **63P636**   **XX**   **XXX**   **X**

Motorola Memory Prefix ⎯⎯⎯⎯

Part Number ⎯⎯⎯⎯

Blank = Trays, R = Tape and Reel

Speed (250 = 250 MHz, 225 = 225 MHz, 200 = 200 MHz)

Package (TQ = TQFP, ZP = PBGA)
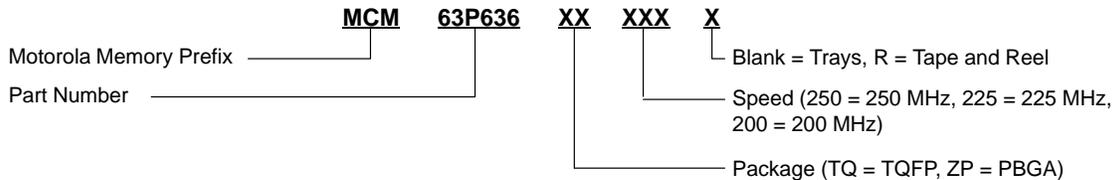
Full Part Numbers —
MCM63P636TQ200	MCM63P636TQ200R
MCM63P636ZP200	MCM63P636ZP200R
MCM63P636ZP225	MCM63P636ZP225R
MCM63P636ZP250	MCM63P636ZP250R

PACKAGE DIMENSIONS

ZP PACKAGE
9 x 17 BUMP PBGA
CASE 1107–01
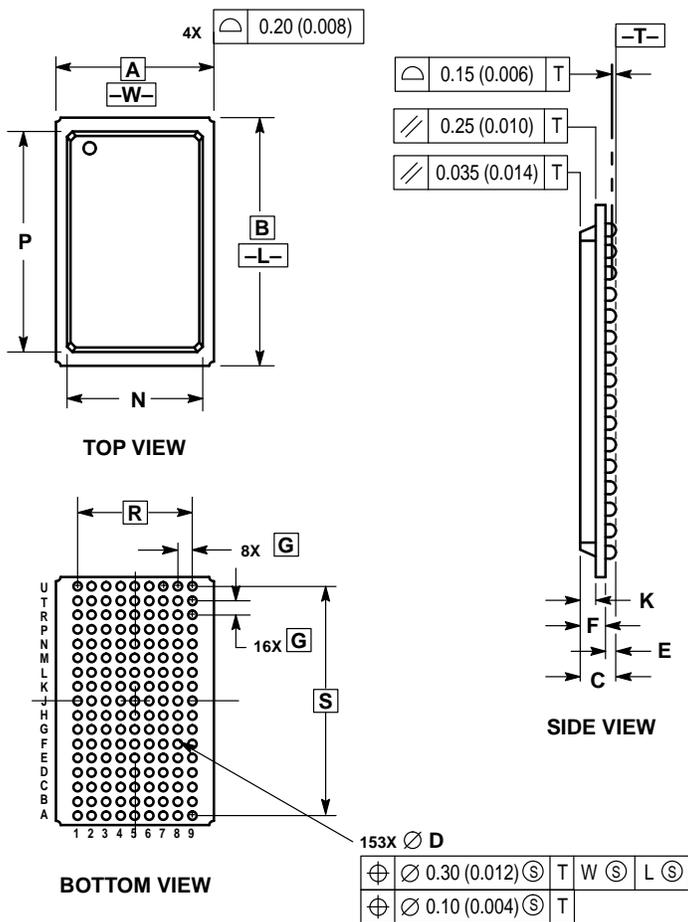
TOP VIEW

BOTTOM VIEW

SIDE VIEW

4X ⌓ 0.20 (0.008)

⌓ 0.15 (0.006) | T

∥ 0.25 (0.010) | T

∥ 0.035 (0.014) | T

8X G

16X G

153X ⌀ D

⊕ | ⌀ 0.30 (0.012) Ⓢ | T | W Ⓢ | L Ⓢ

⊕ | ⌀ 0.10 (0.004) Ⓢ | T

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.00 BSC		0.551 BSC	
B	22.00 BSC		0.866 BSC	
C	—	2.40	—	0.094
D	0.60	0.90	0.024	0.035
E	0.50	0.70	0.020	0.028
F	1.30	1.70	0.051	0.067
G	1.27 BSC		0.050 BSC	
K	0.80	1.00	0.031	0.039
N	11.90	12.10	0.469	0.476
P	19.40	19.60	0.764	0.772
R	10.16 BSC		0.400 BSC	
S	20.32 BSC		0.800 BSC	

TQ PACKAGE
TQFP
CASE 983A–01
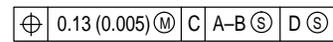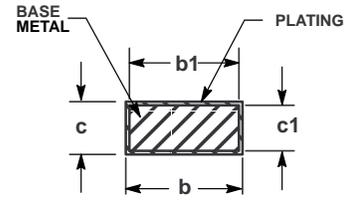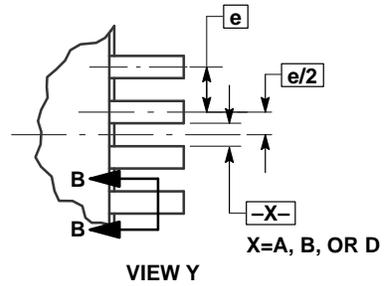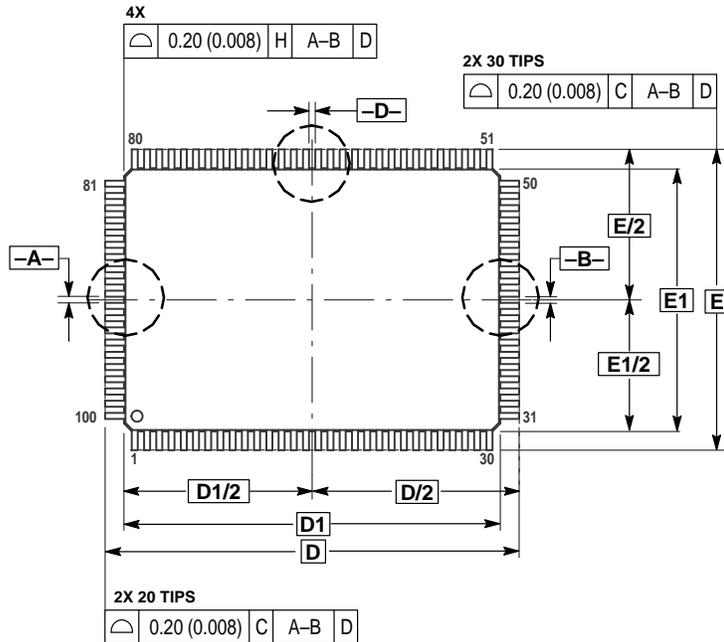
4X
| △ | 0.20 (0.008) | H | A–B | D |

2X 30 TIPS
| △ | 0.20 (0.008) | C | A–B | D |

–D–

80   51
81   50

–A–

–B–

E/2

E1 E

E1/2

100   31

1   30

D1/2   D/2

D1

D

2X 20 TIPS
| △ | 0.20 (0.008) | C | A–B | D |

e

e/2

B

B

–X–

X=A, B, OR D

VIEW Y

BASE
METAL   PLATING

b1

c   c1

b

| ⊕ | 0.13 (0.005) Ⓜ | C | A–B Ⓢ | D Ⓢ |

SECTION B–B

A

–H–

–C–
SEATING
PLANE

θ2

| △ | 0.10 (0.004) | C |

θ3

VIEW AB

| — | 0.05 (0.002) Ⓢ |

S

θ1

A2

0.25 (0.010)
GAGE PLANE

R2

A1   R1

L2

L

L1

θ

VIEW AB

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –A–, –B– AND –D– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE –C–.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS D1 AND B1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE b DIMENSION TO EXCEED 0.45 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	1.60	—	0.063
A1	0.05	0.15	0.002	0.006
A2	1.35	1.45	0.053	0.057
b	0.22	0.38	0.009	0.015
b1	0.22	0.33	0.009	0.013
c	0.09	0.20	0.004	0.008
c1	0.09	0.16	0.004	0.006
D	22.00 BSC		0.866 BSC	
D1	20.00 BSC		0.787 BSC	
E	16.00 BSC		0.630 BSC	
E1	14.00 BSC		0.551 BSC	
e	0.65 BSC		0.026 BSC	
L	0.45	0.75	0.018	0.030
L1	1.00 REF		0.039 REF	
L2	0.50 REF		0.020 REF	
S	0.20	—	0.008	—
R1	0.08	—	0.003	—
R2	0.08	0.20	0.003	0.008
θ	0 °	7 °	0 °	7 °
θ1	0 °	—	0 °	—
θ2	11 °	13 °	11 °	13 °
θ3	11 °	13 °	11 °	13 °

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