

Advance Information

256K/512K Pipelined BurstRAM™ Secondary Cache Module for Pentium™

The MCM64PC32T (256K) and MCM64PC64T (512K) are designed to provide a burstable, high performance, L2 cache for the Pentium microprocessor in conjunction with Intel's Triton II chip set. The MCM64PC32T is configured as 32K x 64 bits and the MCM64PC64T is configured as 64K x 64 bits. Both are packaged in a 160 pin card edge memory module. Each module uses Motorola's 3.3 V 32K x 32 BurstRAMs and one Motorola 3.3 V 32K x 8 FSRAM for the tag RAM.

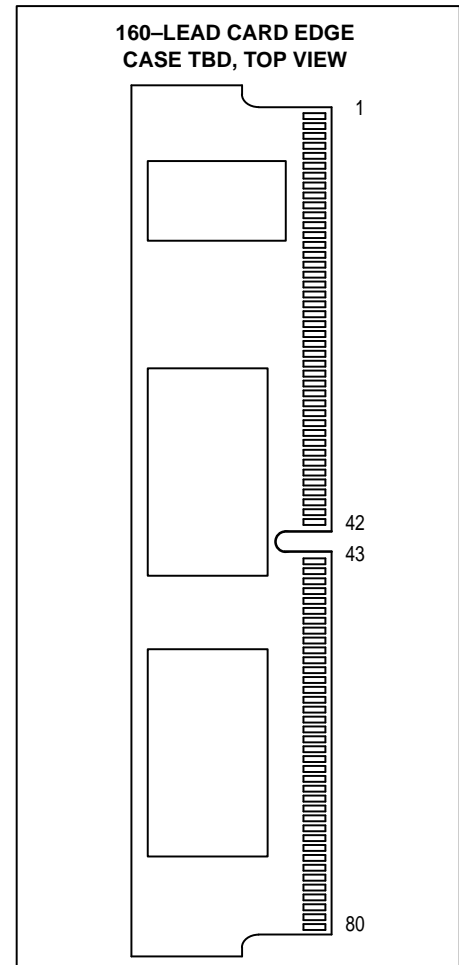
Bursts can be initiated with either address status processor (ADSP) or cache address status (CADS). Subsequent burst addresses are generated internal to the BurstRAM by the cache burst advance (CADV) input pin.

Write cycles are internally self timed and are initiated by the rising edge of the clock (CLK0) input. Eight write enables are provided for byte write control.

PD0 – PD3 map into the Triton II chip set for auto-configuration of the cache control.

- Pentium-Style Burst Counter on Chip
- Pipelined Data Out
- 160 Pin Card Edge Module
- Address Pipeline Supported by ADSP Disabled with \bar{E}_x
- All Cache Data and Tag I/Os are TTL Compatible
- Three State Outputs
- Byte Write Capability
- Fast Module Clock Rate: 66 MHz
- Fast SRAM Access Times: 15 ns for Tag RAM
8 ns for Data RAMs
- 1.5 Cycle Deselect Data RAMs
- Decoupling Capacitors for Each Fast Static RAM
- High Quality Multi-Layer FR4 PWB with Separate Power and Ground Planes
- Single 3.3 V +10%, - 5% Power Supply
- Burndy Connector, Part Number: CELP2X80SC3Z48
- Intel COAST 3.0 Option III Compliant
- Burst Order Select (BOSEL) Option

MCM64PC32T
MCM64PC64T

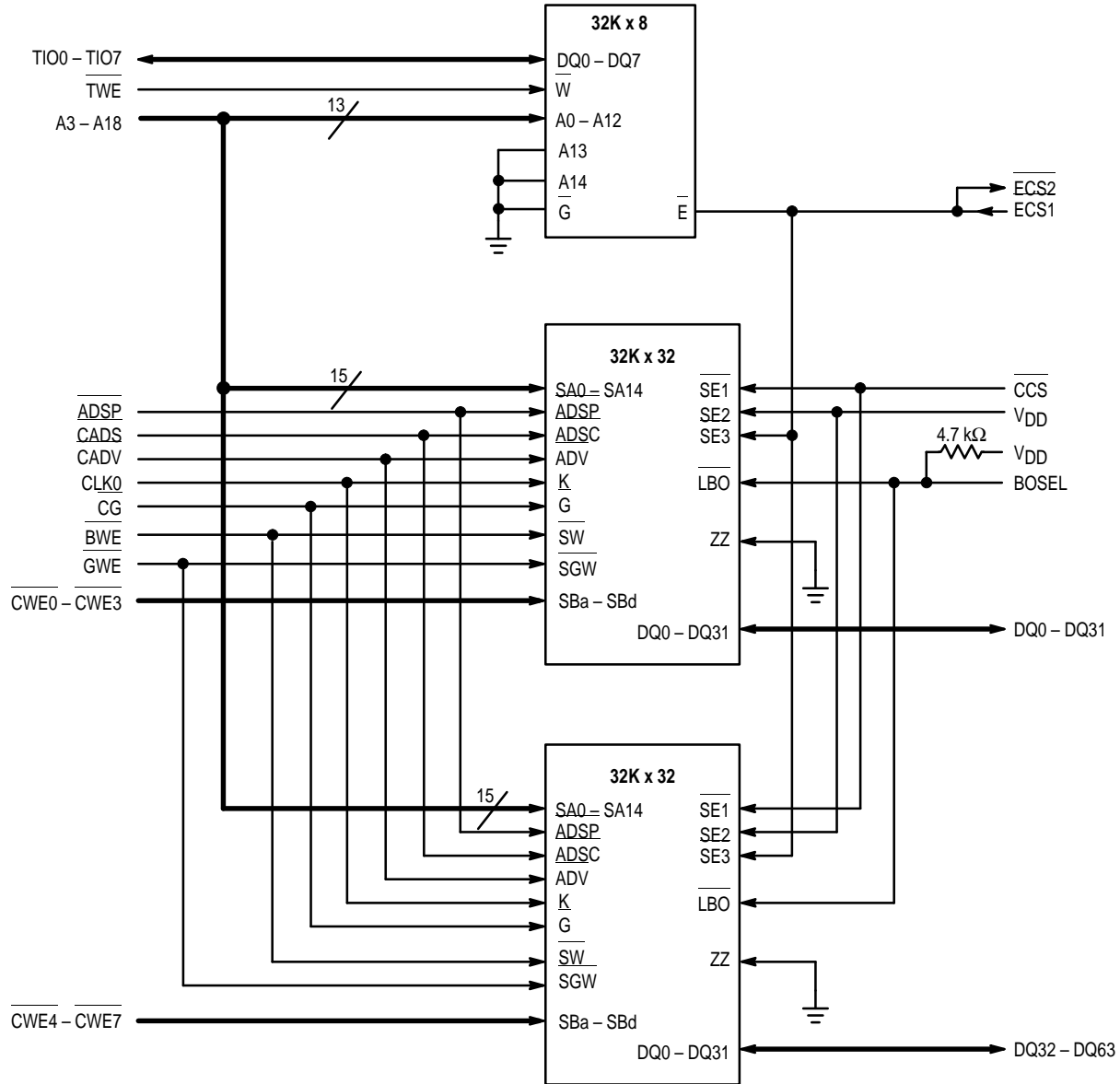


BurstRAM is a trademark of Motorola.
Pentium is a trademark of Intel Corp.

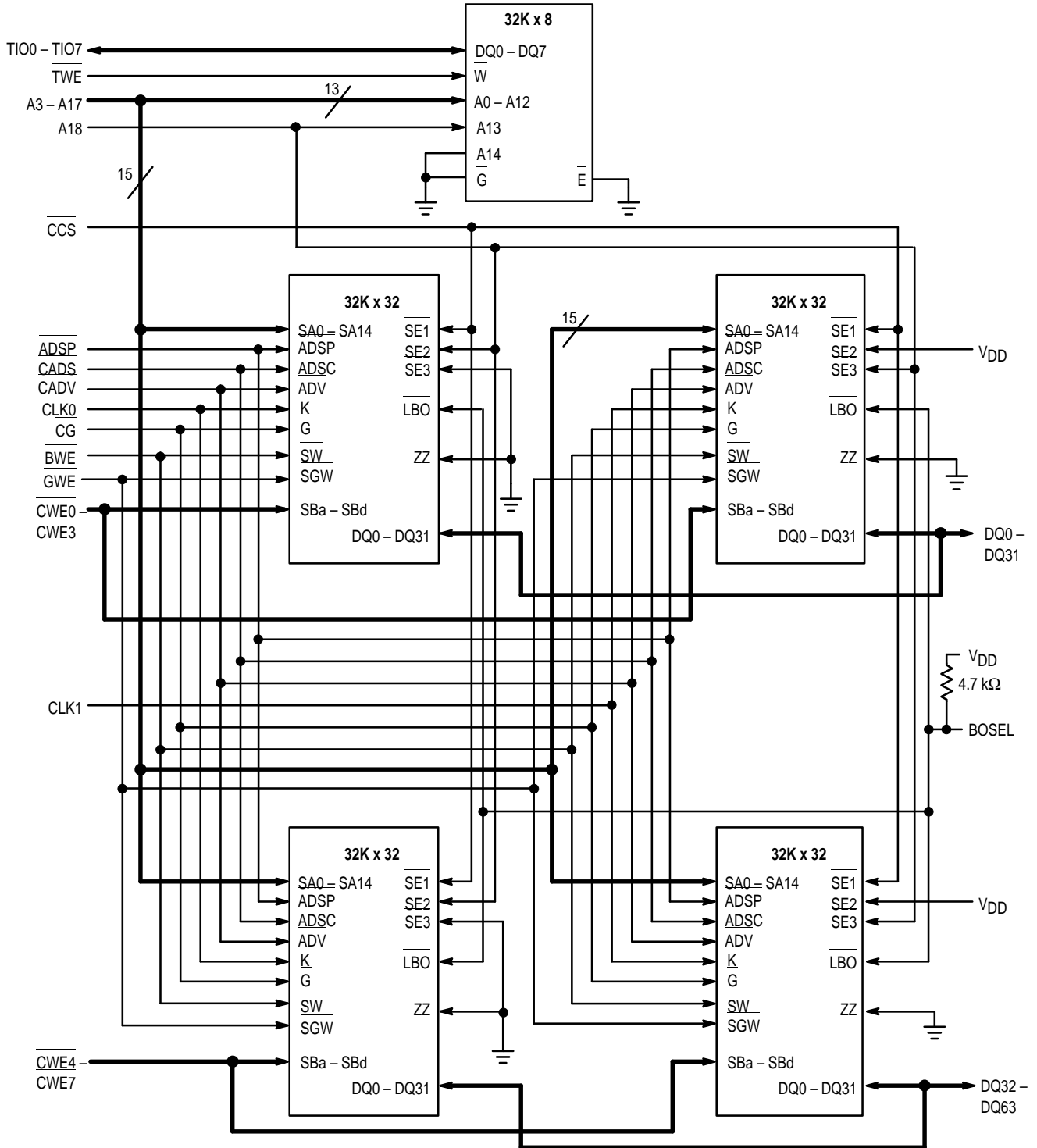
This document contains information on a new product. Specifications and information herein are subject to change without notice.

1/22/97

MCM64PC32T BLOCK DIAGRAM



MCM64PC64T BLOCK DIAGRAM



PIN ASSIGNMENT
160-LEAD CARD EDGE MODULE
(DIMM)
TOP VIEW

PRESENCE DETECT TABLE

| Cache Size and Functionality | PD0 | PD1 | PD2 | PD3 |
|------------------------------|-----------------|-----------------|-----------------|-----------------|
| 256K Pipe Burst | NC | NC | V _{SS} | NC |
| 512K Pipe Burst | V _{SS} | V _{SS} | NC | V _{SS} |

| | | | |
|------------------|-----|----|------------------|
| V _{SS} | 81 | 1 | V _{SS} |
| TIO1 | 82 | 2 | TIO0 |
| TIO7 | 83 | 3 | TIO2 |
| TIO5 | 84 | 4 | TIO6 |
| TIO3 | 85 | 5 | TIO4 |
| NC | 86 | 6 | NC |
| V _{DD5} | 87 | 7 | V _{DD3} |
| NC | 88 | 8 | TWE |
| CADV | 89 | 9 | CADS |
| V _{SS} | 90 | 10 | V _{SS} |
| CG | 91 | 11 | CWE4 |
| CWE5 | 92 | 12 | CWE6 |
| CWE7 | 93 | 13 | CWE0 |
| CWE1 | 94 | 14 | CWE2 |
| V _{DD5} | 95 | 15 | V _{DD3} |
| CWE3 | 96 | 16 | CCS |
| NC | 97 | 17 | GWE |
| NC | 98 | 18 | BWE |
| V _{SS} | 99 | 19 | V _{SS} |
| RSVD | 100 | 20 | A3 |
| A4 | 101 | 21 | A7 |
| A6 | 102 | 22 | A5 |
| A8 | 103 | 23 | A11 |
| A10 | 104 | 24 | A16 |
| V _{DD5} | 105 | 25 | V _{DD3} |
| A17 | 106 | 26 | A18 |
| V _{SS} | 107 | 27 | V _{SS} |
| A9 | 108 | 28 | A12 |
| A14 | 109 | 29 | A13 |
| A15 | 110 | 30 | ADSP |
| RSVD | 111 | 31 | ECS1 |
| PD0 | 112 | 32 | ECS2 |
| PD2 | 113 | 33 | PD1 |
| BOSEL | 114 | 34 | PD3 |
| V _{SS} | 115 | 35 | V _{SS} |
| CLK0 | 116 | 36 | CLK1 |
| V _{SS} | 117 | 37 | V _{SS} |
| DQ63 | 118 | 38 | DQ62 |
| V _{DD5} | 119 | 39 | V _{DD3} |
| DQ61 | 120 | 40 | DQ60 |
| DQ59 | 121 | 41 | DQ58 |
| DQ57 | 122 | 42 | DQ56 |
| V _{SS} | 123 | 43 | V _{SS} |
| DQ55 | 124 | 44 | DQ54 |
| DQ53 | 125 | 45 | DQ52 |
| DQ51 | 126 | 46 | DQ50 |
| DQ49 | 127 | 47 | DQ48 |
| V _{SS} | 128 | 48 | V _{SS} |
| DQ47 | 129 | 49 | DQ46 |
| DQ45 | 130 | 50 | DQ44 |
| DQ43 | 131 | 51 | DQ42 |
| V _{DD5} | 132 | 52 | V _{DD3} |
| DQ41 | 133 | 53 | DQ40 |
| DQ39 | 134 | 54 | DQ38 |
| DQ37 | 135 | 55 | DQ36 |
| V _{SS} | 136 | 56 | V _{SS} |
| DQ35 | 137 | 57 | DQ34 |
| DQ33 | 138 | 58 | DQ32 |
| DQ31 | 139 | 59 | DQ30 |
| V _{DD5} | 140 | 60 | V _{DD3} |
| DQ29 | 141 | 61 | DQ28 |
| DQ27 | 142 | 62 | DQ26 |
| DQ25 | 143 | 63 | DQ24 |
| V _{SS} | 144 | 64 | V _{SS} |
| DQ23 | 145 | 65 | DQ22 |
| DQ21 | 146 | 66 | DQ20 |
| DQ19 | 147 | 67 | DQ18 |
| V _{DD5} | 148 | 68 | V _{DD3} |
| DQ17 | 149 | 69 | DQ16 |
| DQ15 | 150 | 70 | DQ14 |
| DQ13 | 151 | 71 | DQ12 |
| V _{SS} | 152 | 72 | V _{SS} |
| DQ11 | 153 | 73 | DQ10 |
| DQ9 | 154 | 74 | DQ8 |
| DQ7 | 155 | 75 | DQ6 |
| V _{DD5} | 156 | 76 | V _{DD3} |
| DQ5 | 157 | 77 | DQ4 |
| DQ3 | 158 | 78 | DQ2 |
| DQ1 | 159 | 79 | DQ0 |
| V _{SS} | 160 | 80 | V _{SS} |

PIN DESCRIPTIONS

| 160-Lead Card Edge Pin Locations | Symbol | Type | Description |
|--|----------------|--------|--|
| 20, 21, 22, 23, 24, 26, 28, 29, 101, 102, 103, 104, 106, 108, 109, 110 | A3 – A18 | Input | Address Inputs: These inputs are registered into data RAMs and must meet setup and hold times. The tag RAM addresses are not registered. |
| 30 | ADSP | Input | Address Status Processor: Initiates READ, WRITE, or chip deselect cycle (Exception—chip deselect does not occur when ADSP is asserted and CCS is high. |
| 114 | BOSEL | Input | Burst Order Select: NC for interleaved burst counter. Tie to ground for linear burst counter. |
| 18 | BWE | Input | Byte Write Enable: To be used in future modules. |
| 9 | CADS | Input | Cache Address Status: Initiates READ, WRITE, or chip deselect cycle. |
| 89 | CADV | Input | Cache Burst Advance: Increments address count in accordance with interleaved count style. |
| 16 | CCS | Input | Chip Select: Active low chip enable for data RAMs. |
| 91 | CG | Input | Cache Output Enable: Active low asynchronous input. Low—enables output buffers (DQ pins) High—DQx pins are high impedance. |
| 36, 116 | CLK0, CLK1 | Input | Clock: This signal registers the address, data in, and all control signals except CG. |
| 11, 12, 13, 14, 92, 93, 94, 96 | CWE0– CWE7 | Input | Cache Data Byte Write Enable: Active low write signal for data RAMs. |
| 38, 40, 41, 42, 44, 45, 46, 47, 49, 50, 51, 53, 54, 55, 57, 58, 59, 61, 62, 63, 65, 66, 67, 69, 70, 71, 73, 74, 75, 77, 78, 79, 118, 120, 121, 122, 124, 125, 126, 127, 129, 130, 131, 133, 134, 135, 137, 138, 139, 141, 142, 143, 145, 146, 147, 149, 150, 151, 153, 154, 155, 157, 158, 159 | DQ0 – DQ63 | I/O | Synchronous Data I/O: Drives data out of data RAMs during READ cycles. Stores data to data RAMs during WRITE cycles. |
| 31, 32 | ECS1, ECS2 | Input | Expansion Chip Select |
| 17 | GWE | Input | Global Write Enable: To be used in future modules. |
| 33, 34, 112, 113 | PD0 – PD3 | — | Presence Detect: See Presence Detect Table |
| 100, 111 | RSVD | — | No Connection: Reserved for future use. |
| 2, 3, 4, 5, 82, 83, 84, 85 | TIO0 – TIO7 | I/O | Tag RAM I/O: Drives data out during tag compare cycles. Stores data to tag RAM during tag WRITE cycles. |
| 8 | TWE | Input | Tag Write Enable: Active low write signal for tag RAMs. |
| 7, 15, 25, 39, 52, 60, 68, 76 | VDD3 | Supply | Power Supply: 3.3 V + 10%, – 5%. |
| 87, 95, 105, 119, 132, 140, 148, 156 | VDD5 | Supply | Power Supply: 5.0 V ± 5%. |
| 1, 10, 19, 27, 35, 37, 43, 48, 56, 64, 72, 80, 81, 90, 99, 107, 115, 117, 123, 128, 136, 144, 152, 160 | VSS | Supply | Ground |
| 6, 86, 88, 97, 98 | NC | — | No Connection: There is no connection to the module. |

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

| CCS | ADSP | CADS | CADV | CWEx | CLK0 | Address Used | Operation |
|-----|------|------|------|------|------|------------------|-----------------------------|
| H | X | L | X | X | L-H | N/A | Deselected |
| L | L | X | X | X | L-H | External Address | Read Cycle, Begin Burst |
| L | H | L | X | L | L-H | External Address | Write Cycle, Begin Burst |
| L | H | L | X | H | L-H | External Address | Read Cycle, Begin Burst |
| X | H | H | L | L | L-H | Next Address | Write Cycle, Continue Burst |
| X | H | H | L | H | L-H | Next Address | Read Cycle, Continue Burst |
| X | H | H | H | L | L-H | Current Address | Write Cycle, Suspend Burst |
| X | H | H | H | H | L-H | Current Address | Read Cycle, Suspend Burst |
| H | X | H | L | L | L-H | Next Address | Write Cycle, Continue Burst |
| H | X | H | L | H | L-H | Next Address | Read Cycle, Continue Burst |
| H | X | H | H | L | L-H | Current Address | Write Cycle, Suspend Burst |
| H | X | H | H | H | L-H | Current Address | Read Cycle, Suspend Burst |

NOTES:

1. X means Don't Care.
2. All inputs except CG must meet setup and hold times for the low-to-high transition of clock (CLK0/1).
3. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

| Operation | CG | I/O Status |
|------------|----|------------------|
| Read | L | Data Out |
| Read | H | High-Z |
| Write | X | High-Z — Data In |
| Deselected | X | High-Z |

NOTES:

1. X means Don't Care.
2. For a write operation following a read operation, G must be high before the input data required setup time and held high through the input data hold time.

DC ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to $V_{SS} = 0$ V)

| Rating | Symbol | Value | Unit |
|------------------------------|-------------------|-----------------------------------|------|
| Power Supply Voltage | V_{DD3} | - 0.5 to + 4.6 | V |
| Voltage Relative to V_{SS} | V_{in}, V_{out} | $V_{SS} - 0.5$ to $V_{DD3} + 0.5$ | V |
| Output Current (per I/O) | I_{out} | ± 20 | mA |
| Temperature Under Bias | T_{bias} | - 10 to + 85 | °C |
| Operating Temperature | T_J | 20 to +110 | °C |
| Storage Temperature | T_{stg} | - 55 to + 125 | °C |

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High-Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS
 (V_{DD} = 3.3 V + 10%, - 5%, T_J = 20 to + 110°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

| Parameter | Symbol | Min | Max | Unit | Notes |
|--|-----------------|-------|-----------------------|------|-------|
| Supply Voltage (Operating Voltage Range) | V _{DD} | 3.135 | 3.6 | V | 1 |
| Input High Voltage | V _{IH} | 2.0 | V _{DD} + 0.3 | V | 2 |
| Input Low Voltage | V _{IL} | - 0.5 | 0.8 | V | 3 |

NOTES:

1. JEDEC specification 8-1A specifies ± 0.3 V tolerance for V_{DD}.
2. V_{IH} (max) = V_{DD} + 0.3 V dc; V_{IH} (max) = V_{DD} + 1.4 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
3. V_{IL} (min) = - 0.5 V dc; V_{IL} (min) = - 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

| Parameter | Symbol | Min | Max | Unit | Notes |
|--|---------------------|-----|-------|------|-------|
| Input Leakage Current (All Inputs, V _{in} = 0 to V _{DD3}) | I _{Ikg(I)} | — | ± 1.0 | μA | |
| Output Leakage Current (CG = V _{IH}) | I _{Ikg(O)} | — | ± 1.0 | μA | |
| TTL Output Low Voltage (I _{OL} = + 8.0 mA) | V _{OL} | — | 0.4 | V | 1 |
| TTL Output High Voltage (I _{OH} = - 4.0 mA) | V _{OH} | 2.4 | — | V | 1 |

NOTES:

1. Champing diodes exist to V_{SS} and V_{DD}.

POWER SUPPLY CURRENTS

| Parameter | Symbol | Max | Unit |
|--|--|------------|------|
| AC Supply Current (CG = V _{IH} , CCS = V _{IL} , I _{out} = 0 mA, All Inputs = V _{IL} or V _{IH} , V _{IL} = 0.0 V and V _{IH} ≥ 3.0 V, Cycle Time ≥ t _{KHKH} min) | MCM64PC32T MCM64PC64T I _{DDA} | 495 705 | mA |
| AC Standby Current (CG = V _{IH} , CCS = V _{IL} , I _{out} = 0 mA, All Inputs = V _{IL} or V _{IH} , V _{IL} = 0.0 V and V _{IH} ≥ 3.0 V, Cycle Time ≥ t _{KHKH} min) | MCM64PC32T MCM64PC64T I _{SB1} | 230 505 | mA |

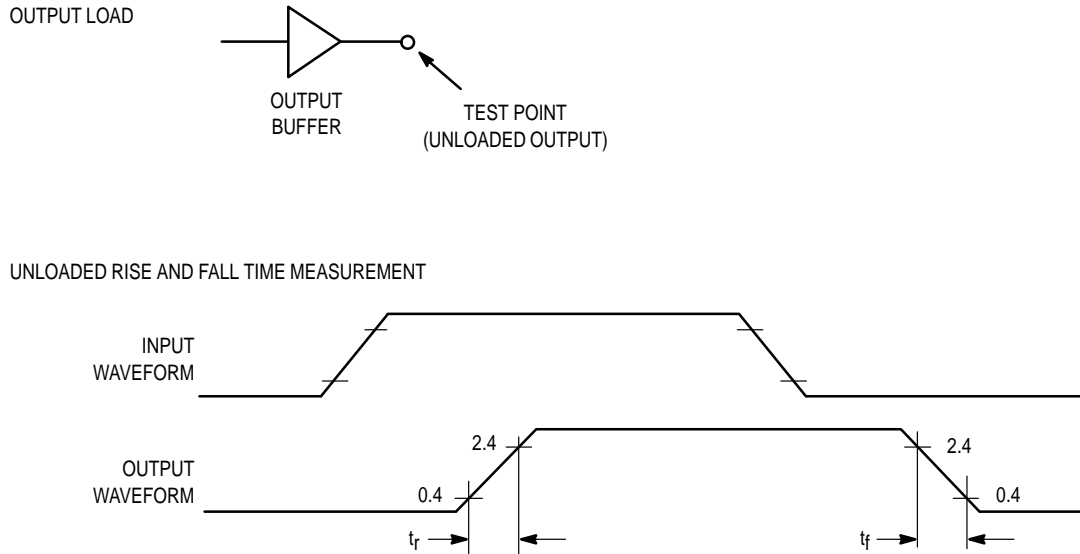
CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_J = 20 to 110°C, Periodically Sampled Rather Than 100% Tested)

| Parameter | Symbol | Max | Unit |
|---------------------------------------|--|----------|------|
| Input Capacitance | MCM64PC32T MCM64PC64T C _{in} | 21 31 | pF |
| Input/Output Capacitance (DQ0 - DQ63) | MCM64PC32T MCM64PC64T C _{I/O} | 8 16 | pF |

DATA RAMs AC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{DD} = 3.3\text{ V} + 10\%, -5\%$ $T_J = 20\text{ to } +110^\circ\text{C}$, Unless Otherwise Noted)

| | | | |
|--|------------|-------------------------------------|-------------------------------------|
| Input Timing Measurement Reference Level | 1.5 V | Output Timing Reference Level | 1.5 V |
| Input Pulse Levels | 0 to 3.0 V | Output Load | See Figure 3 Unless Otherwise Noted |
| Input Rise/Fall Time | 2 ns | | |



NOTES:

1. Input waveform should have a slew rate of 1 V/ns.
2. Rise time is measure from 0.4 V to 2.4 V unloaded.
3. Fall time is measure from 2.4 V to 0.4 V unloaded.

Figure 1. Unloaded Rise and Fall time Characterization

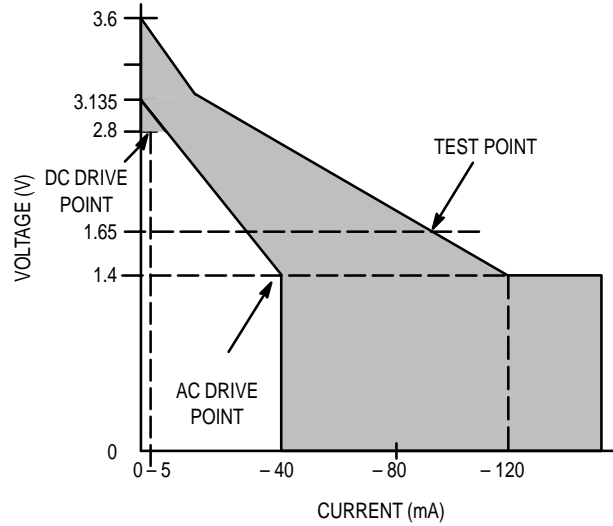
DATA RAMs READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

| Parameter | Symbol | MCM64PC32T-66 MCM64PC32T-66 | | Unit | Notes | |
|--------------------------------|---|--|-----|------|-------|---|
| | | Min | Max | | | |
| Cycle Time | t _{KHKH} | 15 | — | ns | | |
| Clock Access Time | t _{KHQV} | — | 8 | ns | 5 | |
| Output Enable to Output Valid | t _{GLQV} | — | 6 | ns | 5 | |
| Clock High to Output Active | t _{KHQX1} | 0 | — | ns | 5, 7 | |
| Clock High to Output Change | t _{KHQX2} | 2 | — | ns | 5, 7 | |
| Output Enable to Output Active | t _{GLQX} | 0 | — | ns | 5, 7 | |
| Output Disable to Q High-Z | t _{GHQZ} | — | 8 | ns | 6, 7 | |
| Clock High to Q High-Z | t _{KHQZ} | 2 | 8 | ns | 6, 7 | |
| Clock High Pulse Width | t _{KHKL} | 5 | — | ns | | |
| Clock Low Pulse Width | t _{KLKH} | 5 | — | ns | | |
| Setup Times: | Address Address Status Data In Write Address Advance Chip Enable | t _{AVKH} t _{ADSVKH} t _{DVKH} t _{WVKH} t _{ADVVKH} t _{EVKH} | 2.5 | — | ns | 4 |
| Hold Times: | Address Address Status Data In Write Address Advance Chip Enable | t _{KHAX} t _{KHADSX} t _{KHDX} t _{KHWX} t _{KHADVX} t _{KHEX} | 0.5 | — | ns | 4 |

NOTES:

1. Write applies to all SBx, SW, and SGW signals when the chip is selected and ADSP high.
2. Chip Enable applies to all SE1, SE2 and SE3 signals whenever ADSP or ADSC is asserted.
3. All read and write cycle timings are referenced from K or G.
4. G is a don't care after write cycle begins. To prevent bus contention, G should be negated prior to start of write cycle.
5. Tested per AC Test Load.
6. Measured at ± 200 mV from steady state. Tested per High-Z Test Load.
7. This parameter is sampled and is not 100% tested.

| PULL-UP | | |
|-------------|------------|------------|
| VOLTAGE (V) | I (mA) Min | I (mA) Max |
| -0.5 | -40 | -120 |
| 0 | -40 | -120 |
| 1.4 | -40 | -120 |
| 1.65 | -37 | -104 |
| 2 | -28 | -81 |
| 3.135 | 0 | -20 |
| 3.6 | 0 | 0 |

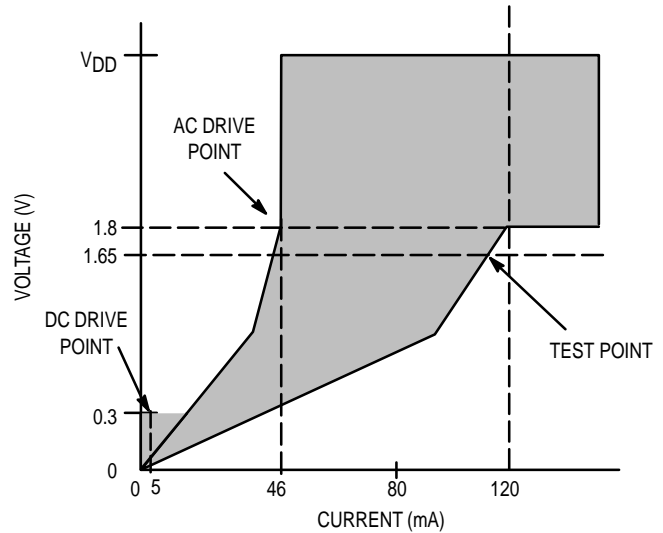


NOTES:

1. Driver impedance @ 1.65 V = 15.9 to 44.6 Ω .
2. Meets the temperature and voltage range specified in DC Characteristics tables.
3. This drawing is not to scale. Comparisons should be made to the table in Figure 2a.

2a. Pull-Up

| PULL-DOWN | | |
|-------------|------------|------------|
| VOLTAGE (V) | I (mA) Min | I (mA) Max |
| -0.5 | -34 | -126 |
| 0 | 0 | 0 |
| 0.5 | 17 | 47 |
| 1 | 35 | 90 |
| 1.65 | 45 | 114 |
| 1.8 | 46 | 120 |
| 3.6 | 46 | 120 |
| 4 | 46 | 120 |



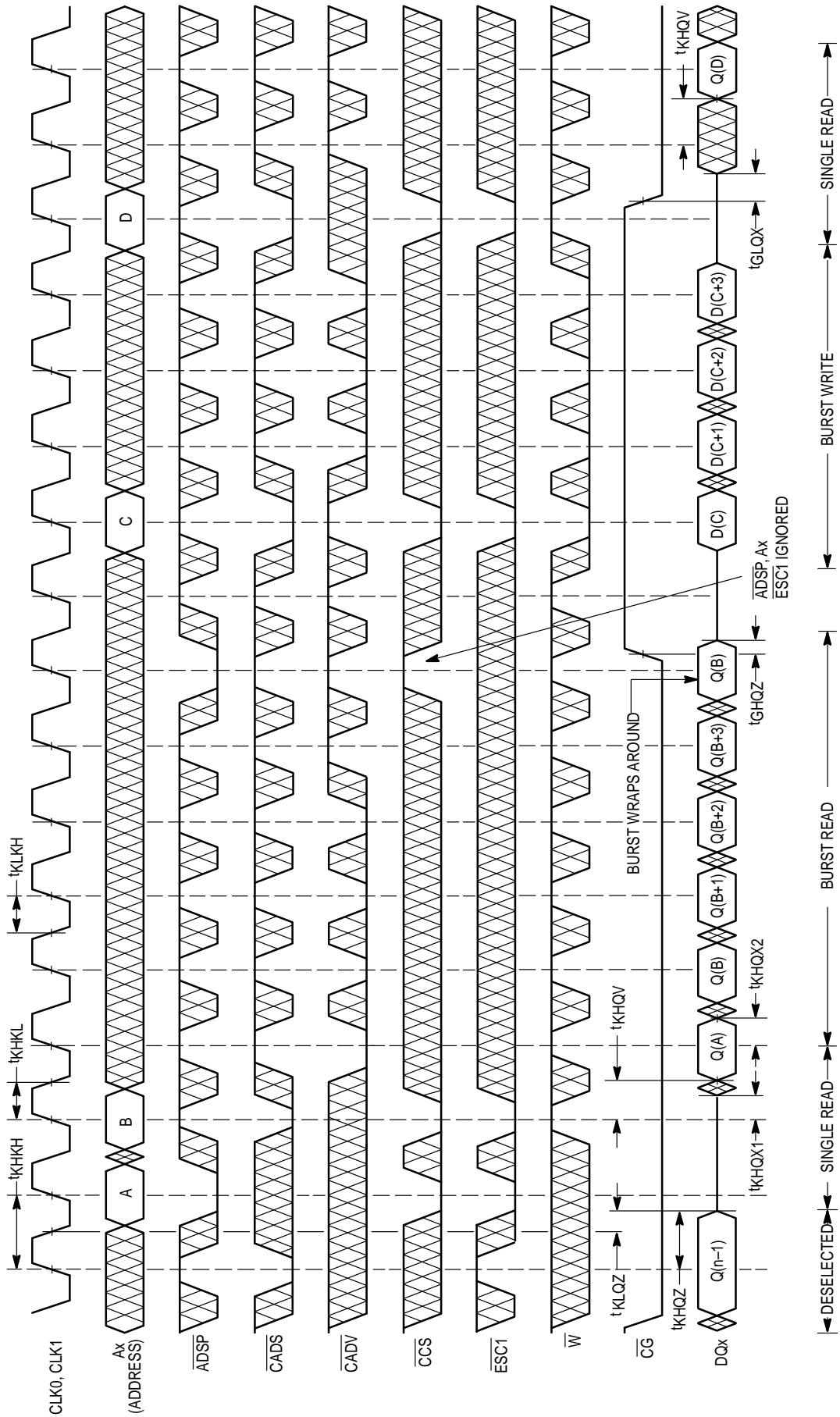
NOTES:

1. Driver impedance @ 1.65 V = 15.9 to 44.6 Ω .
2. Meets the temperature and voltage range specified in DC Characteristics tables.
3. This drawing is not to scale. Comparisons should be made to the table in Figure 2b.

2b. Pull-Down

Figure 2. Output Buffer Characteristics

DATA RAMs READ/WRITE CYCLES



Note: \overline{W} low = \overline{GWE} low and/or \overline{BWE} and \overline{CWEx} low.

TAG RAM AC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $T_J = 20 \text{ to } +110^\circ\text{C}$, Unless Otherwise Noted)

Input Timing Measurement Reference Level 1.5 V
 Input Pulse Levels 0 to 3.0 V
 Input Rise/Fall Time 3 ns

Output Timing Measurement Reference Level 1.5 V
 Output Load Figure 3 Unless Otherwise Noted

TAG RAM READ CYCLE (See Notes 1 and 2)

| Parameter | Symbol | - 15 | | Unit | Notes |
|---------------------------------|------------|------|-----|------|-------|
| | | Min | Max | | |
| Read Cycle Time | t_{AVAV} | 15 | — | ns | 3 |
| Address Access Time | t_{AVQV} | — | 15 | ns | |
| Output Hold from Address Change | t_{AXQX} | 4 | — | ns | 4, 5 |

NOTES:

1. \overline{CWE} is high for read cycle.
2. Device is continuously selected ($\overline{CG} = V_{IL}$).
3. All timings are referenced from the last valid address to the first address transition.
4. Transition is measured $\pm 500 \text{ mV}$ from steady-state voltage with load of Figure 3b.
5. This parameter is sampled and not 100% tested.

TAG RAM READ CYCLE (See Note 5)

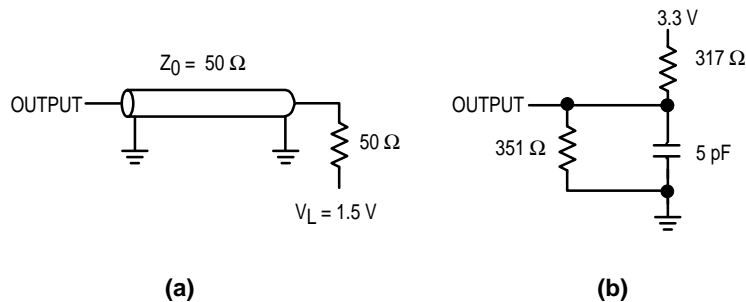
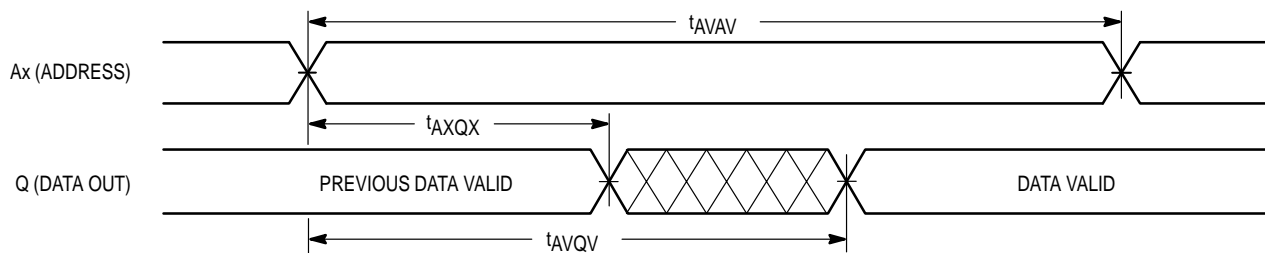


Figure 3. Test Loads

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

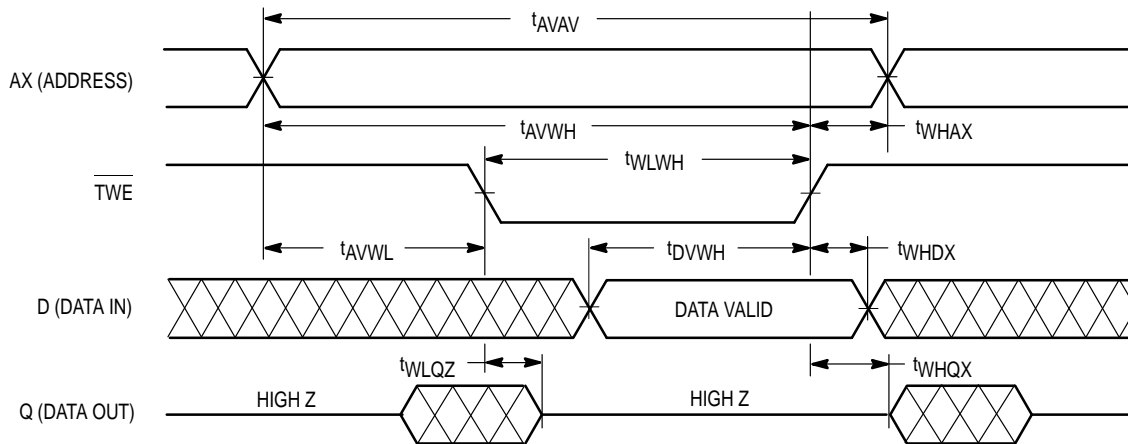
TAG RAM WRITE CYCLE (See Notes 1 and 2)

| Parameter | Symbol | - 15 | | Unit | Notes |
|-------------------------------|------------|------|-----|------|-------|
| | | Min | Max | | |
| Write Cycle Time | t_{AVAV} | 15 | — | ns | 3 |
| Address Setup Time | t_{AVWL} | 0 | — | ns | |
| Address Valid to End of Write | t_{AVWH} | 12 | — | ns | |
| Data Valid to End of Write | t_{DVWH} | 7 | — | ns | |
| Data Hold Time | t_{WHDX} | 0 | — | ns | |
| Write Low to Output High-Z | t_{WLQZ} | 0 | 7 | ns | 5,6,7 |
| Write High to Output Active | t_{WHQX} | 4 | — | ns | 5,6,7 |
| Write Recovery Time | t_{WHAX} | 0 | — | ns | |

NOTES:

1. A write occurs when \overline{CWE} is low.
2. If CG goes low coincident with or after \overline{CWE} goes low, the output will remain in a high impedance state.
3. All timings are referenced from the last valid address to the first address transition.
4. If $CG \geq V_{IH}$, the output will remain in a high impedance state.
5. At any given voltage and temperature, t_{WLQZ} (max) is less than t_{WHQX} (min), both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady-state voltage with load of Figure 3b.
7. This parameter is sampled and not 100% tested.

TAG RAM WRITE CYCLE (See Notes 1 and 2)



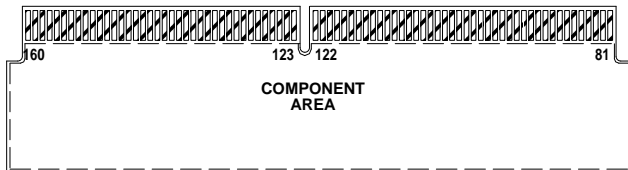
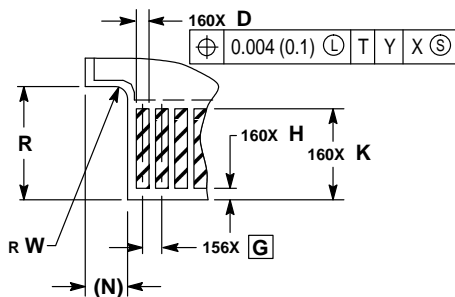
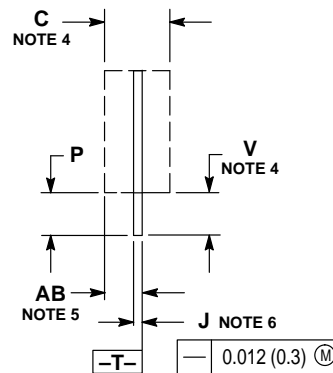
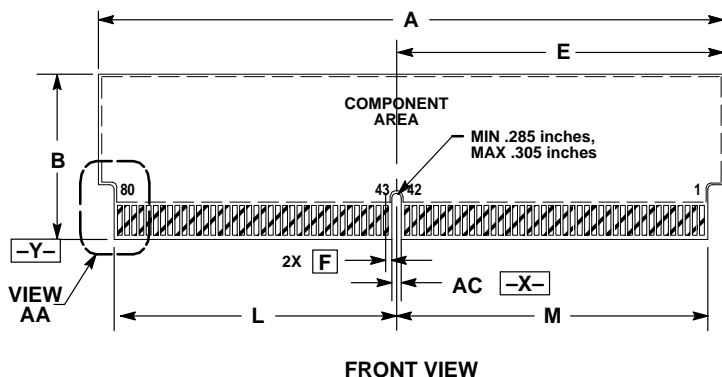
ORDERING INFORMATION
(Order by Full Part Number)



Full Part Number — MCM64PC32TSG66 MCM64PC64TSG66

PACKAGE DIMENSIONS


**160-LEAD
CARD EDGE MODULE
CASE TBD**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALLIZATION.
 4. DIMENSIONS C AND V DEFINE A DOUBLE-SIDED MODULE.
 5. DIMENSION AB DEFINES OPTIONAL SINGLE-SIDED MODULE.
 6. STRAIGHTNESS CALLOUT APPLIES TO TAB AREA ONLY.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|--------|
| | MIN | MAX | MIN | MAX |
| A | 4.330 | 4.350 | 109.98 | 110.49 |
| B | 1.120 | 1.140 | 28.45 | 28.96 |
| C | — | 0.454 | — | 11.53 |
| D | 0.033 | 0.037 | 0.84 | 0.94 |
| E | 2.265 | 2.275 | 57.53 | 57.79 |
| F | 0.075 BSC | | 1.91 BSC | |
| G | 0.050 BSC | | 1.27 BSC | |
| H | — | 0.030 | — | 0.51 |
| J | 0.055 | 0.069 | 1.40 | 1.75 |
| K | 0.210 | — | 5.33 | — |
| L | 1.955 | 1.965 | 49.66 | 49.91 |
| M | 2.155 | 2.165 | 54.74 | 54.99 |
| N | 0.110 REF | | 2.79 REF | |
| P | 0.300 | — | 7.62 | — |
| R | 0.492 | 0.512 | 7.24 | 7.75 |
| V | 0.300 | — | 7.62 | — |
| W | 0.040 | 0.060 | 1.02 | 1.52 |
| AB | — | 0.262 | — | 6.66 |
| AC | 0.072 | 0.076 | 1.83 | 1.93 |

NOTE: Case Outline number to be determined.

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and  are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

Mfax is a trademark of Motorola, Inc.

How to reach us:

USA/EUROPE/Locations Not Listed: Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado, 80217. 303-675-2140 or 1-800-441-2447

Mfax™: RMFAX0@email.sps.mot.com — TOUCHTONE 602-244-6609
INTERNET: <http://Design-NET.com>

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, 6F Seibu-Butsuryu-Center,
3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 81-3-3521-8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

