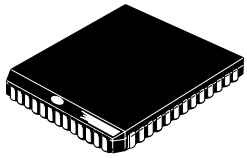
# MCM67C618A

# 64K x 18 Bit BurstRAM™ Synchronous Fast Static RAM

## With Burst Counter and Registered Outputs



**FN PACKAGE**
**PLASTIC**
**CASE 778–02**

The MCM67C618A is a 1,179,648 bit synchronous static random access memory designed to provide a burstable, high–performance, secondary cache for the i486™ and Pentium™ microprocessors. It is organized as 65,536 words of 18 bits, fabricated with Motorola's high–performance silicon–gate BiCMOS technology. The device integrates input registers, a 2–bit counter, high speed SRAM, and high drive registered output drivers onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (A0 – A15), data inputs (D0 – D17), and all control signals except output enable (G) are clock (K) controlled through positive–edge–triggered noninverting registers.

This device contains output registers for pipeline operations. At the rising edge of K, the RAM provides the output data from the previous cycle.

Output enable (G) is asynchronous for maximum system design flexibility.

Burst can be initiated with either address status processor ($\overline{\text{ADSP}}$) or address status cache controller (ADSC) input pins. Subsequent burst addresses can be generated internally by the MCM67C618A (burst sequence imitates that of the i486 and Pentium) and controlled by the burst address advance (ADV) input pin. The following pages provide more detailed information on burst controls.

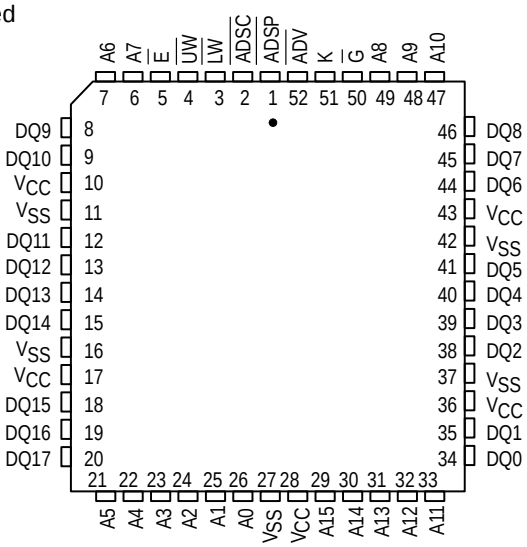
Write cycles are internally self–timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased flexibility for incoming signals.

Dual write enables (LW and UW) are provided to allow individually writeable bytes. LW controls DQ0 – DQ8 (the lower bits), while UW controls DQ9 – DQ17 (the upper bits).

This device is ideally suited for systems that require wide data bus widths and cache memory. See Figure 2 for applications information.

- Single 5 V ± 5% Power Supply
- Fast Access Time/Fast Cycle Time = 5 ns/100 MHz, 7 ns/80 MHz
- Byte Writeable via Dual Write Enables
- Internal Input Registers (Address, Data, Control)
- Output Registers for Pipelined Applications
- Internally Self–Timed Write Cycle
- ADSP, ADSC, and ADV Burst Control Pins
- Asynchronous Output Enable Controlled Three–State Outputs
- Common Data Inputs and Data Outputs
- 3.3 V I/O Compatible
- High Board Density 52–Lead PLCC Package

**PIN ASSIGNMENTS**




| PIN NAMES | |
|---|---|
| A0 – A15 | Address Inputs |
| K | Clock |
| ADV | Burst Address Advance |
| LW | Lower Byte Write Enable |
| UW | Upper Byte Write Enable |
| ADSC | Controller Address Status |
| ADSP | Processor Address Status |
| E | Chip Enable |
| G | Output Enable |
| DQ0 – DQ17 | Data Input/Output |
| $V_{CC}$ | + 5 V Power Supply |
| $V_{SS}$ | Ground |
| NC | No Connection |

All power supply and ground pins must be connected for proper operation of the device.

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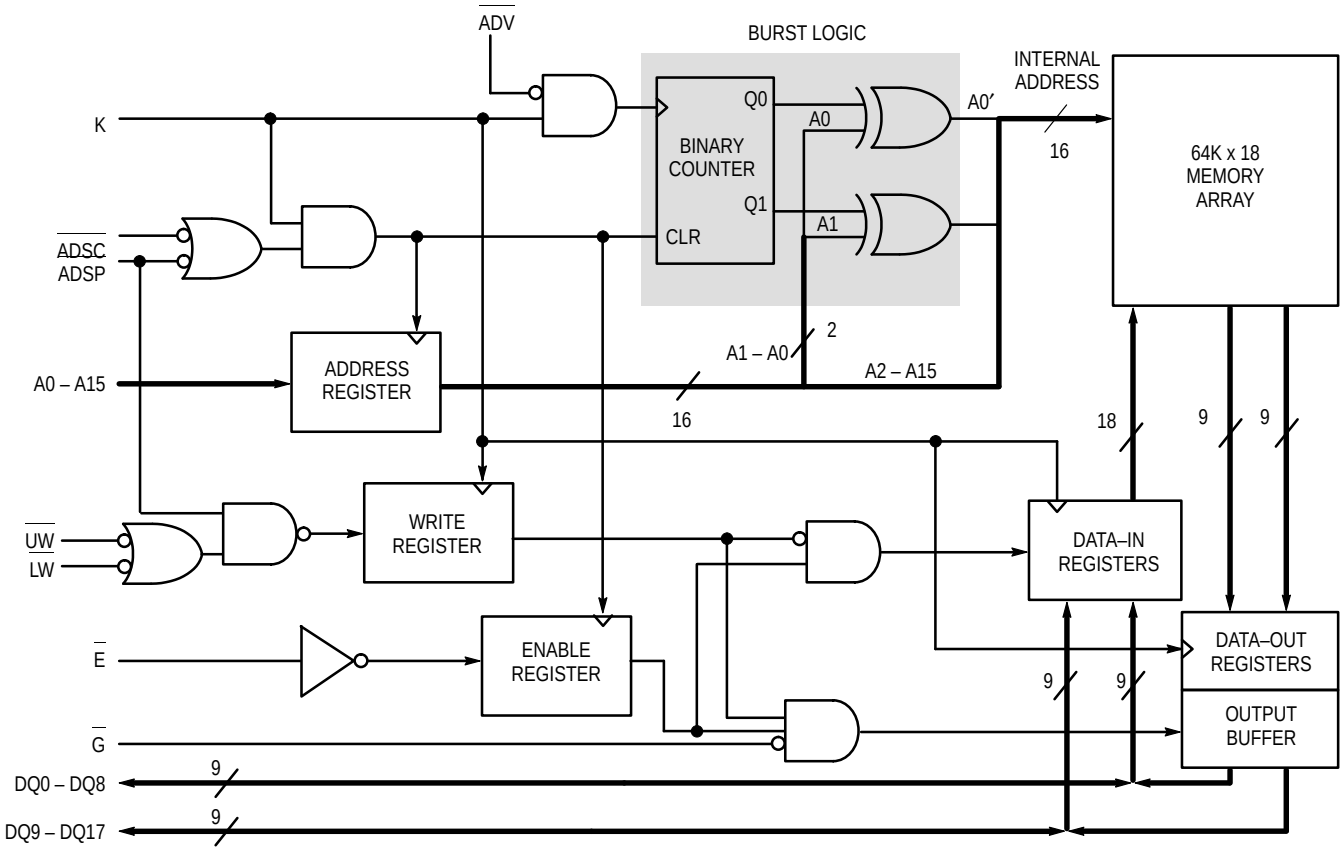
i486 and Pentium are trademarks of Intel Corp.

**REV 2**
**11/5/96**

**BLOCK DIAGRAM** (See Note)




NOTE: All registers are positive–edge triggered. The $\overline{\text{ADSC}}$ or $\overline{\text{ADSP}}$ signals control the duration of the burst and the start of the next burst. When ADSP is sampled low, any ongoing burst is interrupted and a read (independent of W and ADSC) is performed using the new external address. Alternatively, an ADSP–initiated two cycle WRITE can be performed by asserting ADSP and a valid address on the first cycle, then negating both ADSP and ADSC and asserting LW and/or UW with valid data on the second cycle (see Single Write cycle in WRITE CYCLES timing diagram).
When ADSC is sampled low (and ADSP is sampled high), any ongoing burst is interrupted and a read or write (dependent on W) is performed using the new external address. Chip enable (E) is sampled only when a new base address is loaded. After the first cycle of the burst, ADV controls subsequent burst cycles. When ADV is sampled low, the internal address is advanced prior to the operation. When ADV is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**. Write refers to either or both byte write enables (LW, UW).

**BURST SEQUENCE TABLE** (See Note)

| | | | |
|---|---|---|---|
| External Address | A15 – A2 | A1 | A0 |
| 1st Burst Address | A15 – A2 | A1 | $\overline{\text{A0}}$ |
| 2nd Burst Address | A15 – A2 | $\overline{\text{A1}}$ | A0 |
| 3rd Burst Address | A15 – A2 | $\overline{\text{A1}}$ | $\overline{\text{A0}}$ |

NOTE: The burst wraps around to its initial state upon completion.

**SYNCHRONOUS TRUTH TABLE** (See Notes 1, 2, and 3)

| E | ADSP | ADSC | ADV | UW or LW | K | Address Used | Operation |
|---|---|---|---|---|---|---|---|
| H | L | X | X | X | L–H | N/A | Deselected |
| H | X | L | X | X | L–H | N/A | Deselected |
| L | L | X | X | X | L–H | External Address | Read Cycle, Begin Burst |
| L | H | L | X | L | L–H | External Address | Write Cycle, Begin Burst |
| L | H | L | X | H | L–H | External Address | Read Cycle, Begin Burst |
| X | H | H | L | L | L–H | Next Address | Write Cycle, Continue Burst |
| X | H | H | L | H | L–H | Next Address | Read Cycle, Continue Burst |
| X | H | H | H | L | L–H | Current Address | Write Cycle, Suspend Burst |
| X | H | H | H | H | L–H | Current Address | Read Cycle, Suspend Burst |

NOTES:
1. X means Don't Care.
2. All inputs except G must meet setup and hold times for the low–to–high transition of clock (K).
3. Wait states are inserted by suspending burst.

**ASYNCHRONOUS TRUTH TABLE** (See Notes 1 and 2)

| Operation | G | I/O Status |
|---|---|---|
| Read | L | Data Out |
| Read | H | High–Z |
| Write | X | High–Z — Data In |
| Deselected | X | High–Z |

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

**ABSOLUTE MAXIMUM RATINGS** (Voltages Referenced to $V_{SS}$ = 0 V)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | – 0.5 to + 7.0 | V |
| Voltage Relative to $V_{SS}$ for Any Pin Except $V_{CC}$ | $V_{in}$, $V_{out}$ | – 0.5 to $V_{CC}$ + 0.5 | V |
| Output Current (per I/O) | $I_{out}$ | ± 30 | mA |
| Power Dissipation | $P_D$ | 1.6 | W |
| Temperature Under Bias | $T_{bias}$ | – 10 to + 85 | °C |
| Operating Temperature | $T_A$ | 0 to +70 | °C |
| Storage Temperature | $T_{stg}$ | – 55 to + 125 | °C |

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

## DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC}$ = 5.0 V ± 5%, $T_A$ = 0 to + 70°C, Unless Otherwise Noted)

**RECOMMENDED OPERATING CONDITIONS** (Voltages Referenced to $V_{SS}$ = 0 V)

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply Voltage (Operating Voltage Range) | $V_{CC}$ | 4.75 | 5.25 | V |
| Input High Voltage | $V_{IH}$ | 2.2 | $V_{CC}$ + 0.3** | V |
| Input Low Voltage | $V_{IL}$ | – 0.5* | 0.8 | V |

* $V_{IL}$ (min) = – 0.5 V dc; $V_{IL}$ (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
** $V_{IH}$ (max) = $V_{CC}$ + 0.3 V dc; $V_{IH}$ (max) = $V_{CC}$ + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

**DC CHARACTERISTICS**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input Leakage Current (All Inputs, $V_{in}$ = 0 to $V_{CC}$) | $I_{lkg(I)}$ | — | ± 1.0 | µA |
| Output Leakage Current (G = $V_{IH}$) | $I_{lkg(O)}$ | — | ± 1.0 | µA |
| AC Supply Current (G = $V_{IH}$, E = $V_{IL}$, $I_{out}$ = 0 mA, All Inputs = $V_{IL}$ or $V_{IH}$, $V_{IL}$ = 0.0 V and $V_{IH}$ ≥ 3.0 V, Cycle Time ≥ $t_{KHKH}$ min) | $I_{CCA5}$<br>$I_{CCA7}$ | — | 310<br>290 | mA |
| AC Standby Current (E = $V_{IH}$, $I_{out}$ = 0 mA, All Inputs = $V_{IL}$ and $V_{IH}$, $V_{IL}$ = 0.0 V and $V_{IH}$ ≥ 3.0 V, Cycle Time ≥ $t_{KHKH}$ min) | $I_{SB1}$ | — | 95 | mA |
| Output Low Voltage ($I_{OL}$ = + 8.0 mA) | $V_{OL}$ | — | 0.4 | V |
| Output High Voltage ($I_{OH}$ = – 4.0 mA) | $V_{OH}$ | 2.4 | 3.3 | V |

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible i486 and Pentium bus cycles.

**CAPACITANCE** (f = 1.0 MHz, dV = 3.0 V, $T_A$ = 25°C, Periodically Sampled Rather Than 100% Tested)

| Parameter | Symbol | Typ | Max | Unit |
|---|---|---|---|---|
| Input Capacitance (All Pins Except DQ0 – DQ17) | $C_{in}$ | 4 | 5 | pF |
| Input/Output Capacitance (DQ0 – DQ17) | $C_{I/O}$ | 6 | 8 | pF |

## AC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC}$ = 5.0 V ± 5% $T_A$ = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 3 ns

Output Timing Reference Level . . . . . 1.5 V
Output Load . . . . . See Figure 1a Unless Otherwise Noted

**READ/WRITE CYCLE TIMING** (See Notes 1, 2, 3, and 4)

| Parameter | Symbol | MCM67C618A–5 | | MCM67C618A–7 | | Unit | Notes |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| Cycle Time | $t_{KHKH}$ | 10 | — | 12.5 | — | ns | |
| Clock Access Time | $t_{KHQV}$ | — | 5 | — | 7 | ns | 5 |
| Output Enable to Output Valid | $t_{GLQV}$ | — | 5 | — | 5 | ns | |
| Clock High to Output Active | $t_{KHQX1}$ | 0 | — | 0 | — | ns | |
| Clock High to Output Change | $t_{KHQX2}$ | 2 | — | 2 | — | ns | |
| Output Enable to Output Active | $t_{GLQX}$ | 0 | — | 0 | — | ns | |
| Output Disable to Q High–Z | $t_{GHQZ}$ | — | 6 | — | 6 | ns | 6 |
| Clock High to Q High–Z | $t_{KHQZ}$ | 2 | 6 | 2 | 6 | ns | |
| Clock High Pulse Width | $t_{KHKL}$ | 4.5 | — | 5 | — | ns | |
| Clock Low Pulse Width | $t_{KLKH}$ | 4.5 | — | 5 | — | ns | |
| Setup Times: Address<br>Address Status<br>Data In<br>Write<br>Address Advance<br>Chip Enable | $t_{AVKH}$<br>$t_{ADSVKH}$<br>$t_{DVKH}$<br>$t_{WVKH}$<br>$t_{ADVVKH}$<br>$t_{EVKH}$ | 2.5 | — | 2.5 | — | ns | 7 |
| Hold Times: Address<br>Address Status<br>Data In<br>Write<br>Address Advance<br>Chip Enable | $t_{KHAX}$<br>$t_{KHADSX}$<br>$t_{KHDX}$<br>$t_{KHWX}$<br>$t_{KHADVX}$<br>$t_{KHEX}$ | 0.5 | — | 0.5 | — | ns | 7 |

NOTES:
1. In setup and hold times, W (write) refers to either one or both byte write enables $\overline{LW}$ and $\overline{UW}$.
2. A read cycle is defined by UW and LW high or ADSP low for the setup and hold times. A write cycle is defined by $\overline{LW}$ or $\overline{UW}$ low and $\overline{ADSP}$ high for the setup and hold times.
3. All read and write cycle timings are referenced from K or $\overline{G}$.
4. G is a don't care when UW or LW is sampled low.
5. Maximum access times are guaranteed for all possible i486 and Pentium external bus cycles.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1b. This parameter is sampled rather than 100% tested. At any given voltage and temperature, $t_{KHQZ}$ max is less than $t_{KHQZ1}$ min for a given device and from device to device.
7. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of K whenever $\overline{ADSP}$ or $\overline{ADSC}$ is low, and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is enabled. Chip enable must be valid at each rising edge of clock for the device (when $\overline{ADSP}$ or $\overline{ADSC}$ is low) to remain enabled.

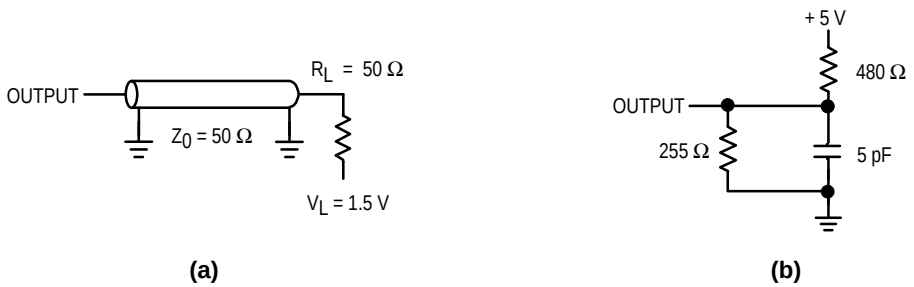
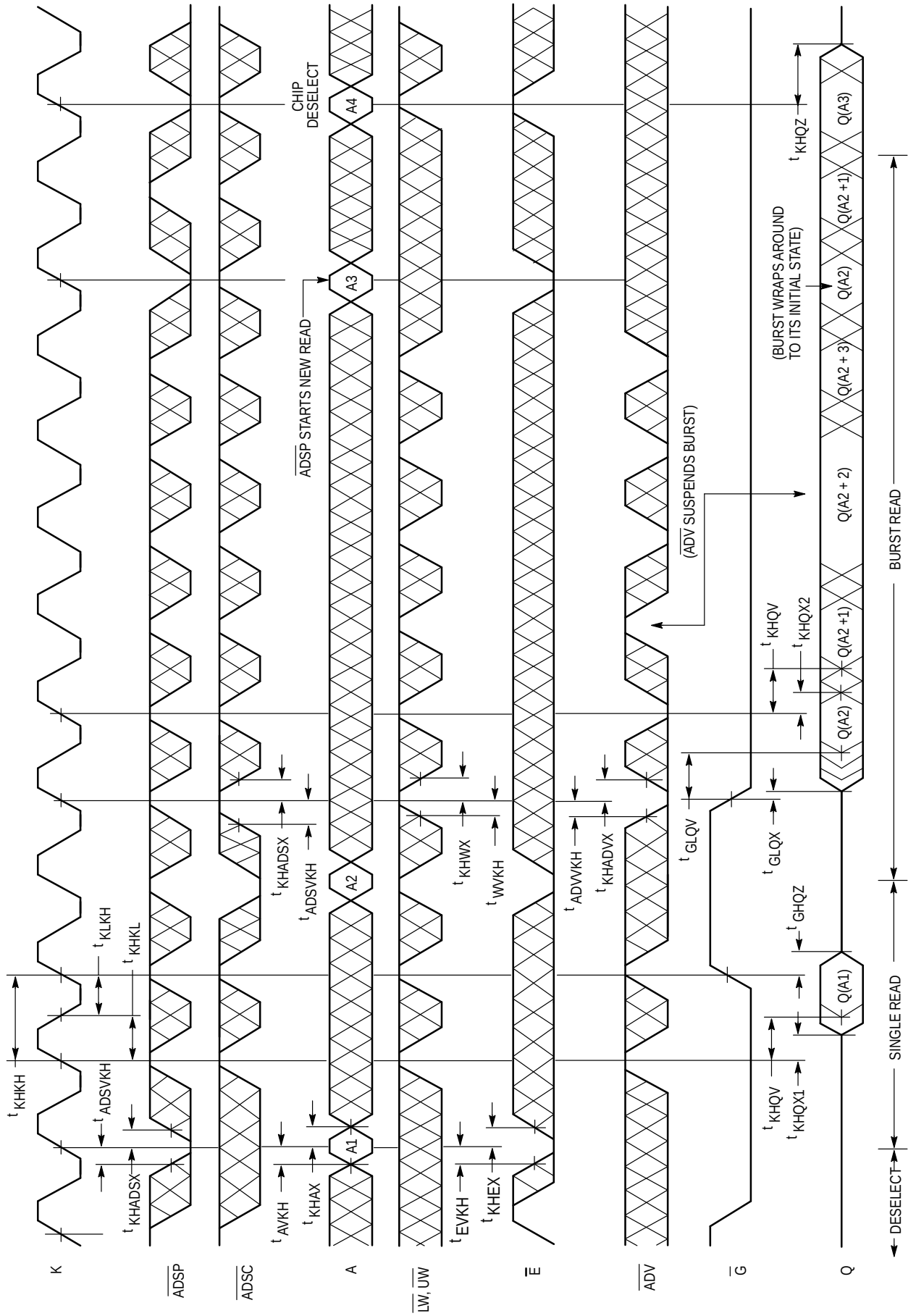
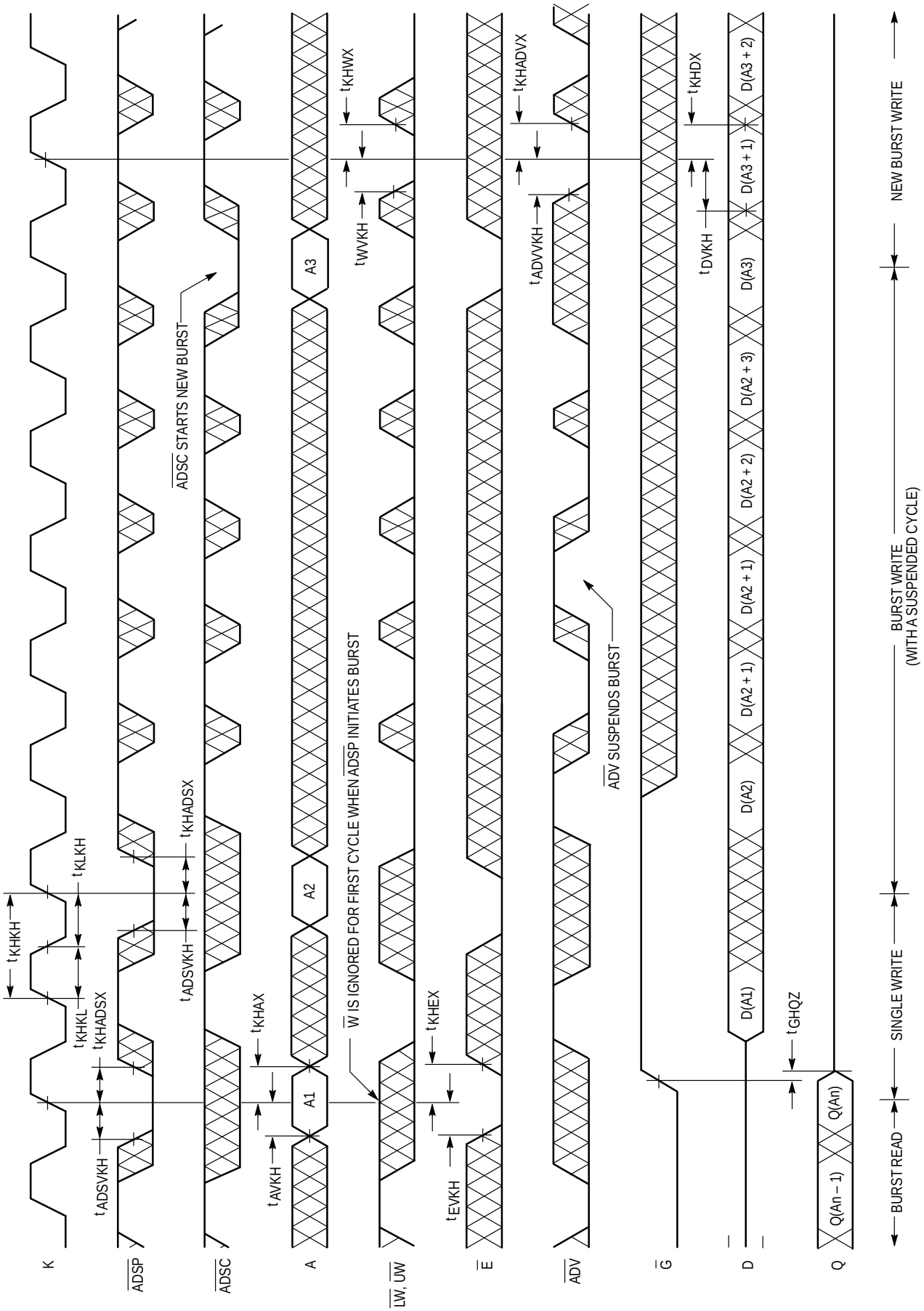



**Figure 1. Test Loads**

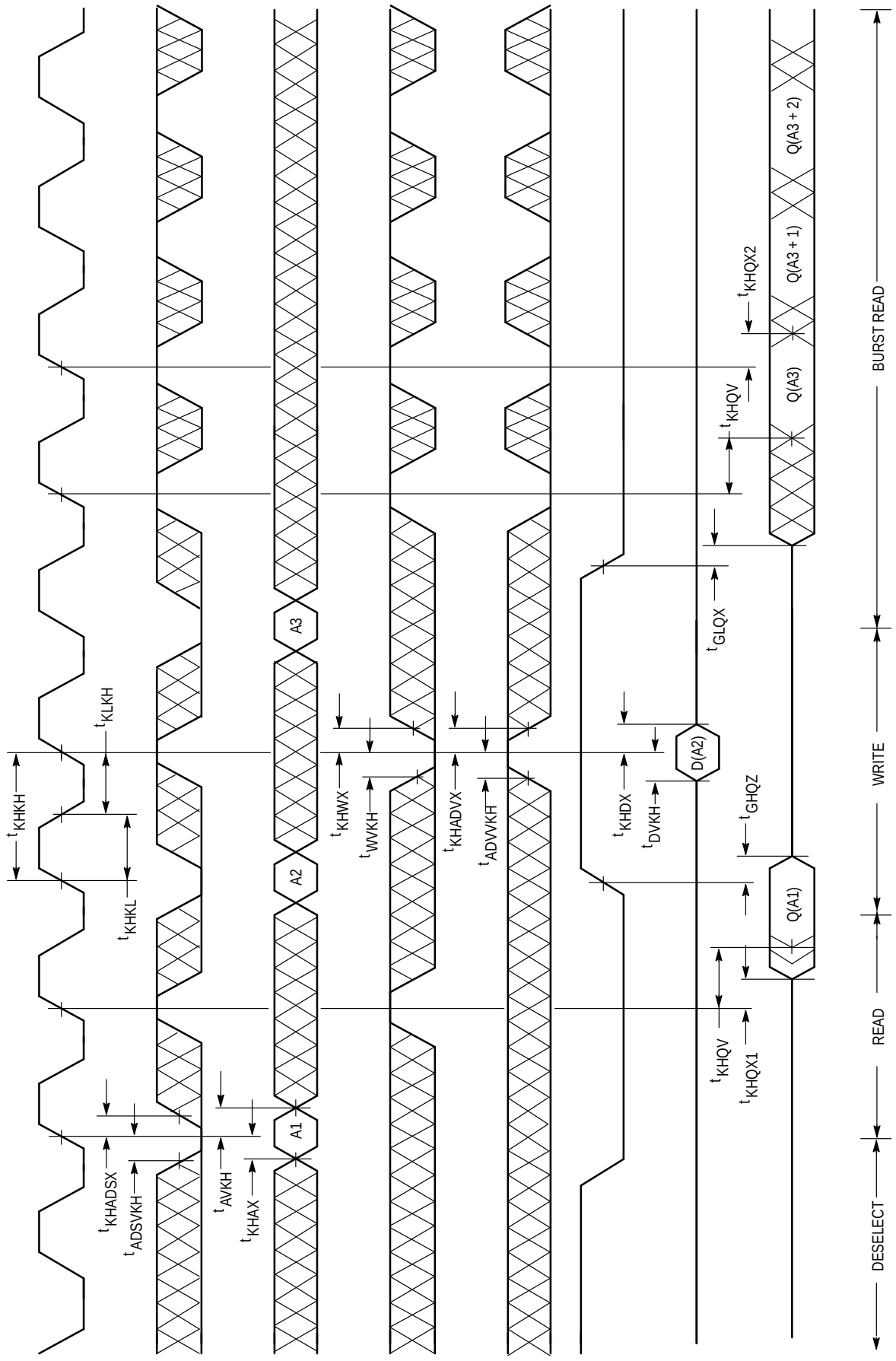
**READ CYCLES**


K
ADSP
ADSC
A
LW, UW
E
ADV
G
Q
tKHKH
tKLKH
tKHKL
tADSVKH
tKHADSX
tAVKH
tKHAX
tKHADSX
tADSVKH
tEVKH
tKHEX
tKHWX
tWVKH
tADVVKH
tKHADVX
tGLQV
tGLQX
tGHQZ
tKHQV
tKHQX1
tKHQV
tKHQX2
tKHQZ
A1
A2
A3
A4
CHIP DESELECT
ADSP STARTS NEW READ
(ADV SUSPENDS BURST)
(BURST WRAPS AROUND TO ITS INITIAL STATE)
Q(A1)
Q(A2)
Q(A2 +1)
Q(A2 + 2)
Q(A2 + 3)
Q(A2)
Q(A2 +1)
Q(A3)
DESELECT
SINGLE READ
BURST READ

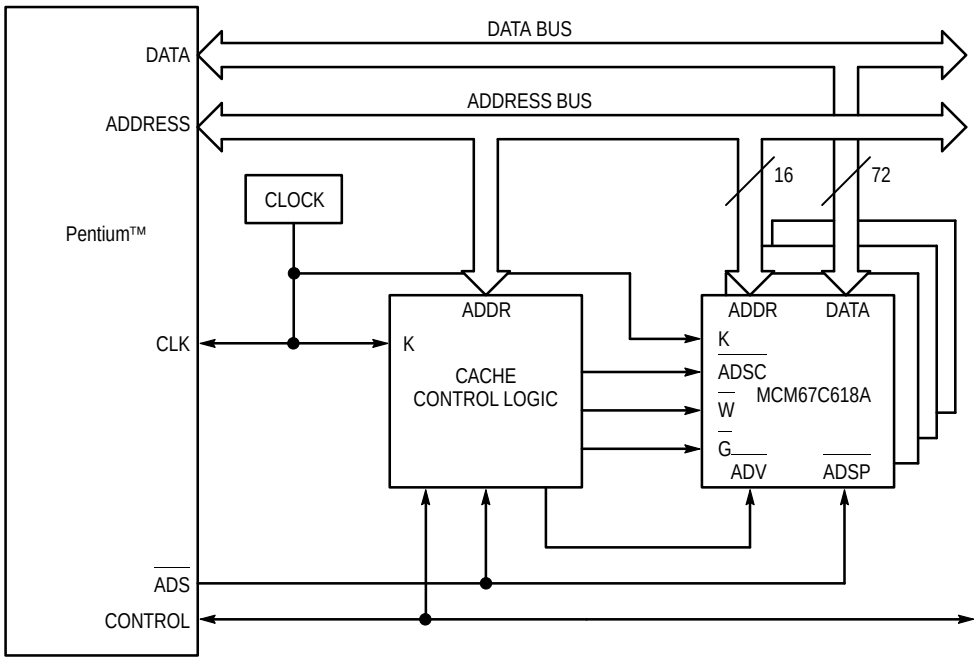
## WRITE CYCLES



**COMBINATION READ/WRITE CYCLES ($\overline{E}$ low, $\overline{ADSC}$ high)**



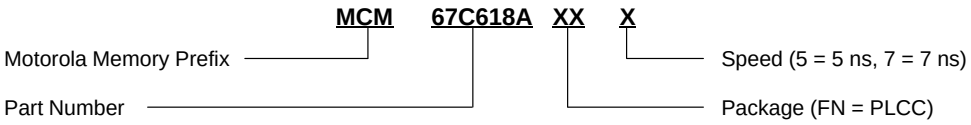
## APPLICATION EXAMPLE




512K Byte Burstable, Secondary Cache Using
Four MCM67C618AFN7s With a 75 MHz (bus speed) Pentium

**Figure 2**

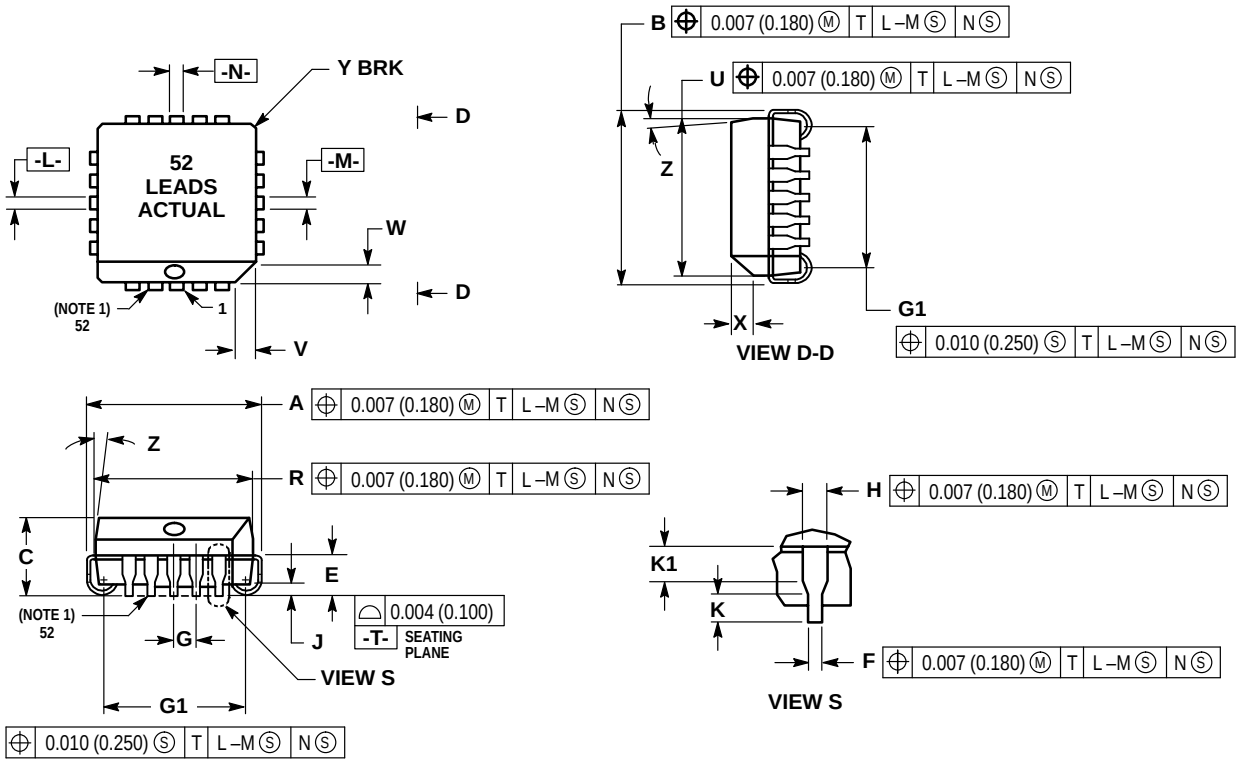
## ORDERING INFORMATION
**(Order by Full Part Number)**




Full Part Numbers — MCM67C618AFN5 MCM67C618AFN7

## PACKAGE DIMENSIONS

**FN PACKAGE**
**52–LEAD PLCC**
**CASE 778–02**




NOTES:
1. **DUE TO SPACE LIMITATION, CASE 778-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 52 LEADS.**
2. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.
7. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
8. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.785 | 0.795 | 19.94 | 20.19 |
| B | 0.785 | 0.795 | 19.94 | 20.19 |
| C | 0.165 | 0.180 | 4.20 | 4.57 |
| E | 0.090 | 0.110 | 2.29 | 2.79 |
| F | 0.013 | 0.019 | 0.33 | 0.48 |
| G | 0.050 BSC | | 1.27 BSC | |
| H | 0.026 | 0.032 | 0.66 | 0.81 |
| J | 0.020 | — | 0.51 | — |
| K | 0.025 | — | 0.64 | — |
| R | 0.750 | 0.756 | 19.05 | 19.20 |
| U | 0.750 | 0.756 | 19.05 | 19.20 |
| V | 0.042 | 0.048 | 1.07 | 1.21 |
| W | 0.042 | 0.048 | 1.07 | 1.21 |
| X | 0.042 | 0.056 | 1.07 | 1.42 |
| Y | — | 0.020 | — | 0.50 |
| Z | 2° | 10° | 2° | 10° |
| G1 | 0.710 | 0.730 | 18.04 | 18.54 |
| K1 | 0.040 | — | 1.02 | — |

**How to reach us:**

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