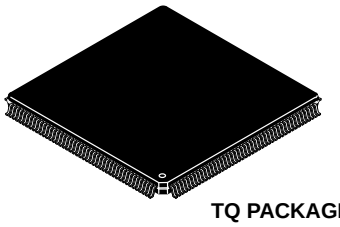
MCM69Q536

Advance Information

32K x 36 Bit Synchronous Separate I/O SRAM



TQ PACKAGE
176 LEAD TQFP
CASE 1101–01

The Motorola MCM69Q536 is a 1 Megabit static random access memory, organized as 32K words of 36 bits. It features separate data input and data output buffers and incorporates input and output registers on board with high speed SRAM.

The MCM69Q536 allows the user to perform transparent writes and data pass through. Two data bus ports are provided — a data input (D) and a data output (Q) port.

The synchronous design allows for precise cycle control with the use of an external single clock (K). Address port, data input (D0 – D35), data output (Q0 – Q35), write enable (W), chip enables (E1, E2), and pass–through enable (PT) are registered on the rising edge of clock (K).

Any given cycle operates on only one address. However, for any cycle, reads and writes can be intermixed. Thus, one can perform a read, a write, or a combination read/write during any one cycle. For a combination read/write, the contents of the array are read before the new data is written.

By using the pass–through function, the output port Q can be made to reflect either the contents of the array or the data presented to the input port D. For read/write or a read cycle with G low, the Q port will output the contents of the array. However, if PT is asserted, the Q port will instead output the data presented at the D input port.

- Single 3.3 V ± 5% Power Supply
- Fast Access Times: 6/8/10 ns Max
- Sustained Throughput of 2.98 Gigabits/Second
- Single Clock Operation
- Address, Data Input, E1, E2, PT, W, and Data Output Registers on Chip
- 83 MHz Maximum Clock Cycle Time
- Self Timed Write
- Separate Data Input and Data Output Pins
- Pass–Through Feature
- Asynchronous Output Enable (G)
- LVTTL Compatible I/O
- No Dead Cycles Required for Reads after Writes or for Writes after Reads
- 176 Pin TQFP Package
- Simultaneous Reads and Writes

Suggested Applications

— ATM — Ethernet Switches — Routers
— Cell/Frame Buffers — SNA Switches — Shared Memory

Product Family Configurations

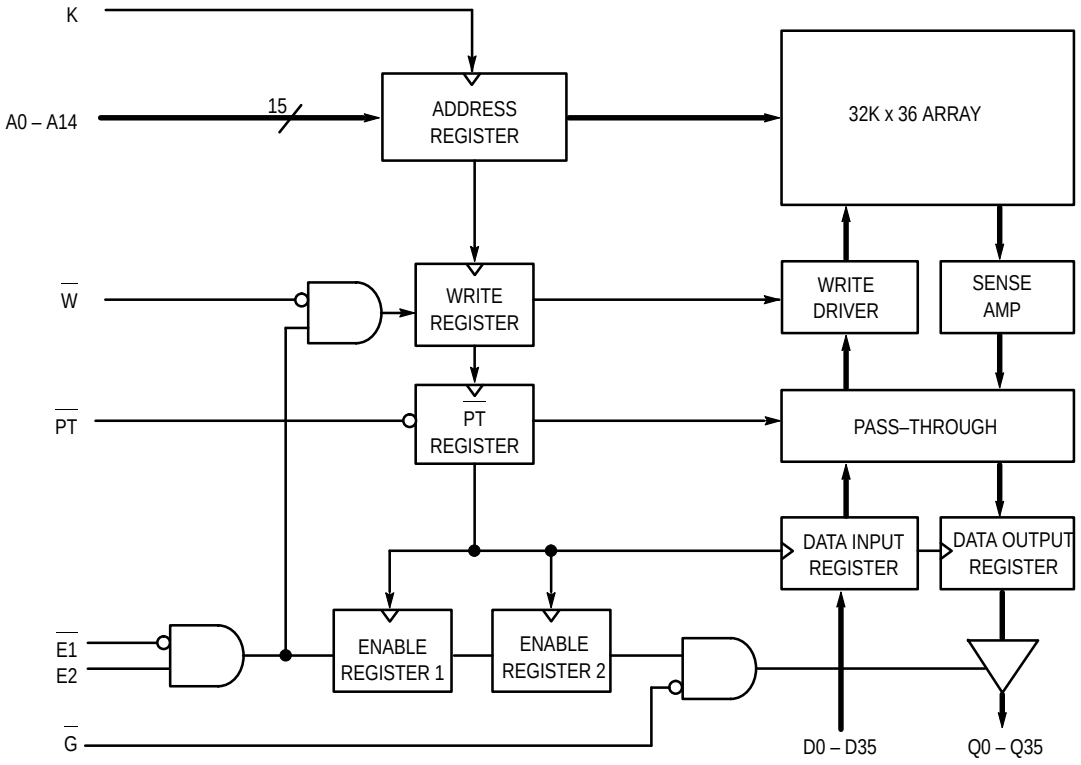
Part Number	Dual Address	Single Address	Dual I/O	Separate I/O
MCM69D536	✓	Note 1	✓	Note 2
MCM69D618	✓	Note 1	✓	Note 2
MCM69Q536		✓		✓
MCM69Q618		✓		✓
MCM67Q709		✓		✓
MCM67Q909		✓		✓

NOTES:
1. Tie AX and AY address ports together for the part to function as a single address part.
2. Tie GX high for DQX to be inputs and tie WY high and GY low for DQY to be outputs.

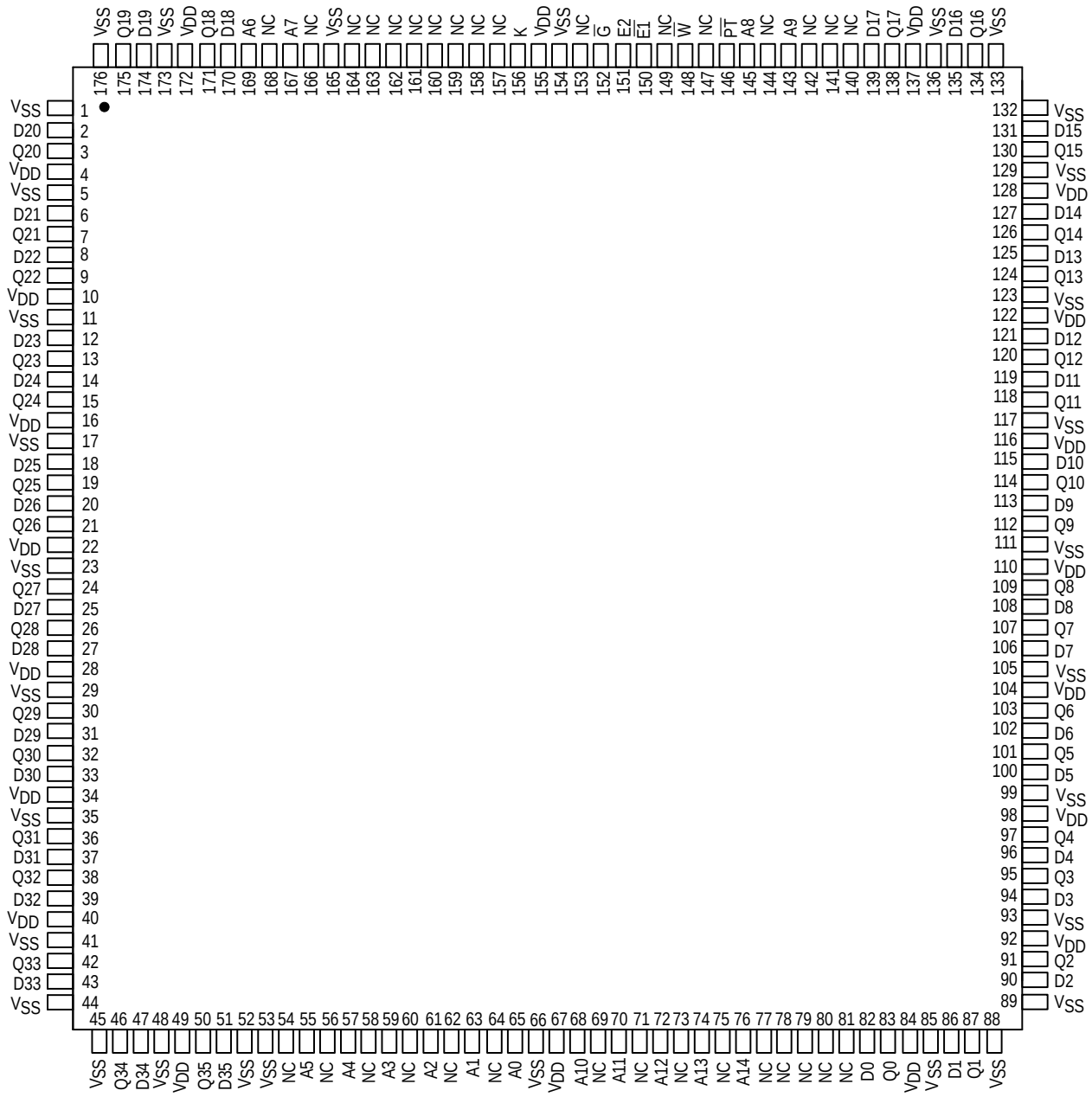
This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 3
11/20/97

BLOCK DIAGRAM



PIN ASSIGNMENT



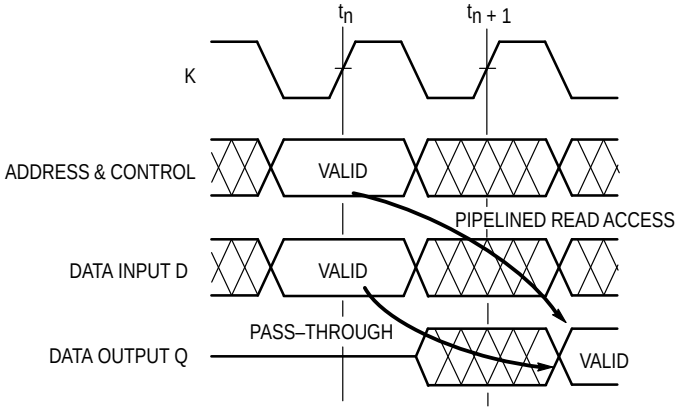
PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
55, 57, 59, 61, 63, 65, 68, 70, 72, 74, 76, 143, 145, 167, 169	A0 – A14	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
2, 6, 8, 12, 14, 18, 20, 25, 27, 31, 33, 37, 39, 43, 47, 51, 82, 86, 90, 94, 96, 100, 102, 106, 108, 113. 115, 119, 121, 125, 127, 131, 135, 139, 170, 174	D0 – D35	Input	Synchronous Data Input.
150	E1	Input	Synchronous Chip Enable: Active low for depth expansion.
151	E2	Input	Synchronous Chip Enable: Active high for depth expansion.
152	G	Input	Asynchronous Output Enable Input: Low — enables output buffers (Qx pins). High — Qx pins are high impedance.
156	K	Input	Clock: This signal registers the address, data in, and all control signals except G.
146	$\overline{PT}$	Input	Pass–through enable: Synchronous.
3, 7, 9, 13, 15, 19, 21, 24, 26, 30, 32, 36, 38, 42, 46, 50, 83, 87, 91, 95, 97, 101, 103, 107, 109, 112, 114, 118, 120, 124, 126, 130, 143, 138, 171, 175	Q0 – Q35	Output	Synchronous Data Output.
148	W	Input	Synchronous Write.
4, 10, 16, 22, 28, 34, 40, 49, 67, 84, 98, 104, 110, 116, 122, 128, 137, 155, 172	V_{DD}	Supply	+ 3.3 V Power Supply.
1, 5, 11, 17, 23, 29, 35, 41, 44, 45, 48, 52, 53, 66, 85, 88, 89, 93, 99, 105, 111, 117, 123. 129, 132, 133, 136, 154, 165, 173, 176	V_{SS}	Supply	Ground.
54, 56, 58, 60, 62, 64, 69, 71, 73, 75, 77 – 81, 140, 141, 142, 144, 147, 149, 153, 157 – 164, 166, 168	NC	—	No Connection: There is no connection to the chip.

TRUTH TABLE

Operation	Input at t_n Clock					Result from t_{n+1} Clock	Notes
	E1	E2	W	PT	Data Input D	Data Output Q	
Write and Pass–Through	L	H	L	L	D written to A	D data appears	1
Write/Read	L	H	L	H	D written to A	Q out from A	2
Pass–Through	L	H	H	L	D data	D data appears	3
Read	L	H	H	H	Don’t Care	Q out from A	4
Deselected	X	L	X	X	Don’t Care	Q is high–Z	5
Deselected	H	X	X	X	Don’t Care	Q is high–Z	6

NOTES:
1. Write D to array and output D at Q.
2. Output contents of array to Q then write D to array.
3. Output D at Q. Do not write.
4. Output contents of array to Q. Do not write.
5. No operation.
6. No operation.



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Voltage Relative to V_{SS} for Any Pin Except V_{DD}	V_{in}, V_{out}	– 0.5 to V_{DD} + 0.5	V
Output Current	I_{out}	± 20	mA
Power Dissipation	P_D	TBD	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This is a synchronous device. All synchronous inputs must meet specified setup and hold times with stable logic levels for ***ALL*** rising edges of clock (K) while the device is selected.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

PACKAGE THERMAL CHARACTERISTICS (See Note 1)

Rating		Symbol	TQFP	Unit	Notes
Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	40 35	°C/W	2
Junction to Board (Bottom)		$R_{\theta JB}$	23	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	9	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)		V_{DD}	3.135	3.465	V
Input High Voltage		V_{IH}	2.0	V_{DD} + 0.5**	V
Input Low Voltage		V_{IL}	– 0.5*	0.8	V
Input Leakage Current (All Inputs, V_{in} = 0 to V_{DD})		$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current (E = V_{IH}, V_{out} = 0 to V_{DD})		$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current (I_{out} = 0 mA) (V_{DD} = max, f = f_{max})	MCM69Q536–6 ns MCM69Q536–8 ns MCM69Q536–10 ns	I_{DDA}	— — —	TBD TBD TBD	mA
CMOS Standby Supply Current (Deselected, Clock (K) Cycle Time ≥ t_{KHKH}, All Inputs Toggling at CMOS Levels V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{DD} – 0.2 V)	MCM69Q536–6 ns MCM69Q536–8 ns MCM69Q536–10 ns	I_{SB1}	— — —	TBD TBD TBD	mA
Output Low Voltage (I_{OL} = + 8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)		V_{OH}	2.4	V_{DD}	V

* V_{IL} ≥ –1.5 V for t ≤ t_{KHKH}/2.
** V_{IH} ≤ V_{DD} + 1.0 V for t ≤ t_{KHKH}/2.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 0 to + 70°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address and Data Input Capacitance	C_{in}	6	pF
Control Pin Input Capacitance	C_{in}	6	pF
Output Capacitance	C_{out}	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 3 ns

Output Timing Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1 Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM69Q536–6		MCM69Q536–8		MCM69Q536–10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	12	—	15	—	20	—	ns	1
Clock Access Time	t_{KHQV}	—	6	—	8	—	10	ns	2
Clock Low Pulse Width	t_{KLKH}	4	—	6	—	8	—	ns	
Clock High Pulse Width	t_{KHKL}	4	—	6	—	8	—	ns	
Clock High to Data Output Invalid	t_{KHQX}	0	—	0	—	0	—	ns	
Clock High to Data Output High–Z	t_{KHQZ}	—	5	—	6	—	7	ns	4
Output Enable to Output Valid	t_{GLQV}	—	6	—	8	—	10	ns	
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	4
Output Disable to Output High–Z	t_{GHQZ}	—	5	—	6	—	7	ns	4
Setup Times: A0 – A15 W PT E1, E2 D0 – D17	t_{AVKH} t_{WVKH} t_{PTVKH} t_{EVKH} t_{DVKH}	2.5	—	3	—	3	—	ns	3
Hold Times: A0 – A15 W PT E1, E2 D0 – D17	t_{KHAX} t_{KHWX} t_{KHPTX} t_{KHEX} t_{KHDX}	0.5	—	2	—	2	—	ns	3

NOTES:
1. All read and write cycles are referenced from K.
2. Valid data from Clock High will be the data stored at the address or the last valid read cycle.
3. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for ***ALL*** rising edges of clock (K) while the device is selected.
4. This parameter is sampled and not 100% tested.

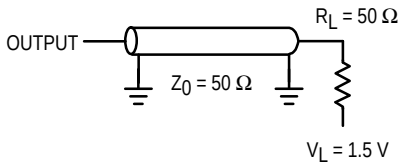
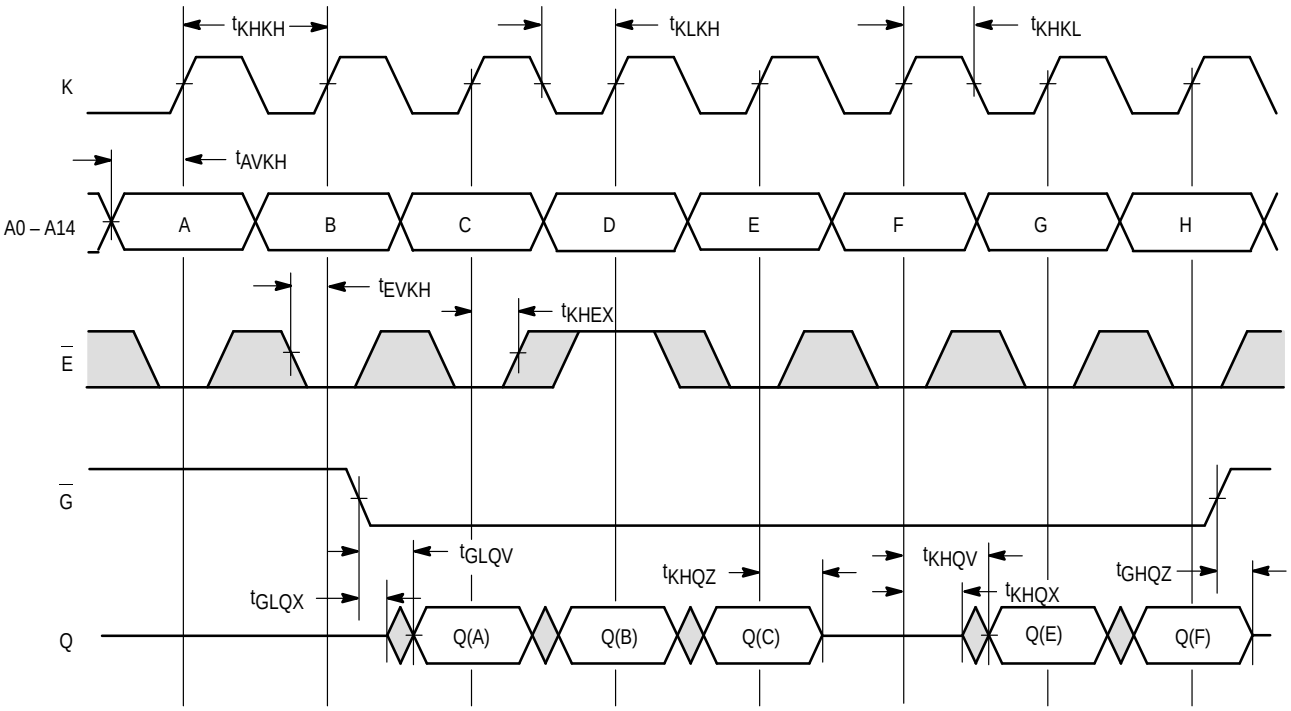


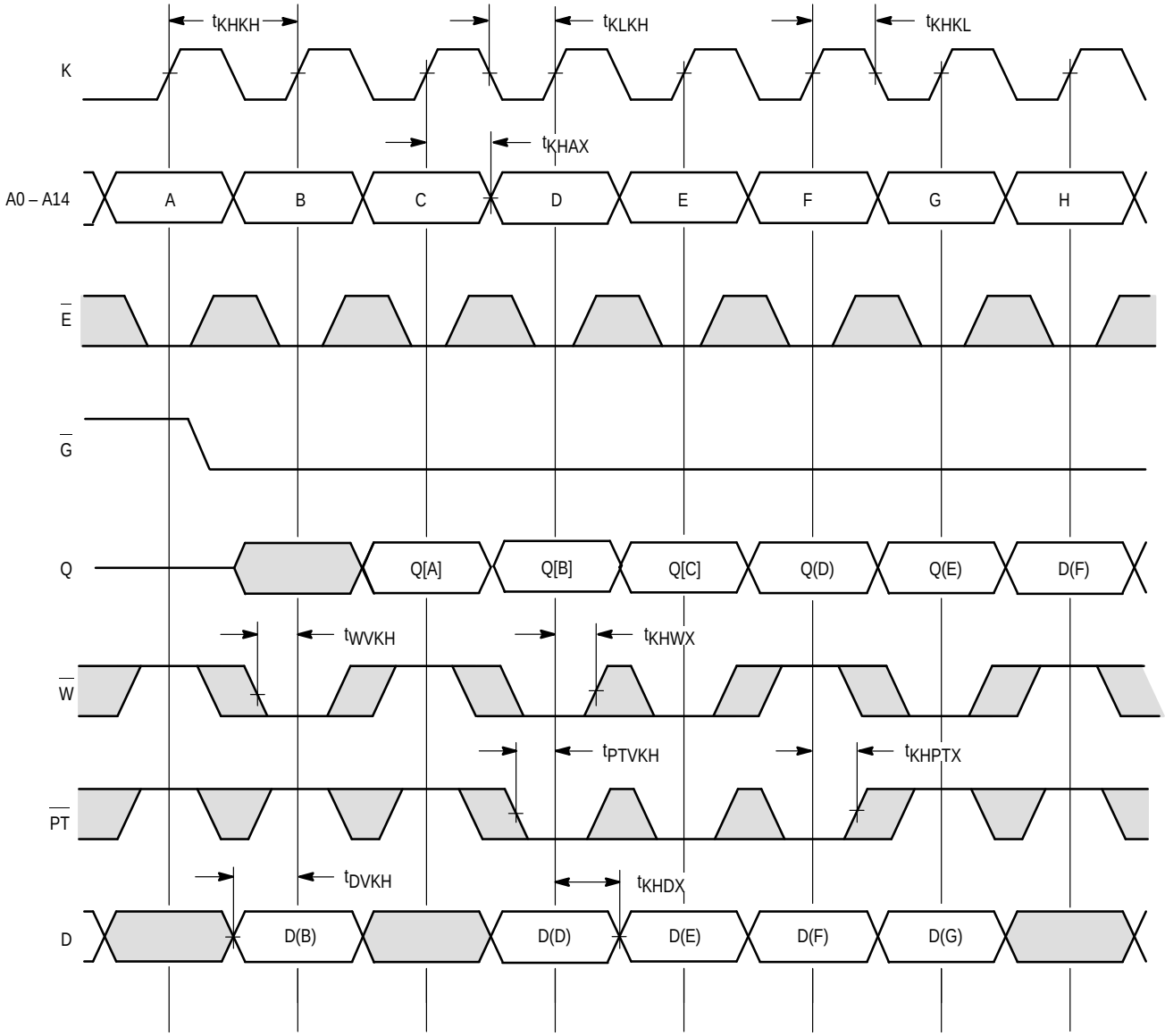
Figure 1. AC Test Load

READ CYCLE TIMING



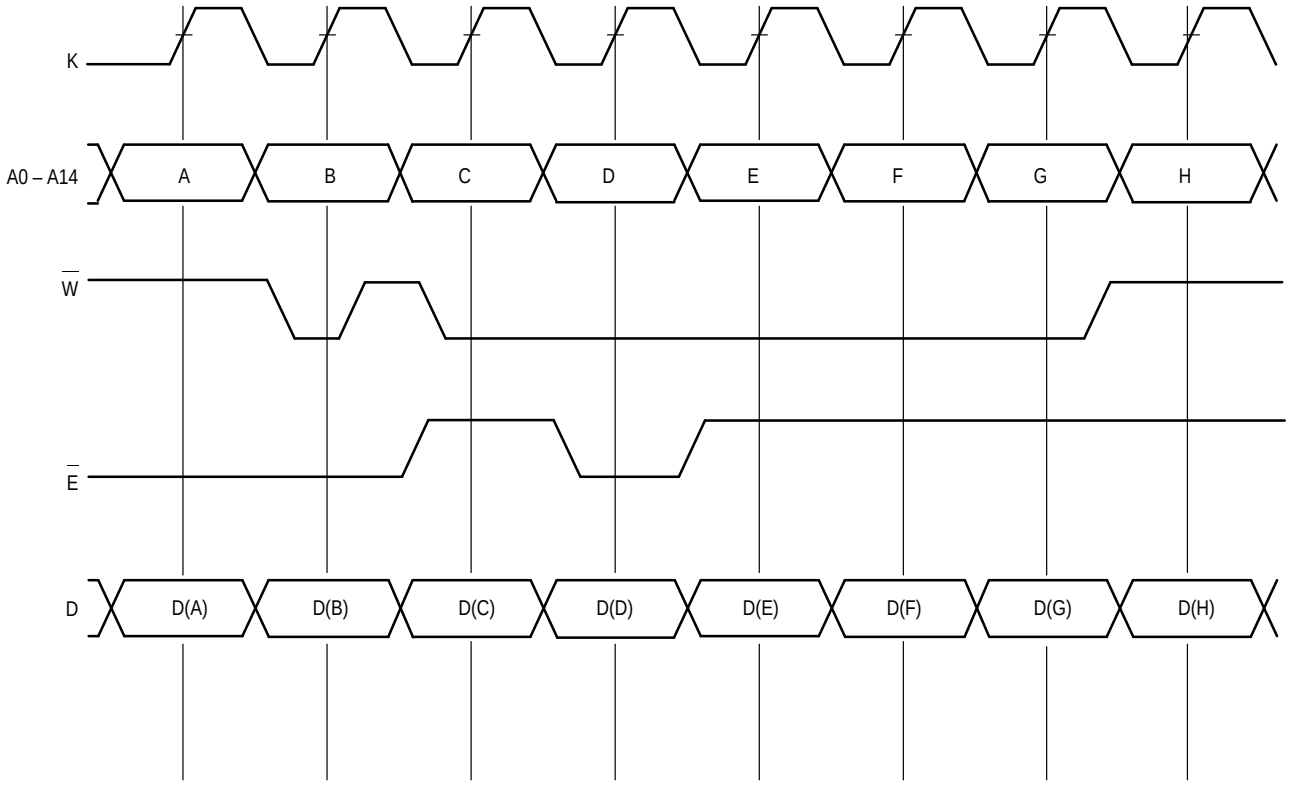
$\overline{E}$ low = $\overline{E1}$ low, E2 high. $\overline{E}$ high = $\overline{E1}$ high or E2 low.

COMBINATION READ/WRITE CYCLE TIMING



NOTES:
1. E low = E1 low and E2 high. E high = E1 high or E2 low.
2. Q[A] = Previous contents of array at address A.
3. Q(A) = Data presented at input port.

$\overline{E}$ CONTROLLED WRITE



NOTES:
1. E low = $\overline{E}$1 low, E2 high. $\overline{E}$ high = $\overline{E}$1 high or E2 low.
2. Only D(B) and D(D) are written to the array.

ORDERING INFORMATION
(Order by Full Part Number)

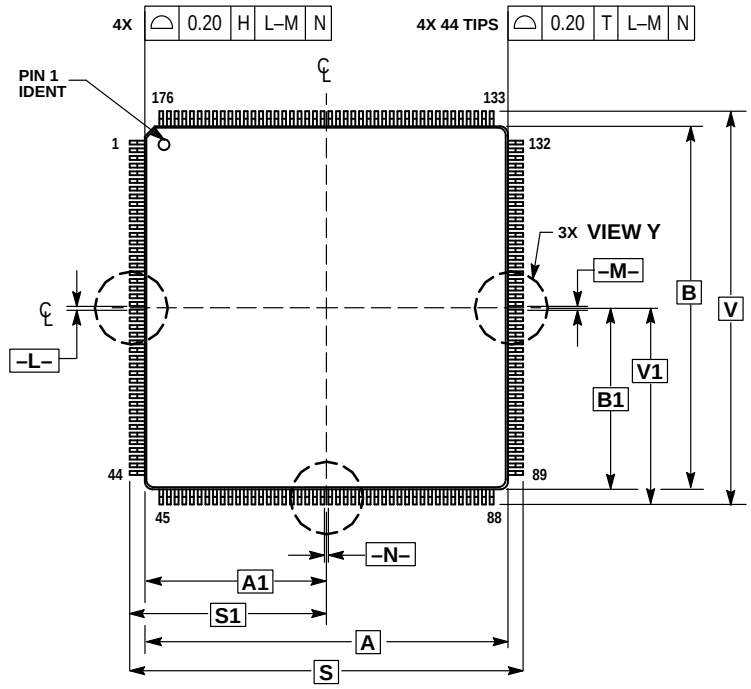
MCM 69Q536 XX XX X

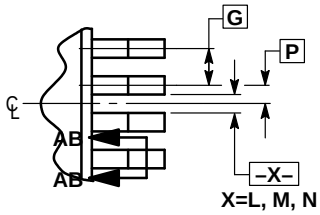
- Motorola Memory Prefix
- Part Number
- Shipping Method (R = Tape and Reel, Blank = Rails)
- Speed (6 = 6 ns, 8 = 8 ns, 10 = 10 ns)
- Package (TQ = TQFP)

Full Part Numbers — MCM69Q536TQ6 MCM69Q536TQ8 MCM69Q536TQ10
MCM69Q536TQ6R MCM69Q536TQ8R MCM69Q536TQ10R

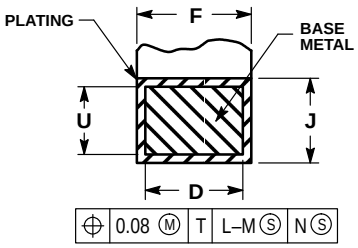
PACKAGE DIMENSIONS

TQFP PACKAGE
176 LEAD
CASE 1101–01

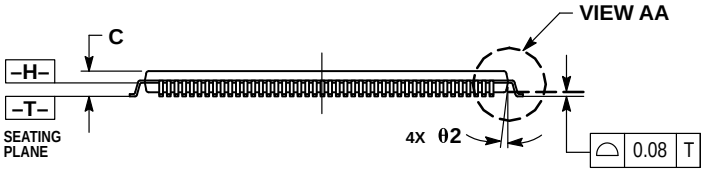


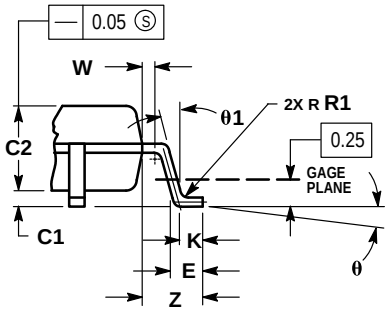


VIEW Y



SECTION AB–AB
ROTATED 90° CLOCKWISE





VIEW AA

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –L–, –M–, AND –N– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –T–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INLCUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35 (0.014) MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD 0.07 (0.003).

	MILLIMETERS	
DIM	MIN	MAX
A	24.00 BSC	
A1	12.00 BSC	
B	24.00 BSC	
B1	12.00 BSC	
C	—	1.60
C1	0.05	—
C2	1.35	1.45
D	0.17	0.23
E	0.45	0.75
F	0.17	0.27
G	0.50 BSC	
J	0.09	0.20
K	0.50 REF	
P	0.25 BSC	
R1	0.10	0.20
S	26.00 BSC	
S1	13.00 BSC	
U	0.09	0.16
V	26.00 BSC	
V1	13.00 BSC	
W	0.20 REF	
Z	1,00 REF	
θ	0°	7°
θ1	0°	—
θ2	12° REF	

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