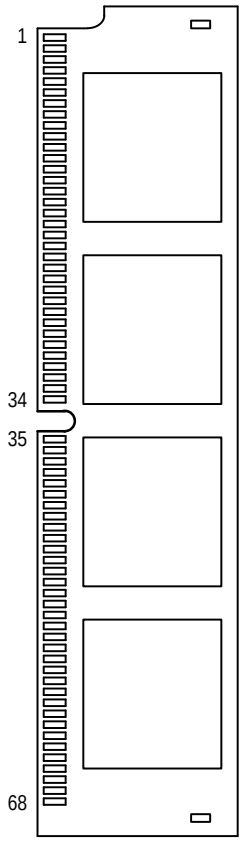
256KB and 512KB BurstRAM™ Secondary Cache Module for Pentium™

MCM72BA32
MCM72BA64

136–LEAD DIMM
CASE 1104–01
TOP VIEW



The MCM72BA32SG and MCM72BA64SG are designed to provide a burstable, high performance, 256K/512K L2 cache for the Pentium microprocessor. The modules are configured as 32K x 72 and 64K x 72 bits in a 136 pin dual readout single inline memory module (DIMM). The module uses four of Motorola's MCM67B518 or MCM67B618 BiCMOS BurstRAMs.

Bursts can be initiated with either address status processor ($\overline{ADSP}$) or address status controller ($\overline{ADSC}$). Subsequent burst addresses are generated internal to the BurstRAM by the burst advance ($\overline{ADV}$) input pin.

Write cycles are internally self timed and are initiated by the rising edge of the clock (K) input. Eight write enables are provided for byte write control.

The cache family is designed to interface with popular Pentium cache controllers with on board TAG.

PD0 – PD2 are reserved for density and speed identification.

- Pentium–style Burst Counter on Board
- Dual Readout SIMM for Circuit Density
- Single 5 V ± 5% Power Supply
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Byte Parity
- Byte Write Capability
- Fast Module Clock Rates: 66 MHz, 60 MHz, 50MHz
- Decoupling Capacitors for each Fast Static RAM
- High Quality Multi–Layer FR4 PWB With Separate Power and Ground Planes
- I/Os are 3.3 V Compatible

BurstRAM is a trademark of Motorola.
Pentium is a trademark of Intel Corp.

REV 2
5/95

PIN ASSIGNMENT
136–LEAD DIMM
TOP VIEW

PD0	1	69	V_{SS}
PD1	2	70	PD2
DQ0	3	71	V_{CC}
DQ1	4	72	DQ2
V_{CC}	5	73	DQ3
DQ4	6	74	DQ5
DQ6	7	75	DQ7
DQP0	8	76	V_{SS}
DQ8	9	77	DQ9
DQ10	10	78	DQ11
V_{SS}	11	79	DQ12
K0	12	80	V_{SS}
V_{SS}	13	81	DQ13
DQ14	14	82	DQ15
V_{CC}	15	83	DQP1
DQ16	16	84	V_{SS}
DQ17	17	85	DQ18
DQ19	18	86	DQ20
DQ21	19	87	DQ22
V_{CC}	20	88	DQ23
DQP2	21	89	V_{SS}
DQ24	22	90	DQ25
DQ26	23	91	DQ27
DQ28	24	92	DQ29
V_{SS}	25	93	DQ30
DQ31	26	94	V_{SS}
DQP3	27	95	$\overline{E0}$
V_{SS}	28	96	$\overline{W1}$
$\overline{W0}$	29	97	$\overline{W3}$
$\overline{W2}$	30	98	$\overline{G0}$
$\overline{ADSP}$	31	99	$\overline{ADSC}$
$\overline{ADV}$	32	100	V_{SS}
V_{CC}	33	101	$\overline{G1}$
$\overline{W4}$	34	102	$\overline{W5}$
$\overline{W6}$	35	103	$\overline{W7}$
DQ32	36	104	$\overline{E1}$
DQ33	37	105	DQ34
V_{SS}	38	106	DQ35
DQ36	39	107	DQ37
DQ38	40	108	V_{CC}
DQ39	41	109	DQP4
DQ40	42	110	DQ41
V_{CC}	43	111	DQ42
DQ43	44	112	DQ44
DQ45	45	113	V_{SS}
DQ46	46	114	DQ47
DQP5	47	115	DQ48
V_{SS}	48	116	DQ49
K1	49	117	V_{SS}
V_{SS}	50	118	DQ50
DQ52	51	119	DQ51
DQ53	52	120	DQ54
DQ55	53	121	DQ56
DQP6	54	122	V_{SS}
V_{CC}	55	123	DQ57
DQ58	56	124	DQ59
DQ60	57	125	DQ61
DQ62	58	126	DQ63
DQP7	59	127	V_{CC}
A0	60	128	A1
A2	61	129	A3
A4	62	130	A5
A6	63	131	A7
A8	64	132	NC
A10	65	133	A9
A12	66	134	A11
A14	67	135	A13
V_{SS}	68	136	A15*

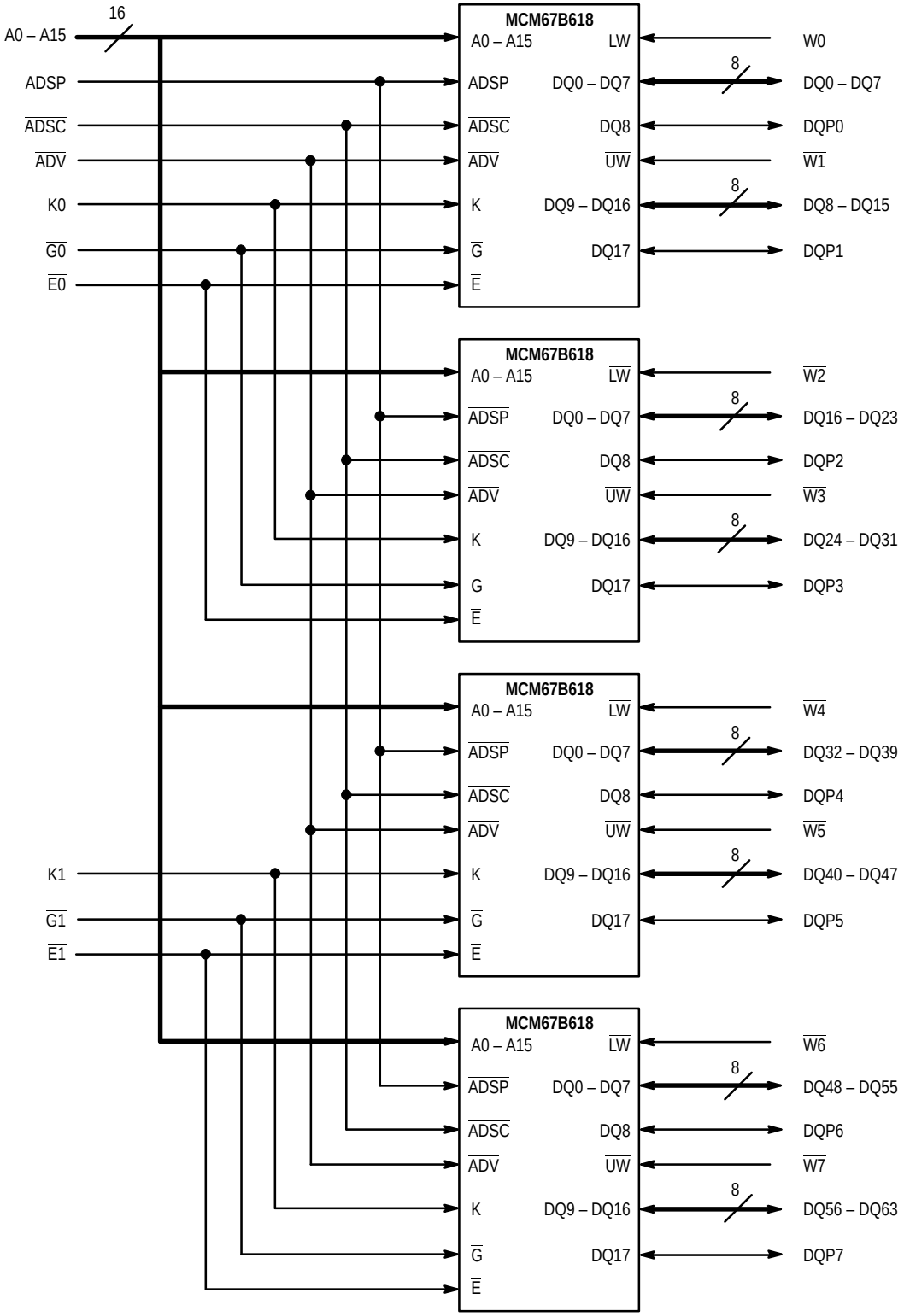
PD2	PD1	PD0	Cache Size	Module
V_{SS}	NC	NC	512KB	72BA64SG66/60
V_{SS}	NC	V_{SS}	512KB	72BA64SG50
V_{SS}	V_{SS}	NC	256KB	72BA32SG66/60
V_{SS}	V_{SS}	V_{SS}	256KB	72BA32SG50

PIN NAMES

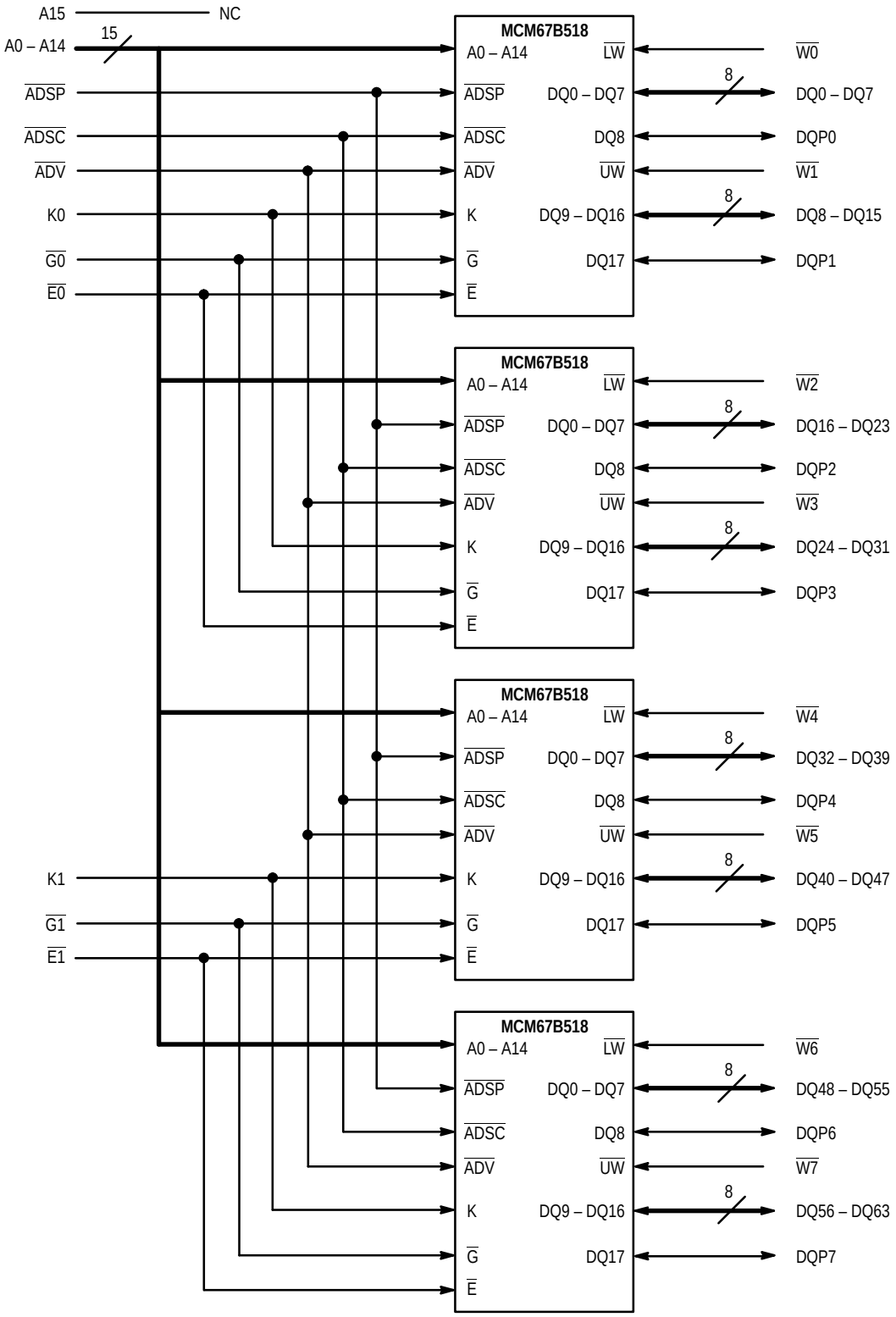
A0 – A15	Address Inputs
K0, K1	Clock
$\overline{W0}$ – $\overline{W7}$	Byte Write
$\overline{E0}$, $\overline{E1}$	Module Enable
$\overline{G0}$, $\overline{G1}$	Module Output Enable
DQ0 – DQ63	Cache Data Input/Output
DQP0 – DQP7	Data Parity Input/Output
$\overline{ADSC}$	Controller Address Status
$\overline{ADSP}$	Processor Address Status
$\overline{ADV}$	Burst Advance
PD0 – PD2	Presence Detect
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

* This pin on the MCM72BA32 is a No Connect (NC)

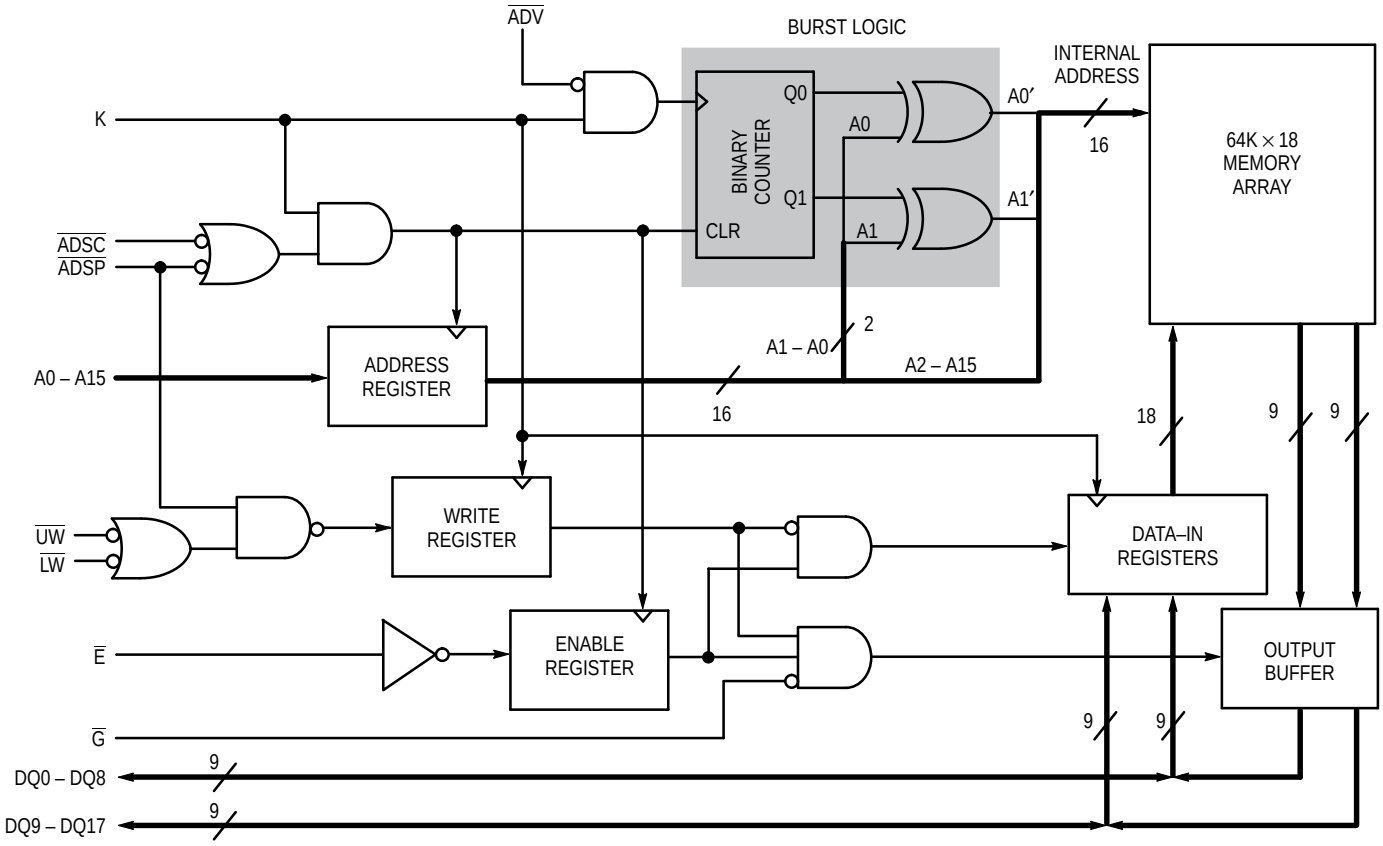
64K x 72 BurstRAM MEMORY MODULE BLOCK DIAGRAM



32K x 72 BurstRAM MEMORY MODULE BLOCK DIAGRAM



MCM67B618 BLOCK DIAGRAM (See Note)



NOTE: All registers are positive–edge triggered. The $\overline{\text{ADSC}}$ or $\overline{\text{ADSP}}$ signals control the duration of the burst and the start of the next burst. When $\overline{\text{ADSP}}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{\text{W}}$ and $\overline{\text{ADSC}}$) is performed using the new external address. Alternatively, an $\overline{\text{ADSP}}$–initiated two cycle WRITE can be performed by asserting $\overline{\text{ADSP}}$ and a valid address on the first cycle, then negating both $\overline{\text{ADSP}}$ and $\overline{\text{ADSC}}$ and asserting $\overline{\text{LW}}$ and/or $\overline{\text{UW}}$ with valid data on the second cycle (see Single Write Cycle in WRITE CYCLES timing diagram).
When $\overline{\text{ADSC}}$ is sampled low (and $\overline{\text{ADSP}}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{\text{W}}$) is performed using the new external address. Chip enable ($\overline{\text{E}}$) is sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{\text{ADV}}$ controls subsequent burst cycles. When $\overline{\text{ADV}}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{\text{ADV}}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**. Write refers to either or both byte write enables ($\overline{\text{LW}}$, $\overline{\text{UW}}$).

BURST SEQUENCE TABLE (See Note)

External Address	A15 – A2	A1	A0
1st Burst Address	A15 – A2	A1	$\overline{\text{A0}}$
2nd Burst Address	A15 – A2	$\overline{\text{A1}}$	A0
3rd Burst Address	A15 – A2	$\overline{\text{A1}}$	$\overline{\text{A0}}$

NOTE: The burst wraps around to its initial state upon completion.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

$\overline{E}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{UW}$ or $\overline{LW}$	K	Address Used	Operation
H	L	X	X	X	L–H	N/A	Deselected
H	X	L	X	X	L–H	N/A	Deselected
L	L	X	X	X	L–H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L–H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L–H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low–to–high transition of clock (K).
3. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out
Read	H	High–Z
Write	X	High–Z — Data In
Deselected	X	High–Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	6.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, $\overline{E}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{CCA66} I_{CCA60} I_{CCA50}	—	1100 1100 1000	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	300	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible Pentium bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Typ	Max	Unit
Input Capacitance	(A0 – A15, $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$)	C_{in}	25	32	pF
Input/Output Capacitance	(DQ0 – DQ63, DQP0 – DQP7)	$C_{I/O}$	8	10	pF
Input Capacitance	(Kx, $\overline{Gx}$, $\overline{Ex}$, $\overline{Wx}$)	C_{in}	12	15	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 3 ns

Output Timing Reference Level . . . . . 1.5 V
Output Load . . . . . See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3) ($\overline{Wx}$ refers to any or all byte write enables)

Parameter	Symbol	MCM72BA64SG66		MCM72BA64SG60		MCM72BA64SG50		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	15	—	16.7	—	20	—	ns	
Clock Access Time	t_{KHQV}	—	9	—	10	—	12	ns	4
Output Enable to Output Valid	t_{GLQV}	—	5	—	5	—	6	ns	
Clock High to Output Active	t_{KHQX1}	6	—	6	—	6	—	ns	
Clock High to Output Change	t_{KHQX2}	3	—	3	—	3	—	ns	
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	
Output Disable to Q High–Z	t_{GHQZ}	2	6	2	6	2	7	ns	5
Clock High to Q High–Z	t_{KHQZ}	—	6	—	6	—	6	ns	
Clock High Pulse Width	t_{KHKL}	5	—	5	—	6	—	ns	
Clock Low Pulse Width	t_{KLKH}	5	—	5	—	6	—	ns	
Setup Times: Address Address Status Data In Write Address Advance Chip Enable	t_{AVKH} t_{ADSVKH} t_{DVKH} t_{WVKH} t_{ADVVKH} t_{EVKH}	2.5	—	2.5	—	2.5	—	ns	6
Hold Times: Address Address Status Data In Write Address Advance Chip Enable	t_{KHAX} t_{KHADSX} t_{KHDX} t_{KHWX} t_{KHADVX} t_{KHEX}	0.5	—	0.5	—	0.5	—	ns	6

NOTES:
1. A read cycle is defined by $\overline{UW}$ and $\overline{LW}$ high or $\overline{ADSP}$ low for the setup and hold times. A write cycle is defined by $\overline{LW}$ or $\overline{UW}$ low and $\overline{ADSP}$ high for the setup and hold times.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. $\overline{G}$ is a don't care when $\overline{UW}$ or $\overline{LW}$ is sampled low.
4. Maximum access times are guaranteed for all possible Pentium external bus cycles.
5. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B. This parameter is sampled rather than 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQZ1} min for a given device and from device to device.
6. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of K whenever $\overline{ADSP}$ or $\overline{ADSC}$ is low, and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is enabled.Chip enable must be valid at each rising edge of clock for the device (when $\overline{ADSP}$ or $\overline{ADSC}$ is low) to remain enabled.

AC TEST LOADS

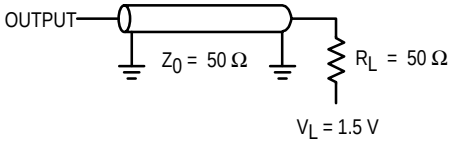


Figure 1A

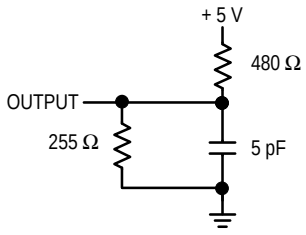
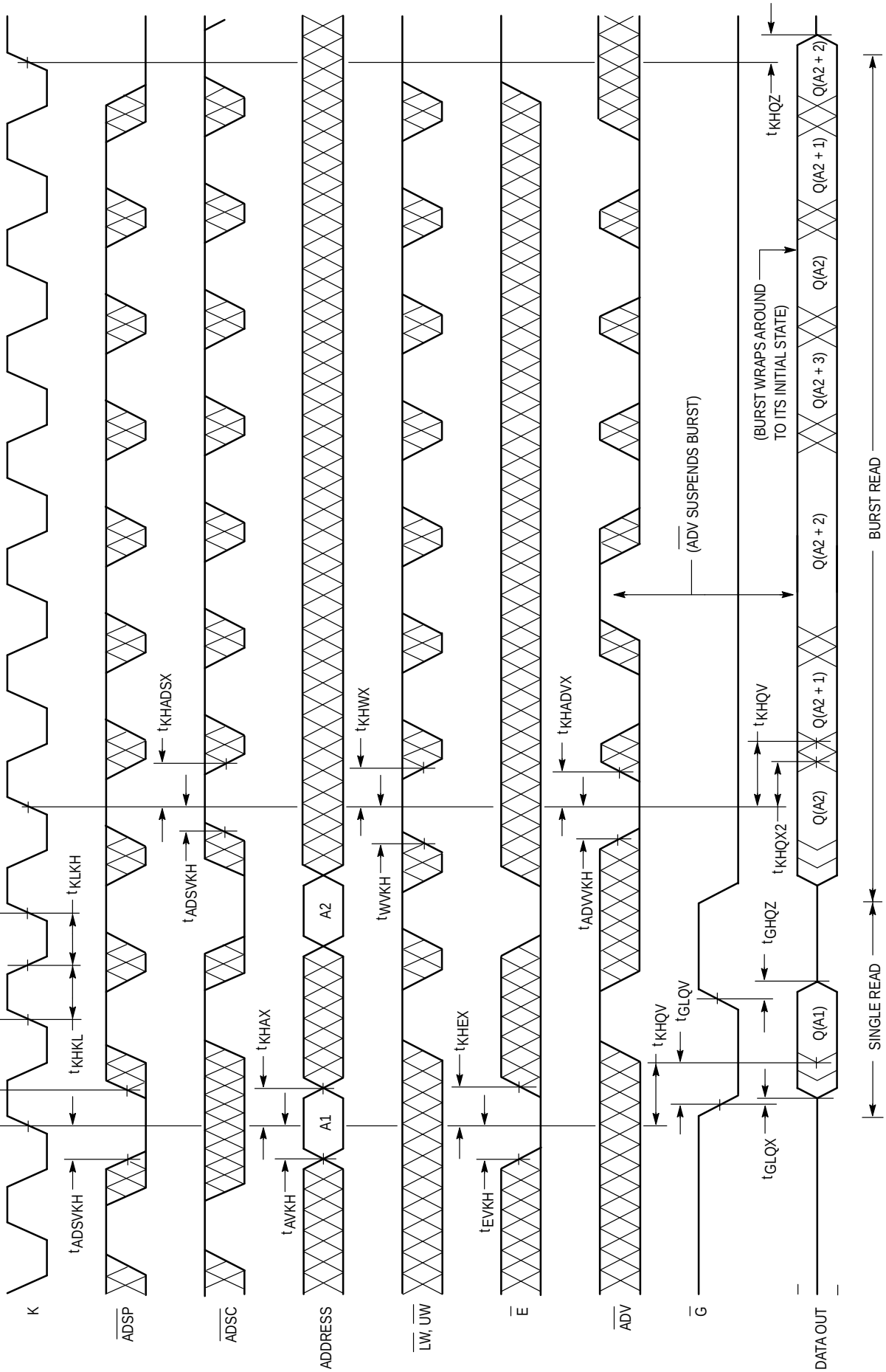


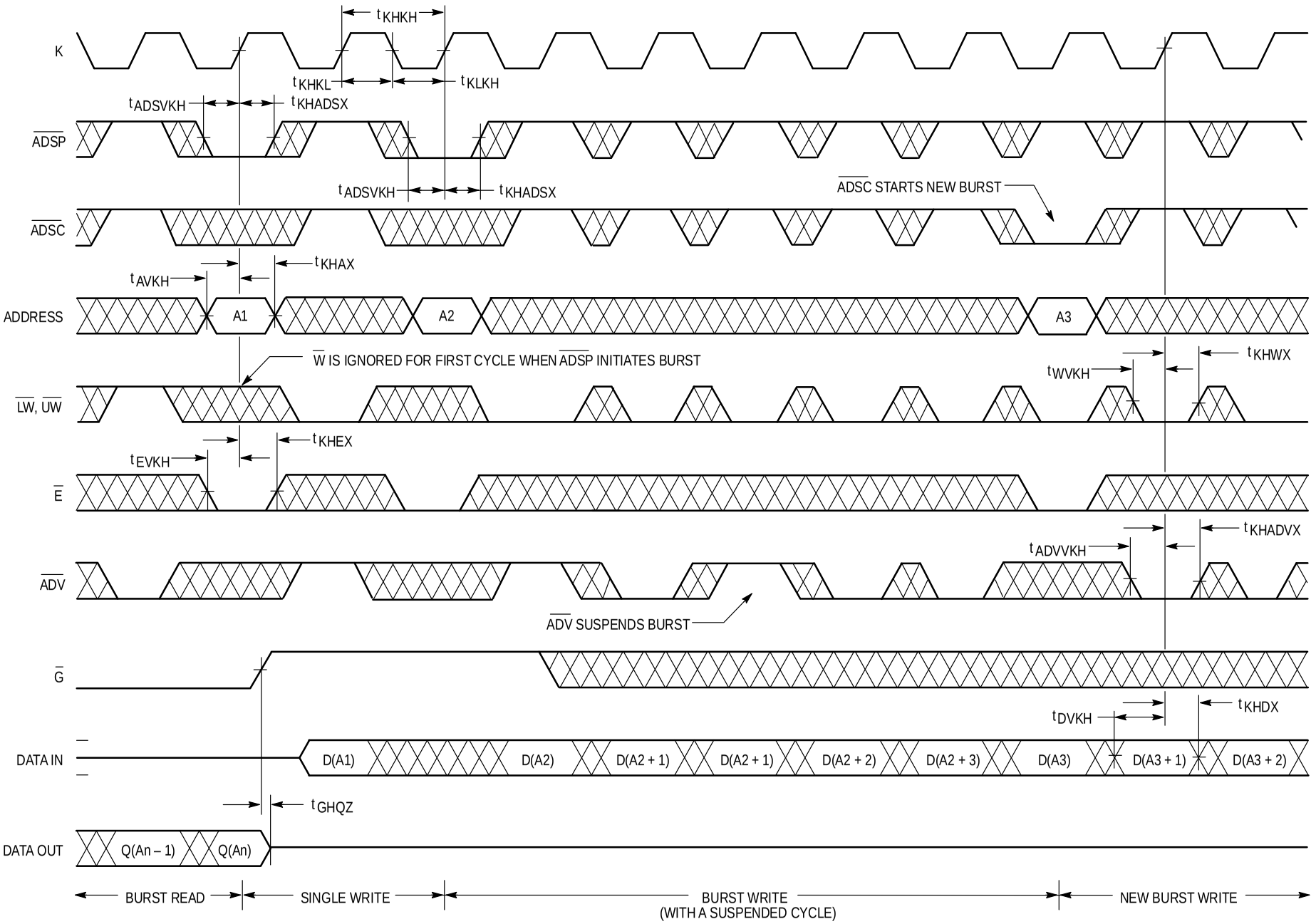
Figure 1B

READ CYCLES

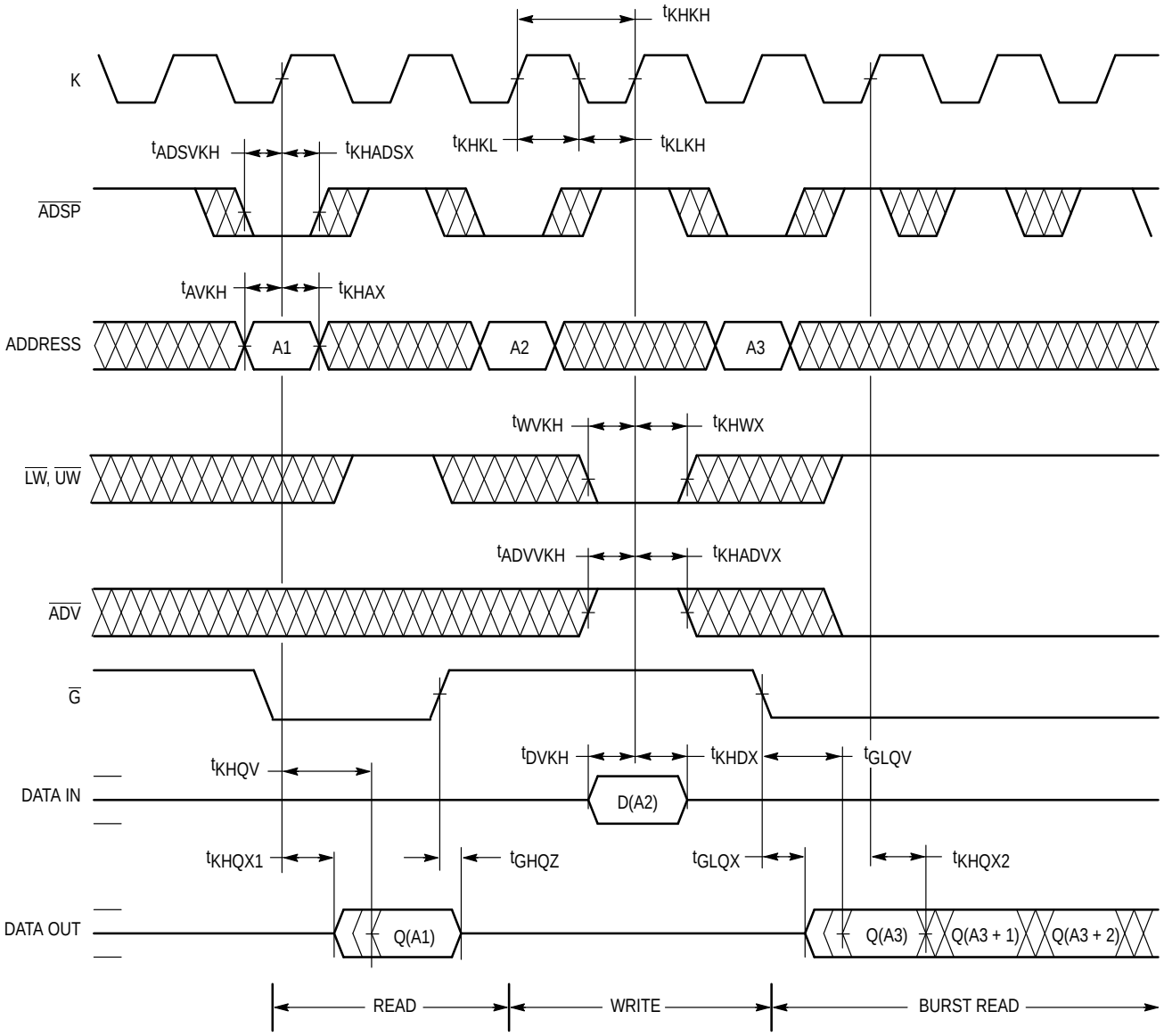


NOTE: Q(A2) represents the first output data from the base address A2; Q(A2 + 1) represents the next output data in the burst sequence with A2 as the base address.

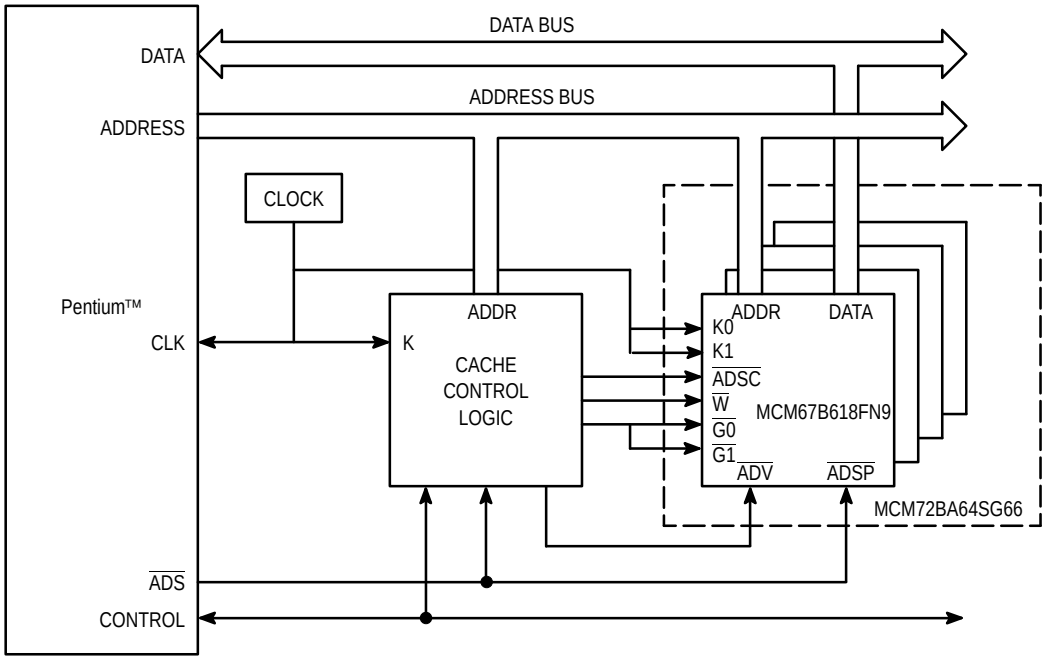
WRITE CYCLES



COMBINATION READ/WRITE CYCLE



APPLICATION EXAMPLE



512K Byte Burstable, Secondary Cache
Using MCM72BA64SG66 with a 66 MHz Pentium

Figure 2

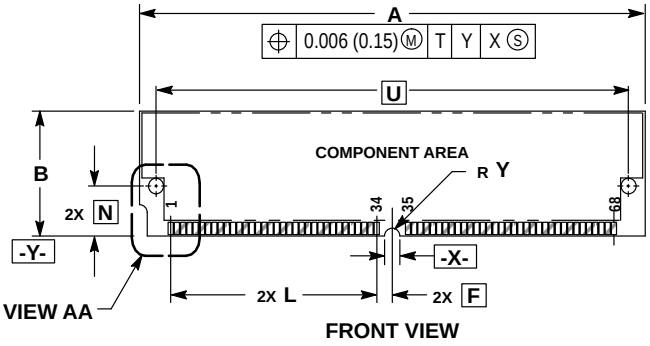
ORDERING INFORMATION
(Order by Full Part Number)

	MCM	72BA32 72BA64	XX	XX
Motorola Memory Prefix				
Part Number				
Speed (66 = 66 MHz, 60 = 60 MHz, 50 = 50 MHz)				
Package (SG = Gold Pad SIMM)				

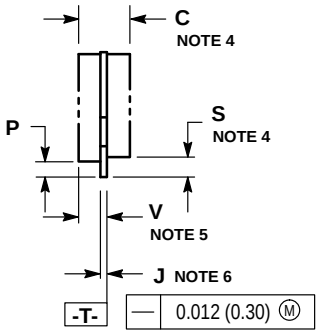
Full Part Numbers —			
	MCM72BA32SG66	MCM72BA32SG60	MCM72BA32SG50
	MCM72BA64SG66	MCM72BA64SG60	MCM72BA64SG50

PACKAGE DIMENSIONS

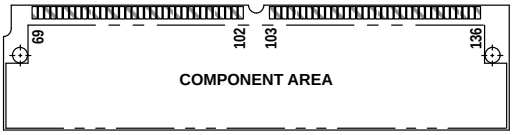
136–LEAD
DIMM MODULE
CASE 1104–01



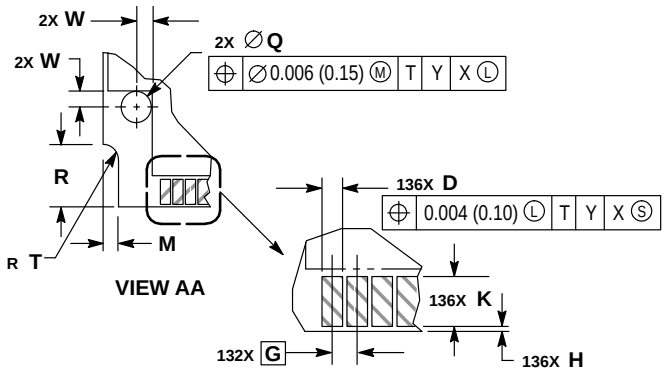
FRONT VIEW



SIDE VIEW



BACK VIEW



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALLIZATION.
4. DIMENSIONS C AND S DEFINE A DOUBLE–SIDED MODULE.
5. DIMENSION V DEFINES OPTIONAL SINGLE–SIDED MODULE.
6. STRAIGHTNESS CALLOUT APPLIES TO TAB AREA ONLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	4.045	4.055	102.74	103.00
B	0.995	1.005	25.27	25.53
C	—	0.413	—	10.50
D	0.040	0.042	1.02	1.07
F	0.125 BSC		3.18 BSC	
G	0.050 BSC		1.27 BSC	
H	—	0.010	—	0.25
J	0.046	0.054	1.17	1.37
K	0.100	—	2.54	—
L	1.650 BSC		41.91 BSC	
M	0.075	0.085	1.91	2.16
N	0.400 BSC		10.16 BSC	
P	0.125	—	3.18	—
Q	0.123	0.127	3.12	3.22
R	0.245	0.255	6.22	6.48
S	0.157	—	4.00	—
T	0.060	0.064	1.52	1.63
U	3.784 BSC		96.11 BSC	
V	—	0.236	—	6.00
W	0.062	—	1.57	—
Y	0.060	0.064	1.52	1.63

Literature Distribution Centers:
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ASIA PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.