MCM72F10

8MB Synchronous Fast Static RAM Module

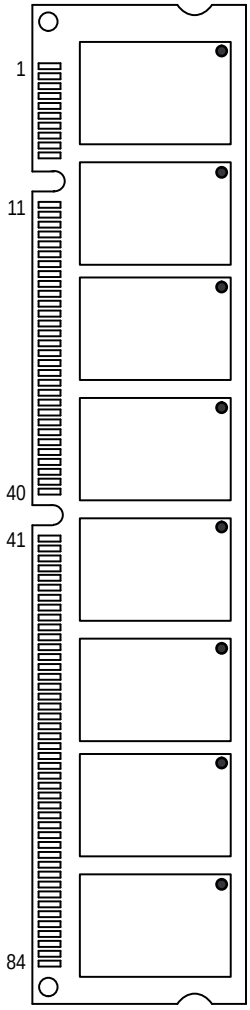
The MCM72F10 (2MB) is configured as 1M x 72 bits. It is packaged in a 168–pin dual–in–line memory module DIMM. The module uses Motorola's 3.3 V, 256K x 18 bit flow–through BurstRAMs.

Address (A), data inputs (DQ, DP), and all control signals except output enable (G) are clock (K) controlled through positive–edge–triggered noninverting registers.

Write cycles are internally self–timed and initiated by the rising edge of the clock (K) input. This feature provides increased timing flexibility for incoming signals. Synchronous byte write (W) allows writes to either individual bytes or to both bytes.

- Single 3.3 V + 10%, – 5% Power Supply
- Plug and Pin Compatibility with 1MB, 2MB, and 4MB
- Multiple Clock Pins for Reduced Loading
- All Inputs and Outputs are LVTTL Compatible
- Byte Write Capability
- Fast SRAM Access Times: 8/9/12 ns
- High Quality Multi–Layer FR4 PWB With Separate Power and Ground Planes
- Amp Connector, Part Number: 390064–4
- 168–Pin DIMM Module

168–LEAD DIMM
CASE TBD
TOP VIEW



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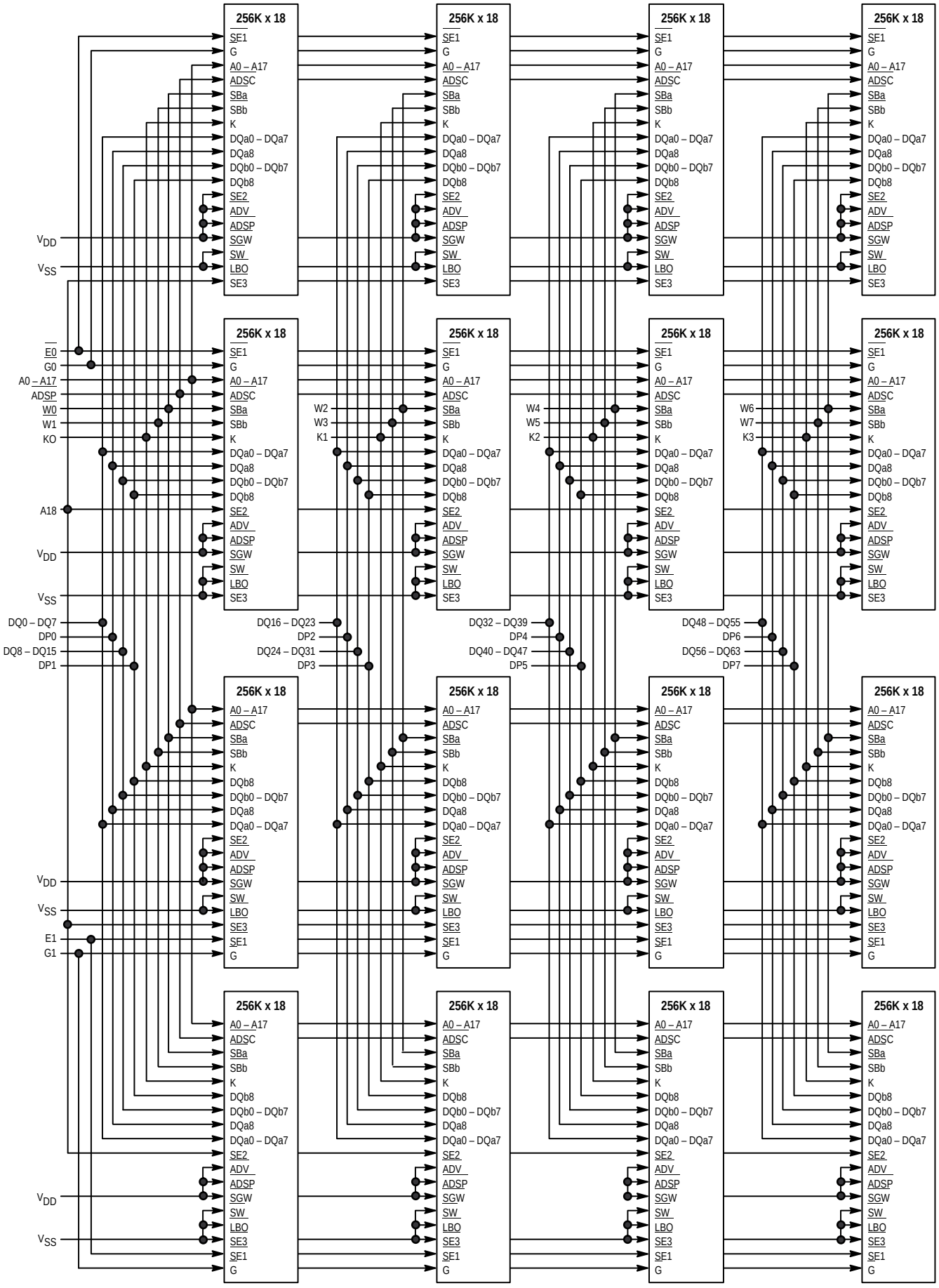
BLOCK DIAGRAM



PIN ASSIGNMENT
168–LEAD DIMM
TOP VIEW

V_{SS}	1	85	V_{SS}
DQ63	2	86	DP7
DQ62	3	87	DQ61
V_{DD}	4	88	V_{SS}
DQ60	5	89	DQ59
DQ58	6	90	DQ57
V_{SS}	7	91	V_{SS}
DQ56	8	92	DP6
DQ55	9	93	DQ54
V_{SS}	10	94	V_{DD}
DQ53	11	95	DQ52
DQ51	12	96	DQ50
V_{SS}	13	97	V_{SS}
DQ49	14	98	DQ48
DP5	15	99	DQ47
V_{DD}	16	100	V_{SS}
DQ46	17	101	DQ45
DQ44	18	102	DQ43
V_{SS}	19	103	V_{SS}
DQ42	20	104	DQ41
DQ40	21	105	DP4
V_{SS}	22	106	V_{DD}
DQ39	23	107	DQ38
DQ37	24	108	DQ36
V_{SS}	25	109	V_{SS}
DQ35	26	110	DQ34
DQ33	27	111	DQ32
V_{SS}	28	112	V_{SS}
K3	29	113	K2
V_{SS}	30	114	V_{SS}
DP3	31	115	DQ31
DQ30	32	116	DQ29
V_{DD}	33	117	V_{SS}
DQ28	34	118	DQ27
DQ26	35	119	DQ25
V_{SS}	36	120	V_{SS}
DQ24	37	121	DP2
DQ23	38	122	DQ22
V_{SS}	39	123	V_{DD}
DQ21	40	124	DQ20
DQ19	41	125	DQ18
V_{SS}	42	126	V_{SS}
DQ17	43	127	DQ16
DP1	44	128	DQ15
V_{DD}	45	129	V_{SS}
DQ14	46	130	DQ13
DQ12	47	131	DQ11
V_{SS}	48	132	V_{SS}
DQ10	49	133	DQ9
DQ8	50	134	DP0
V_{SS}	51	135	V_{DD}
DQ7	52	136	DQ6
DQ5	53	137	DQ4
V_{SS}	54	138	V_{SS}
DQ3	55	139	DQ2
DQ1	56	140	DQ0
V_{DD}	57	141	V_{SS}
NC	58	142	NC
A18	59	143	A17
V_{SS}	60	144	V_{SS}
A16	61	145	A15
A14	62	146	A13
V_{SS}	63	147	V_{DD}
A12	64	148	A11
A10	65	149	A9
V_{SS}	66	150	V_{SS}
A8	67	151	A7
A6	68	152	A5
V_{DD}	69	153	V_{SS}
A4	70	154	A3
A2	71	155	$\overline{A1}$
A0	72	156	ADSP
V_{SS}	73	157	V_{SS}
K1	74	158	K0
V_{SS}	75	159	V_{SS}
$\overline{W7}$	76	160	$\overline{W6}$
W5	77	161	W4
V_{SS}	78	162	V_{SS}
$\overline{W3}$	79	163	$\overline{W2}$
W1	80	164	W0
V_{SS}	81	165	V_{DD}
$\overline{G1}$	82	166	$\overline{G0}$
E1	83	167	E0
V_{SS}	84	168	V_{SS}

PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
59, 61, 62, 64, 65, 67, 68, 70, 71, 72, 143, 145, 146, 148, 149, 151, 152, 154, 155	A0 – A18	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
156	ADSP	Input	Synchronous Addresss Status Controller: Initiates read, write, or chip deselect cycle.
15, 31, 44, 86, 92, 105, 121, 134	DP0 – DP7		Synchronous Parity Data Inputs/Outputs.
2, 3, 5, 6, 8, 9, 11, 12, 14, 17, 18, 20, 21, 23, 24, 26, 27, 32, 34, 35, 37, 38, 40, 41, 43, 46, 47, 49, 50, 52, 53, 55, 56, 87, 89, 90, 93, 95, 96, 98, 99, 101, 102, 104, 107, 108, 110, 111, 115, 116, 118, 119, 122, 124, 125, 127, 128, 130, 131, 133, 136, 137, 139, 140	DQ0 – DQ63	I/O	Synchronous Data Inputs/Outputs.
83, 167	$\overline{E0}$, $\overline{E1}$	Input	Synchronous Chip Enable: Active low to enable chip. Negated high — blocks ADSP or deselects chip when ADSC is asserted.
82, 166	$\overline{G0}$, $\overline{G1}$	Input	Asynchronous Output Enable Input: Low — enables output buffer. High — DQx pins are high impedance.
29, 74, 113, 158	K0 – K3	Input	Clock: This signal registers the address, data in, and all control signals except G and LBO.
76, 77, 79, 80, 160, 161, 163, 164	$\overline{W0}$ – $\overline{W7}$	Input	Synchronous Byte Write Inputs: x refers to the byte being written (byte a, b).
4, 16, 33, 45, 57, 69, 94, 106, 123, 135, 147, 165	V_{DD}	Supply	Power Supply: 3.3 V + 10%, – 5%. Must be connected on all modules.
1, 7, 10, 13, 19, 22, 25, 28, 30, 36, 39, 42, 48, 51, 54, 60, 63, 66, 73, 75, 78, 81, 84, 85, 88, 91, 97, 100, 103, 109, 112, 114, 117, 120, 126, 129, 132, 138, 141, 144, 150, 153, 157, 159, 162, 168	V_{SS}	Supply	Ground.
58, 142	NC		No Connection: There is no connection to the chip.

DATA RAM MCM69F618A SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, 3, and 4)

Next Cycle	Address Used	E	ADSP	G	DQx	WRITE
Deselect	None	1	0	X	High–Z	X
Begin Read	External Address	0	0	0	DQ	Read
Read	Current	X	1	1	High–Z	Read
Read	Current	X	1	0	DQ	Read
Begin Write	External	0	0	X	High–Z	Write
Write	Current	X	1	X	High–Z	Write

NOTES:
1. X = don't care, 1 = logic high, 0 = logic low.
2. Write is defined as any Wx low.
3. G is an asynchronous signal and is not sampled by the clock K. $\overline{G}$ drives the bus immediately (t_{GLQX}) following $\overline{G}$ going low.
4. On write cycles that follow read cycles, $\overline{G}$ must be negated prior to the start of the write cycle to ensure proper write data setup times. $\overline{G}$ must also remain negated at the completion of the write cycle to ensure proper write data hold times.

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Voltage Relative to V_{SS} (See Note 2)	V_{in}, V_{out}	– 0.5 to V_{DD} + 0.5	V
Input Voltage Three State I/O (See Note 2)	V_{IT}	V_{SS} – 0.5 to V_{DD} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	4.6	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. This is a steady–state DC parameter that is in effect after the power supply has achieved its nominal operating level. Power sequencing can not be controlled and is not allowed.
3. Power dissipation capability is dependent upon package characteristics and use environment. See Package Thermal Characteristics.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

PACKAGE THERMAL CHARACTERISTICS — PBGA

Rating		Symbol	Max	Unit	Notes
Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	41 19	°C/W	1, 2
Junction to Board (Bottom)		$R_{\theta JB}$	11	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	19	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

(3.6 V ≥ V_{DD} ≥ 3.1 V, T_J = 20 to + 110°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{DD}	3.135	3.3	3.6	V
Input High Voltage	V_{IH}	1.7	—	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	– 0.3*	—	0.7	V

* V_{IL} ≥ – 2.0 V for t ≤ t_{KHKH}/2.

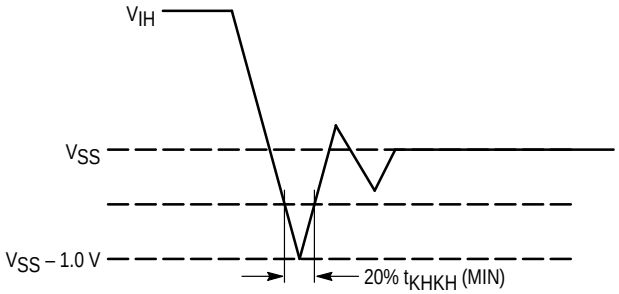


Figure 1. Undershoot Voltage

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (0 V ≤ V_{in} ≤ V_{DD})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current (0 V ≤ V_{in} ≤ V_{DD})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter		Symbol	Min	Max	Unit
AC Supply Current (Device Selected, All Outputs Open, Cycle Time ≥ t_{KHKH} min)	MCM72F10DG8 MCM72F10DG9 MCM72F10DG12	I_{DDA}	—	3580 3480 3380	mA
CMOS Standby Supply Current (Deselected, Clock (K) Cycle Time ≥ t_{KHKH}		I_{SB1}	—	3040	mA
Clock Running Supply Current (Deselected, Clock (K) Cycle Time ≥ t_{KHKH}, All Other Inputs Held to Static CMOS Levels V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{DD} – 0.2 V)		I_{SB2}	—	1360	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_J = 20 to 110 °C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Typ	Max	Unit
Input Capacitance	Address, $\overline{ADSP}$ $\overline{E}$, $\overline{G}$ Other Inputs	C_{in}	74 42 26	90 50 30	pF
I/O Capacitance		$C_{I/O}$	38	42	pF

MASS (Periodically Sampled Rather Than 100% Tested)

Parameter	Max	Unit
Mass	36	g

AC OPERATING CONDITIONS AND CHARACTERISTICS

(3.6 V ≥ V_{DD} ≥ 3.1 V, T_J = 20 to + 110°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.25 V
Input Pulse Levels . . . . . 0 to 2.5 V
Input Slew Rate (See Notes 1 and 2) . . . . . 1.0 V/ns
Output Timing Reference Level . . . . . 1.25 V
Output Load . . . . . See Figure 2 Unless Otherwise Noted
Output Rise/Fall Time . . . . . 1.8 ns

DATA RAMs READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM72F10–8		MCM72F10–9		MCM72F10–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	10	—	11	—	16.6	—	ns	
Clock Access Time	t_{KHQV}	—	8	—	9	—	12	ns	4
Output Enable to Output Valid	t_{GLQV}	—	3.5	—	3.5	—	5	ns	4
Clock High to Output Active	t_{KHQX1}	0	—	0	—	0	—	ns	4, 5, 6, 7
Clock High to Output Change	t_{KHQX2}	2	—	2	—	2	—	ns	4, 6
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	4, 5, 6
Output Disable to Q High–Z	t_{GHQZ}	—	3.5	—	3.5	—	3.5	ns	4, 5, 6
Clock High to Q High–Z	t_{KHQZ}	2	3.5	2	3.5	2	3.5	ns	4, 5, 6, 7
Clock High Pulse Width	t_{KHKL}	4	—	4.5	—	5	—	ns	
Clock Low Pulse Width	t_{KLKH}	4	—	4.5	—	5	—	ns	
Setup Times: Address ADSP Data In Write Chip Enable	t_{AVKH} t_{ADKH} t_{DVKH} t_{WVKH} t_{EVKH}	2	—	2	—	2	—	ns	
Hold Times: Address ADSP, ADSC, ADV Data In Write Chip Enable	t_{KHAX} t_{KHADX} t_{KHDX} t_{KHWX} t_{KHEX}	0.5	—	0.5	—	0.5	—	ns	

NOTES:
1. In setup and hold times, write refers to either any $\overline{SBx}$ and $\overline{SW}$ or $\overline{SGW}$ is low. $\overline{ADSP}$
2. Chip enable is defined as SE1 low, SE2 high, and $\overline{SE3}$ low whenever $\overline{ADSP}$ or $\overline{ADSC}$ is asserted.
3. All read and write cycle timings are referenced from K or G.
4. Tested per AC Test Load (Figure 2).
5. Measured at ± 200 mV from steady state. Tested per High–Z Test Load (Figure 2).
6. This parameter is sampled and not 100% tested.
7. At any given voltage and temperature, t_{KHQZ} (Max) is less than t_{KHQX1} (Min) for a given device and from device to device.

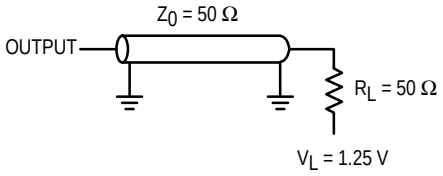
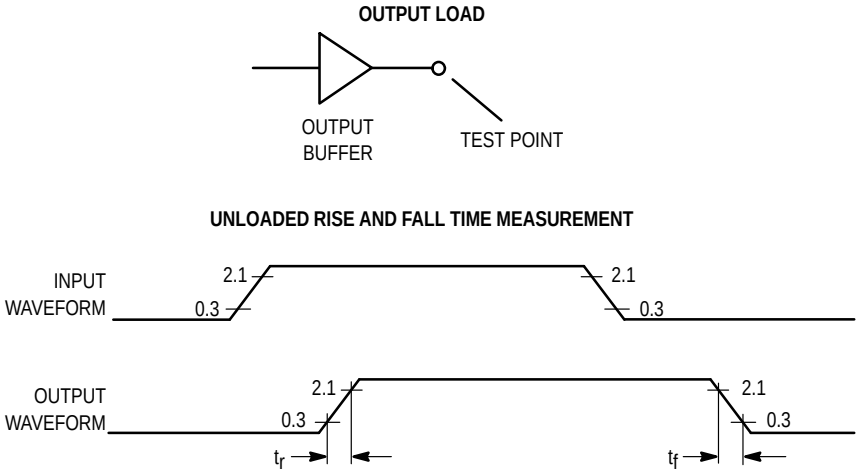


Figure 2. AC Test Load

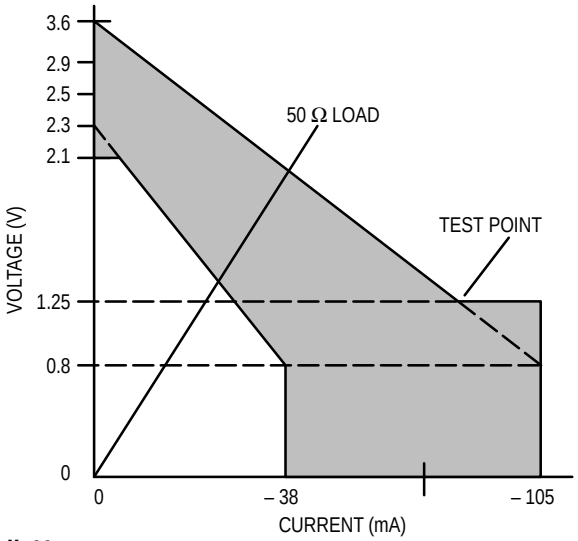


NOTES:

1. Input waveform has a slew rate of 1 V/ns.
2. Rise time is measured from 0.3 to 2.1 V unloaded.
3. Fall time is measured from 2.1 to 0.3 V unloaded.

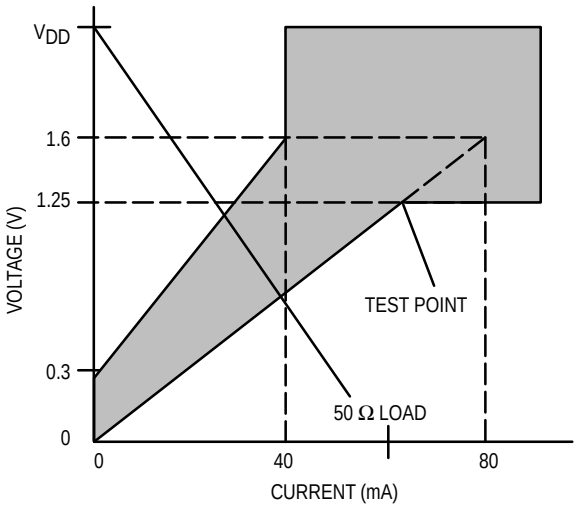
Figure 3. Unloaded Rise and Fall Time Characterization

PULL–UP		
VOLTAGE (V)	I (mA) MIN	I (mA) MAX
– 0.5	– 38	– 105
0	– 38	– 105
0.8	– 38	– 105
1.25	– 26	– 83
1.5	– 20	– 70
2.3	0	– 30
2.7	0	– 10
2.9	0	0
3.4	0	0
3.6	0	0



(a) Pull–Up

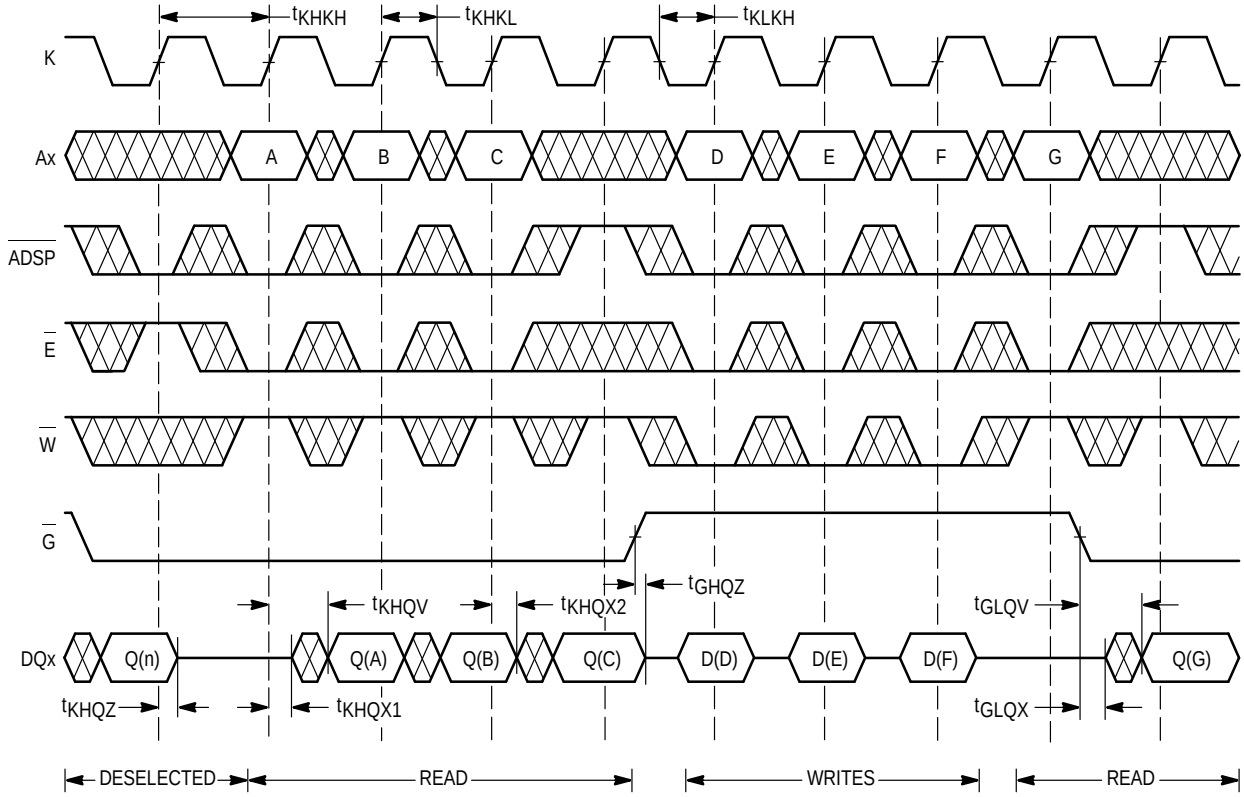
PULL–DOWN		
VOLTAGE (V)	I (mA) MIN	I (mA) MAX
– 0.5	0	0
0	0	0
0.4	10	20
0.8	20	40
1.25	31	63
1.6	40	80
2.8	40	80
3.2	40	80
3.4	40	80
3.6	46	120



(b) Pull–Down

Figure 4. Output Buffer Characteristics

READ/WRITE CYCLES



ORDERING INFORMATION

(Order by Full Part Number)

MCM 72F X XX XX

- MCM — Motorola Memory Prefix
- 72F — Part Number
- X — Memory Size (10 = 8MB)
- XX — Package (DG = Gold Pad DIMM)
- XX — Speed (8 = 8 ns, 9 = 9 ns, 12 = 12 ns)

Full Part Numbers — MCM72F10DG8 MCM72F10DG9 MCM72F10DG12

PACKAGE DIMENSIONS

DG PACKAGE
CASE TBD

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