MCM8A10

Advance Information

1M x 8 Bit Fast Static RAM Module

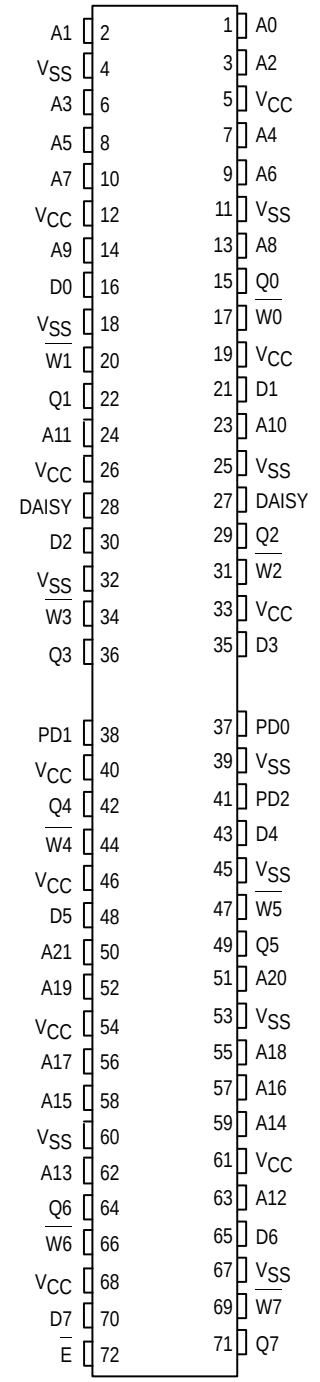
The MCM8A10 is an 8M bit static random access memory module organized as 1,048,576 words of 8 bits. The module is offered in a 72–lead single in–line memory module (SIMM). Eight MCM6227B fast static RAMs, packaged in 28–lead SOJ packages are mounted on a printed circuit board along with eight decoupling capacitors.

The MCM6227B is organized as 1,048,576 words of 1 bit. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM8A10 is equipped with a chip enable (E) and eight separate write enable (W0 – W7) inputs, allowing for greater system flexibility.

- Single 5 V ± 5% Power Supply
- Fast Access Times: 15 ns
- Three–State Outputs
- Fully TTL Compatible
- High Board Density SIMM Package
- Bit Operation: Eight Separate Write Enables, One for Each Bit
- High Quality Six–Layer FR4 PWB with Separate Internal Power and Ground Planes

PIN ASSIGNMENT
TOP VIEW
72-LEAD SIMM – CASE TBD



PIN NAMES

A0 – A19	Address Inputs
W0 – W7	Write Enables
E	Chip Enable
D0 – D7	Data Inputs
Q0 – Q7	Data Outputs
PD0 – PD2	Package Density
DAISY	Pins Single Net
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

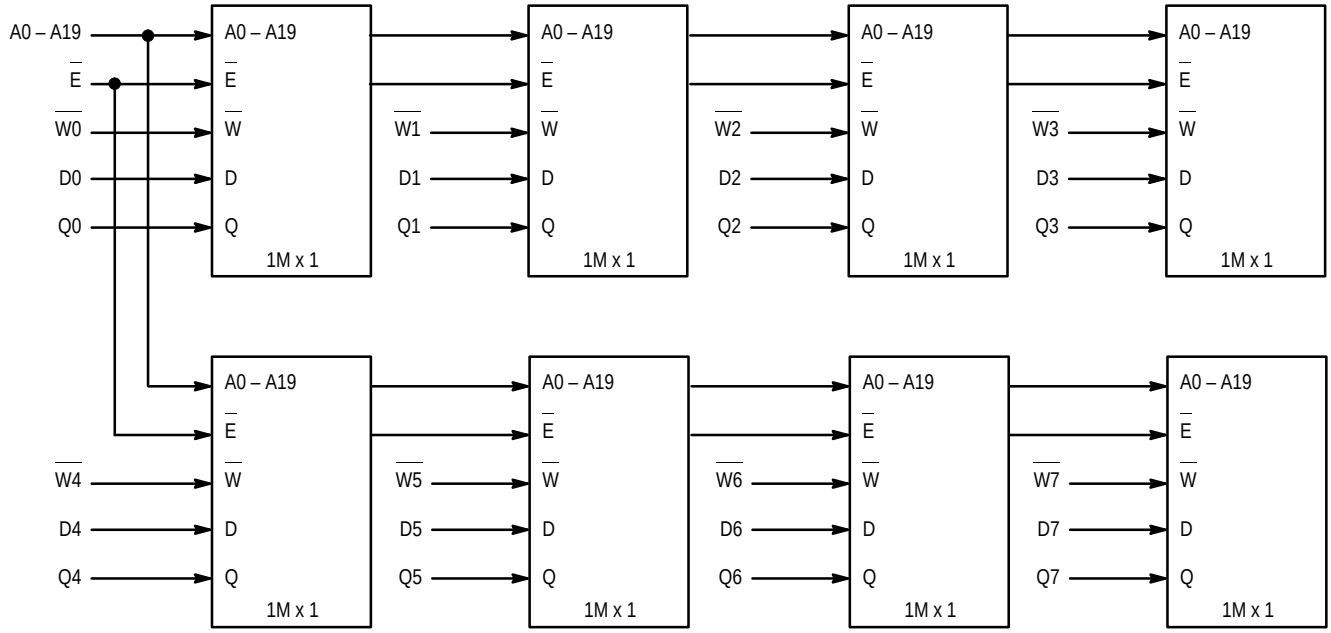
For proper operation of the device, V_{SS} must be connected to ground.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

10/30/96

MOTOROLA

FUNCTIONAL BLOCK DIAGRAM
1M x 8 MEMORY MODULE



PD0 — Open
PD1 — V_{SS}
PD2 — Open

TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	I/O Pin	Cycle	Current
H	X	Not Selected	High–Z	—	I_{SB1}, I_{SB2}
L	H	Read	D_{out}	Read	I_{CCA}
L	L	Write	High–Z	Write	I_{CCA}

NOTE: H = High, L = Low, X = Don't Care

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 20	mA
Power Dissipation	P_D	8.8	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} +0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns).
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns).

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1	μA
Output Leakage Current (E = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1	μA
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max)	I_{CCA}	—	920	mA
AC Standby Current (V_{CC} = max, E = V_{IH}, f ≤ f_{max})	I_{SB1}	—	320	mA
CMOS Standby Current (E ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V, V_{CC} = max, f = 0 MHz)	I_{SB2}	—	40	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	Address Inputs	C_{in}	42	58	pF
	$\overline{E}$		50	74	
	$\overline{W}$		10	13	
Input and Output Capacitance	D, Q	C_{in}, C_{out}	10	13	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

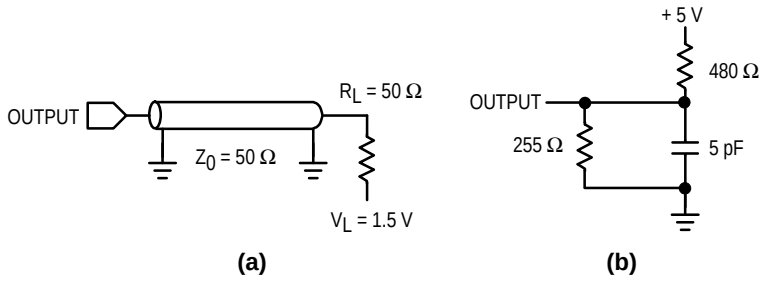
(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 2 ns
Input Timing Measurement Reference Level . . . . . 1.5 V
Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . See Figure 1a

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM8A10–15		Unit	Notes
		Min	Max		
Read Cycle Time	t_{AVAV}	15	—	ns	2, 3
Address Access Time	t_{AVQV}	—	15	ns	
Enable Access Time	t_{ELQV}	—	15	ns	4
Output Hold from Address Change	t_{AXQX}	5	—	ns	
Enable Low to Output Active	t_{ELQX}	5	—	ns	5, 6, 7
Enable High to Output High–Z	t_{EHQZ}	0	6	ns	5, 6, 7

NOTES:
1. W is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with E going low.
5. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1b.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($E \leq V_{IL}$).

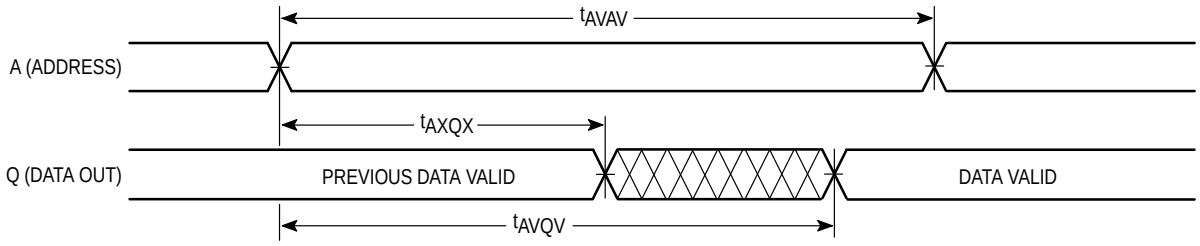


TIMING LIMITS

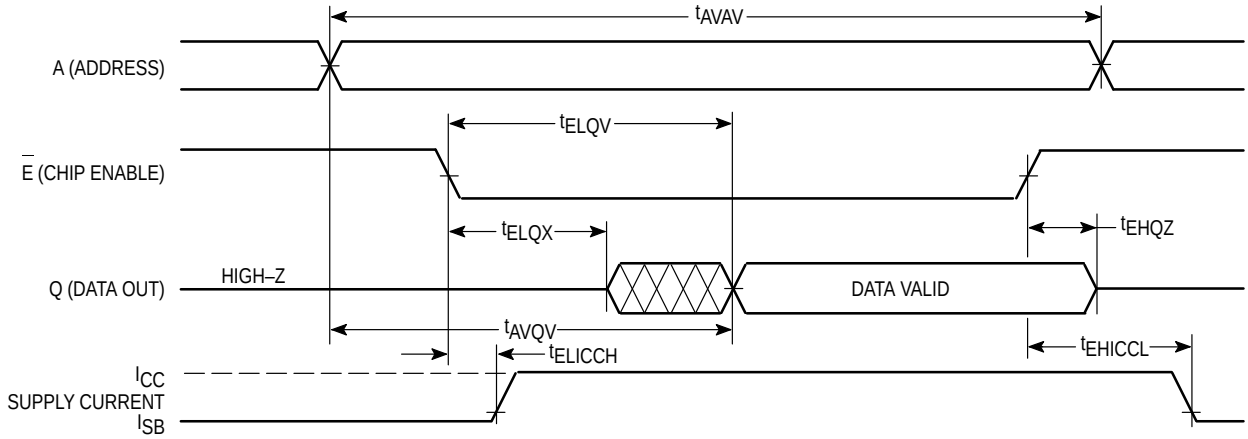
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

Figure 1. AC Test Loads

READ CYCLE 1 (See Notes 1, 2, and 8)



READ CYCLE 2 (See Note 4)

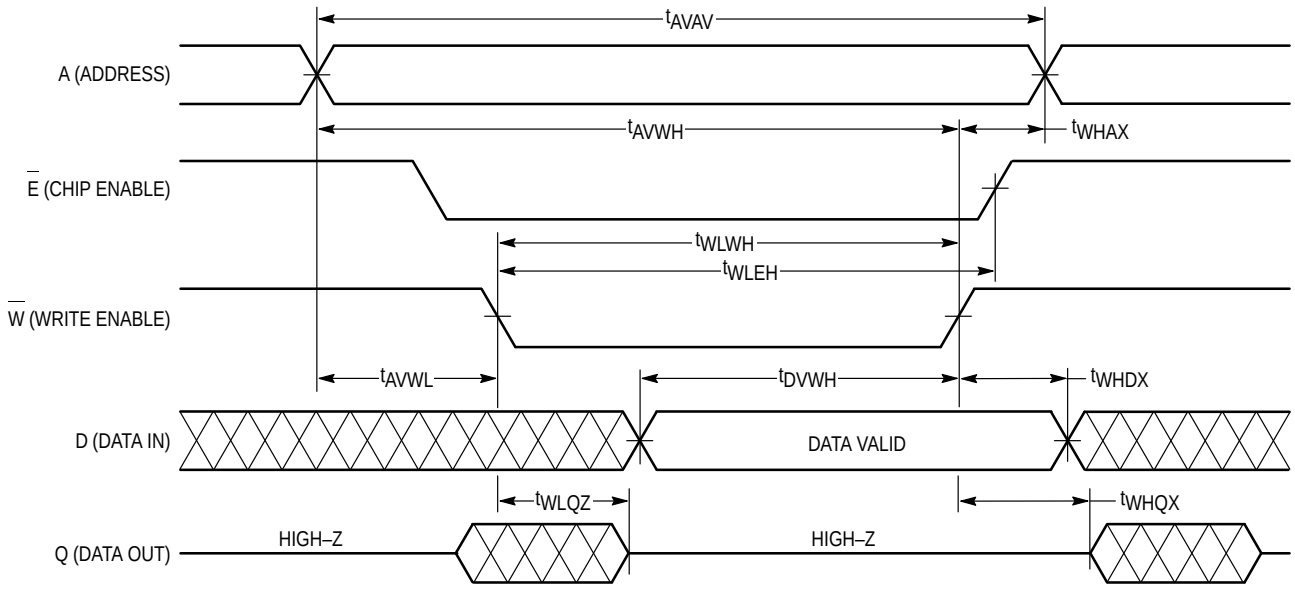


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM8A10–15		Unit	Notes
		Min	Max		
Write Cycle Time	t_{AVAV}	15	—	ns	3
Address Setup Time	t_{AVWL}	0	—	ns	
Address Valid to End of Write	t_{AVWH}	12	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	12	—	ns	
Data Valid to End of Write	t_{DVWH}	7	—	ns	
Data Hold TIme	t_{WHDX}	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	6	ns	4, 5, 6
Write High to Output Active	t_{WHQX}	5	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1b.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1 ($\overline{W}$ Controlled See Notes 1 and 2)

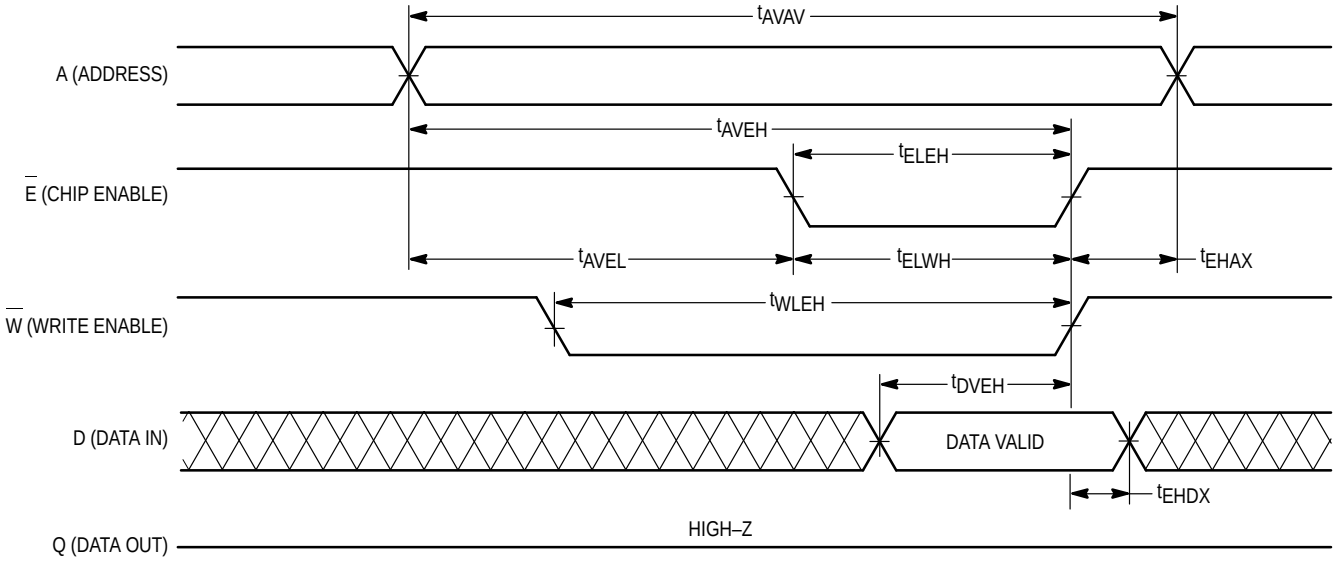


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

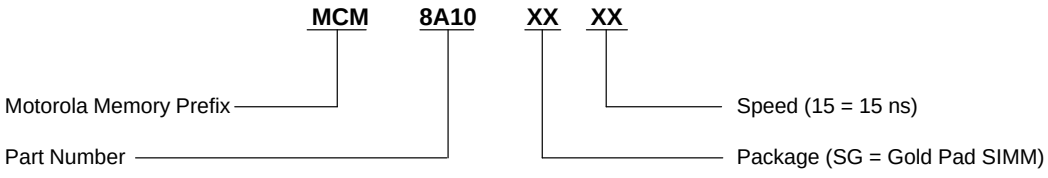
Parameter	Symbol	MCM8A10–15		Unit	Notes
		Min	Max		
Write Cycle Time	t_{AVAV}	15	—	ns	3
Address Setup Time	t_{AVEL}	0	—	ns	
Address Valid to End of Write	t_{AVEH}	12	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	10	—	ns	4, 5
Write Pulse Width	t_{WLEH}	12	—	ns	
Data Valid to End of Write	t_{DVEH}	7	—	ns	
Data Hold Time	t_{EHDX}	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after W goes low, the output will remain in a high–impedance state.
5. If $\overline{E}$ goes high coincident with or before W goes high, the output will remain in a high–impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled See Notes 1 and 2)



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Number — MCM8A10SG15

PACKAGE DIMENSIONS

72–LEAD SIMM
CASE TBD

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