

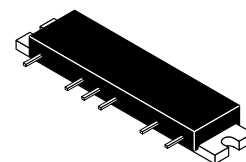
## The RF Line UHF Power Amplifier

... designed specifically for the Pan European digital 8.0 watt, GSM mobile radio. Other applications exist in standard analog cellular radios. The MHW912 is capable of wide power range control, operates from a 12.5 volt supply and requires only 1.0 mW of RF input power.

- Specified 12.5 Volt Characteristics:
  - RF Input Power — 1.0 mW (0 dBm)
  - RF Output Power — 12.5 W
  - Minimum Gain — 41 dB
  - Harmonics — -30 dBc Max @ 2.0  $f_0$
- New Biasing and Control Techniques Providing Dynamic Range and Control Circuit Bandwidth Ideal for GSM
- Low Control Current
- 50 Ohm Input/Output Impedances
- Guaranteed Stability and Ruggedness
- Test fixture circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

**MHW912**

**12.5 W**  
**884 to 915 MHz**  
**RF POWER**  
**AMPLIFIER**



**CASE 301R-01, STYLE 1**

### MAXIMUM RATINGS (Flange Temperature = 25°C)

Rating	Symbol	Value	Unit
DC Supply Voltage	$V_{S1, b}$	8.5	Vdc
DC Supply Voltage — With RF Applied/Without RF Applied	$V_{S2, 3}$	15.6/30	Vdc
DC Control Voltage	$V_{cont}$	4.0	Vdc
RF Input Power	$P_{in}$	3.0	mW
RF Output Power ( $V_S = 15.6$ Vdc)	$P_{out}$	14	W
Operating Case Temperature Range	$T_C$	-30 to +100	°C
Storage Temperature Range	$T_{stg}$	-30 to +100	°C

### ELECTRICAL CHARACTERISTICS ( $V_{S2} = V_{S3} = 12.5$ Vdc; $V_{S1} = V_b = 8.0$ Vdc; $T_C = +25^\circ\text{C}$ , 50 ohm system, unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Frequency Range	BW	884	915	MHz
Output Power ( $P_{in} = 1.0$ mW; $V_{cont} = 3.0$ Vdc)	$P_{out1}$	12.5	—	W
Output Power, Reduced Voltage ( $P_{in} = 1.0$ mW; $V_{cont} = 3.0$ Vdc; $V_{S1} = V_b = 8.0$ V; $V_{S2} = V_{S3} = 10.8$ Vdc)	$P_{out2}$	8.5	—	W
Control Current ( $P_{out} = 12.5$ W; $P_{in} = 1.0$ mW) (1)	$I_{cont}$	—	1.0	mA
Current Consumption in 8.0 V Pins ( $P_{out} = 12.5$ W; $P_{in} = 1.0$ mW)	$I_{S1} + I_b$	—	220	mA
Leakage Current ( $P_{in} = 0$ mW; $V_{cont} = 0$ ; $V_{S1} = V_b = 0$ )	$I_L$	—	1.0	mA
Efficiency ( $P_{out} = 12.5$ W; $P_{in} = 1.0$ mW) (1)	$\eta$	35 33	—	%
Input VSWR ( $P_{out} = 0.03$ to 12.5 W; $P_{in} = 1.0$ mW) (1)	VSWR <sub>in</sub>	—	2.0:1	—
Harmonics ( $P_{out} = 12.5$ W; $P_{in} = 1.0$ mW) (1)				
Noise Power (In 30 kHz Bandwidth, 20 MHz Above $f_0$ ; $P_{out} = 12.5$ W; $P_{in} = 1.0$ mW) (1)	—	—	-70	dBm

**NOTE:**

- Adjust  $V_{cont}$  for specified  $P_{out}$ ; Duty Cycle = 12.5%, Period = 4.6 ms.

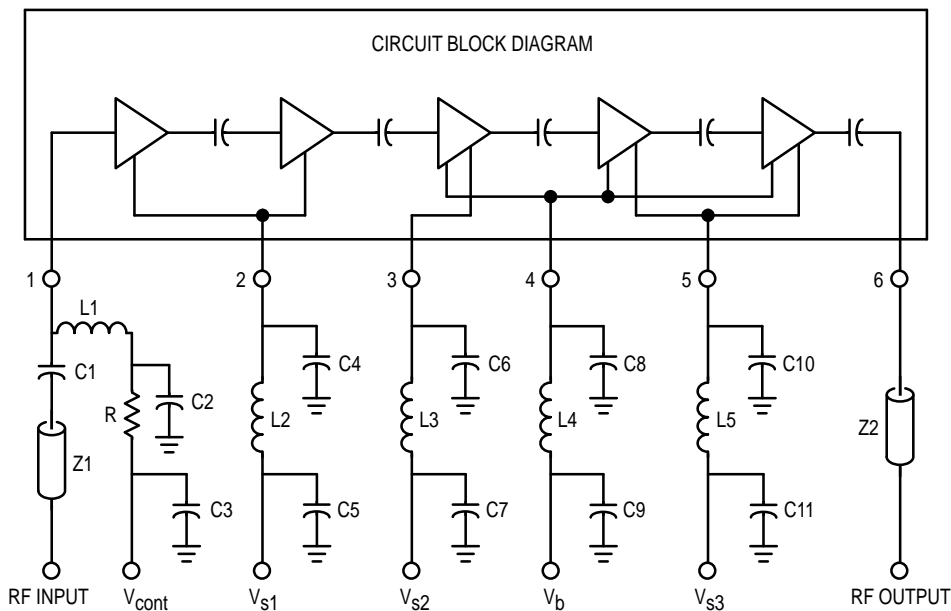
**ELECTRICAL CHARACTERISTICS — continued**

( $V_{S2} = V_{S3} = 12.5$  Vdc;  $V_{S1} = V_b = 8.0$  Vdc;  $T_C = +25^\circ\text{C}$ , 50 ohm system, unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Isolation ( $P_{in} = 1.0$ mW; $V_{cont} = 0$ Vdc; $V_{S1} = V_b = 0$ to 8.0 V)	—	—	-36	dBm
3.0 dB $V_{cont}$ Bandwidth ( $P_{in} = 1.0$ mW; $P_{out} = 0.03$ to 12.5 W) (1)	—	1.0	—	MHz
Load Mismatch Stress ( $V_S = 15.6$ Vdc; $P_{in} = 3.0$ mW; $P_{out} = 14$ W; Load VSWR = 10:1, All Phase Angles at Frequency of Test) (1)	$\psi$	No degradation in output power before and after test		
Stability ( $V_{S2} = V_{S3} = 10.8$ to 15.6 Vdc; $P_{in} = 0.5$ to 3.0 mW; $P_{out} = 12$ mW to 12.5 W; Load VSWR = 6:1, All Phase Angles; Source VSWR = 3:1, All Phase Angles at Frequency of Test) (1)	—	All spurious outputs more than 60 dB below desired signal		

**NOTE:**

1. Adjust  $V_{cont}$  for specified  $P_{out}$ ; Duty Cycle = 12.5%, Period = 4.6 ms.



**PIN DESIGNATIONS:**

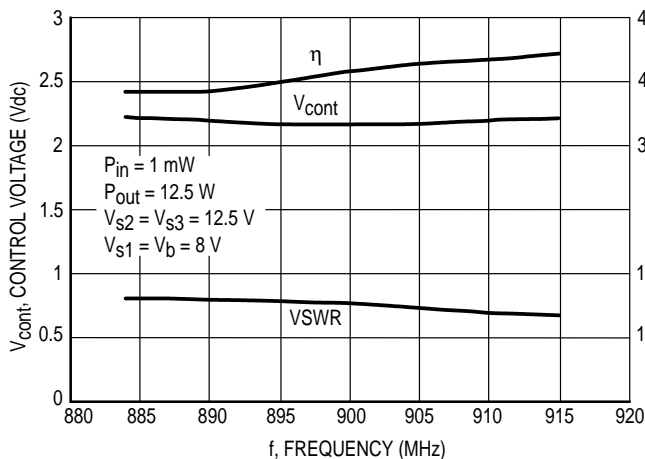
- PIN 1 — RF INPUT POWER @ 0 dBm AND CONTROL VOLTAGE @ 0–3 Vdc
- PIN 2 — FIRST & SECOND STAGE COLLECTOR SUPPLY VOLTAGE @ 8 Vdc
- PIN 3 — THIRD STAGE COLLECTOR VOLTAGE @ 12.5 Vdc
- PIN 4 — TRICKLE BIAS VOLTAGE @ 8 Vdc
- PIN 5 — FOURTH & FIFTH STAGE COLLECTOR SUPPLY VOLTAGE @ 12.5 Vdc
- PIN 6 — RF OUTPUT POWER @ 12.5 W

**ELEMENT VALUES:**

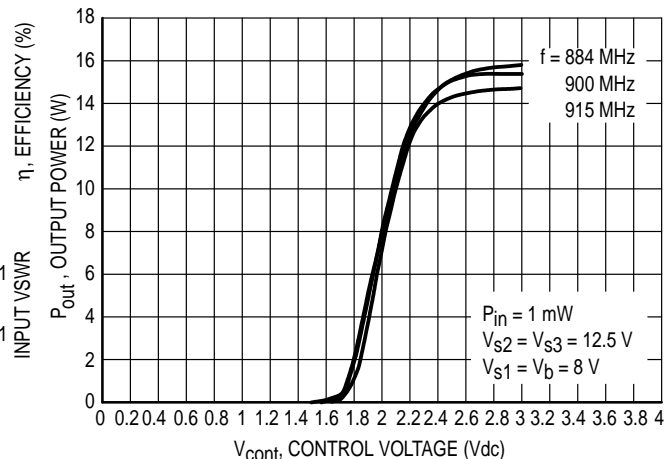
- $C1 = C2 = C4 = C6 = C8 = C10 = 0.018 \mu\text{F}$
- $C3 = C5 = C7 = C9 = C11 = 1 \mu\text{F}$
- $L1-L4 = 0.29 \mu\text{H}$
- $L5 = 0.2 \mu\text{H}$
- $R = 20 \text{ OHMS}$
- $Z1, Z2 = 50 \text{ OHM MICROSTRIP}$

**Figure 1. UHF Power Module Test Circuit Diagram**

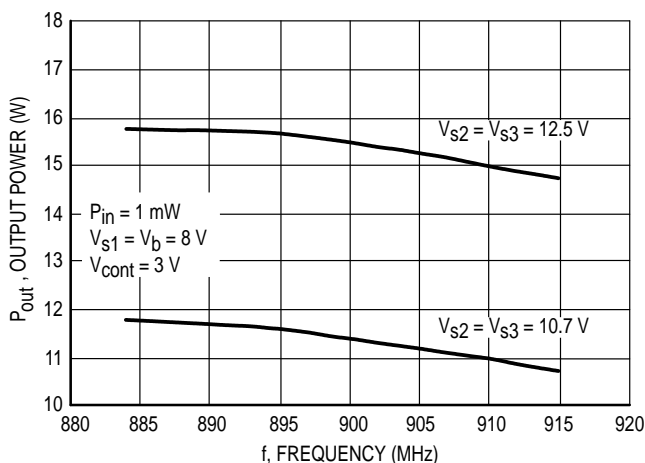
## TYPICAL CHARACTERISTICS



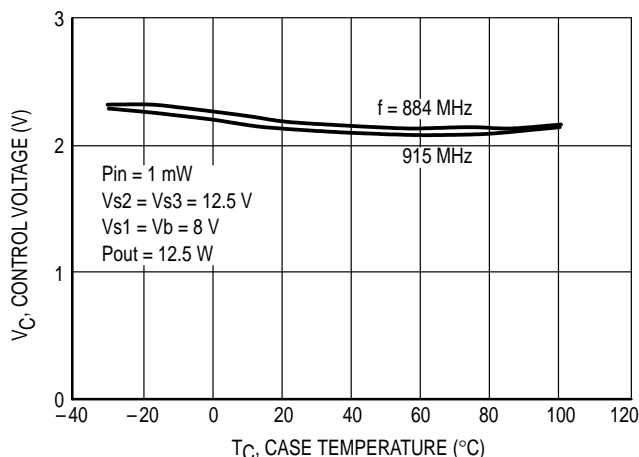
**Figure 2. Control Voltage, Efficiency and Input VSWR versus Frequency**



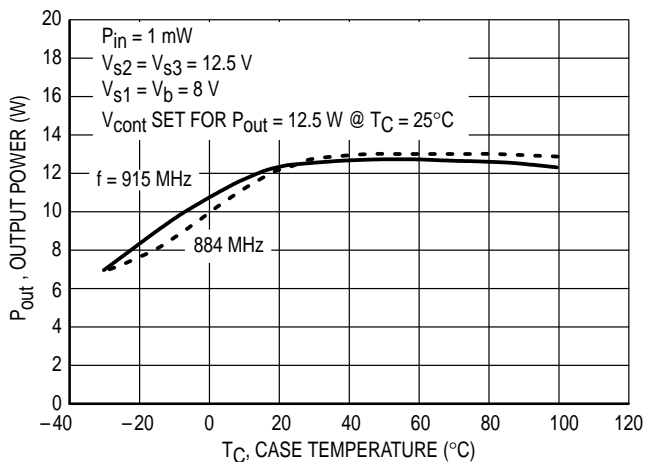
**Figure 3. Output Power versus Control Voltage**



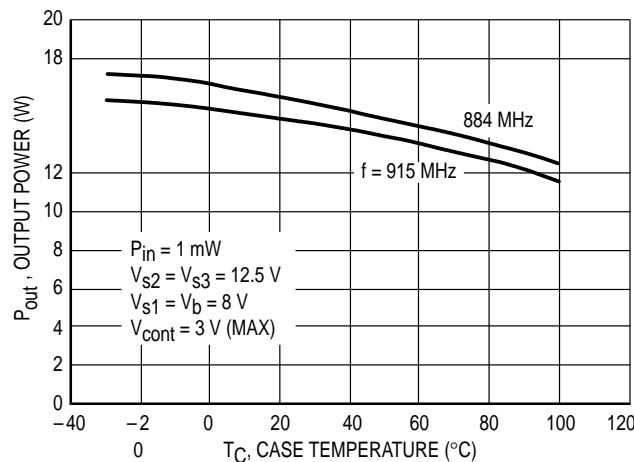
**Figure 4. Output Power versus Frequency**



**Figure 5. Control Voltage versus Case Temperature**



**Figure 6. Output Power versus Case Temperature**



**Figure 7. Output Power versus Case Temperature at Maximum Control Voltage**

## APPLICATIONS INFORMATION

### NOMINAL OPERATION

All electrical specifications are based on the nominal conditions of  $V_b = V_{S1} = 8.0$  Vdc (Pins 2, 4), and  $V_{S2} = V_{S3} = 12.5$  Vdc (Pins 3, 5). With these conditions, maximum current density on any device is  $1.5 \times 10^5$  A/cm<sup>2</sup> and maximum die temperature is 165°C. While the modules are designed to have excess gain margin with ruggedness, operation of these units outside the published specifications is not recommended unless prior communications regarding intended use have been made with the factory representative.

### GAIN CONTROL

The module output power should be limited to specified value. The preferred method of power control is to fix  $V_b = V_{S1} = 8.0$  Vdc (Pins 2, 4),  $V_{S2} = V_{S3} = 12.5$  Vdc (Pins 3, 5), Pin (Pin 1) at 1.0 mW, and vary  $V_{cont}$  (Pin 1) voltage.

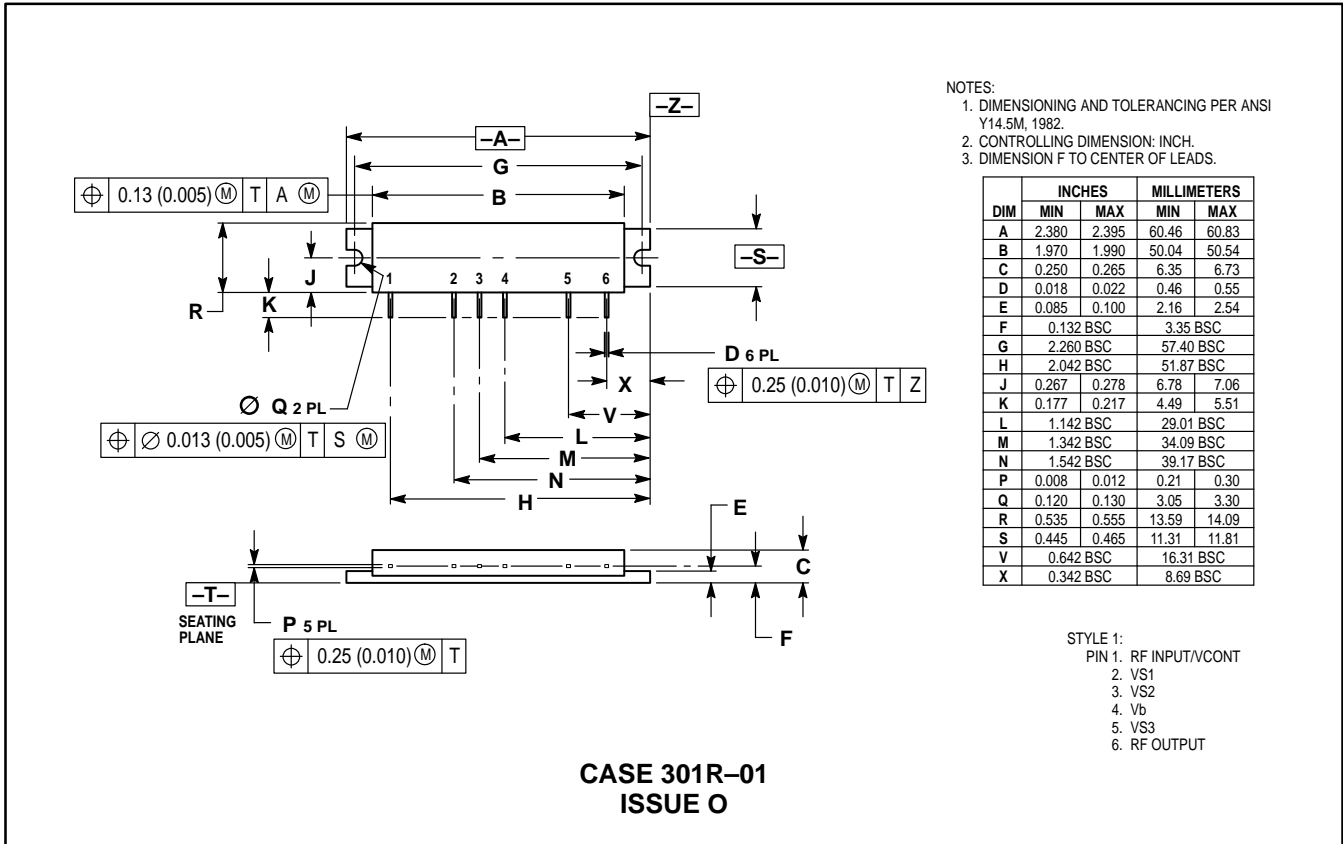
### DECOUPLING

Due to the high gain of the five stages and the module size limitation, external decoupling networks require careful consideration. Pins 2, 3, 4, and 5 are internally bypassed with a 0.018  $\mu$ F chip capacitor which is effective for frequencies from 5.0 MHz through 940 MHz. For bypassing frequencies below 5.0 MHz, networks equivalent to that shown in Figure 1 are recommended. Inadequate decoupling will result in spurious outputs at certain operating frequencies and certain phase angles of input and output VSWR.

### LOAD MISMATCH

During final test, each module is load mismatch tested in a fixture having the identical decoupling networks described in Figure 1. Electrical conditions are  $V_b = V_{S1} = 8.0$  V (Pins 2, 4), and  $V_{S2} = V_{S3} = 15.6$  Vdc (Pins 3, 5),  $P_{in} = 3.0$  mW, VSWR equal to 10:1, and output power equal to 15 watts.


## PACKAGE DIMENSIONS



- NOTES:  
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
 2. CONTROLLING DIMENSION: INCH.  
 3. DIMENSION F TO CENTER OF LEADS.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	2.380	2.395	60.46	60.83
B	1.970	1.990	50.04	50.54
C	0.250	0.265	6.35	6.73
D	0.018	0.022	0.46	0.55
E	0.085	0.100	2.16	2.54
F	0.132 BSC		3.35 BSC	
G	2.260 BSC		57.40 BSC	
H	2.042 BSC		51.87 BSC	
J	0.267	0.278	6.78	7.06
K	0.177	0.217	4.49	5.51
L	1.142 BSC		29.01 BSC	
M	1.342 BSC		34.09 BSC	
N	1.542 BSC		39.17 BSC	
P	0.008	0.012	0.21	0.30
Q	0.120	0.130	3.05	3.30
R	0.535	0.555	13.59	14.09
S	0.445	0.465	11.31	11.81
V	0.642 BSC		16.31 BSC	
X	0.342 BSC		8.69 BSC	

- STYLE 1:  
 PIN 1. RF INPUT/VCONT  
 2. VS1  
 3. VS2  
 4. Vb  
 5. VS3  
 6. RF OUTPUT

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