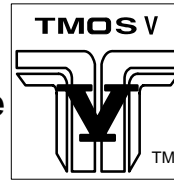


Product Preview

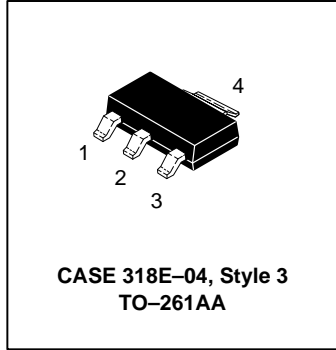
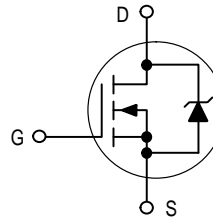
TMOS V™
SOT-223 for Surface Mount
N-Channel Enhancement-Mode Silicon Gate



MMFT3055V

TMOS POWER FET
1.7 AMPERES
60 VOLTS
R_{DS(on)} = 0.130 OHM

TMOS V is a new technology designed to achieve an on-resistance area product about one-half that of standard MOSFETs. This new technology more than doubles the present cell density of our 50 and 60 volt TMOS devices. Just as with our TMOS E-FET designs, TMOS V is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.



New Features of TMOS V

- On-resistance Area Product about One-half that of Standard MOSFETs with New Low Voltage, Low R_{DS(on)} Technology
- Faster Switching than E-FET Predecessors

Features Common to TMOS V and TMOS E-FETS

- Avalanche Energy Specified
- I_{DSS} and V_{DS(on)} Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E-FET
- Available in 12 mm Tape & Reel
Use MMFT3055VT1 to order the 7 inch/1000 unit reel
Use MMFT3055VT3 to order the 13 inch/4000 unit reel

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V _{DSS}	60	Vdc
Drain-to-Gate Voltage (R _{GS} = 1.0 MΩ)	V _{DGR}	60	Vdc
Gate-to-Source Voltage – Continuous – Non-repetitive (t _p ≤ 10 ms)	V _{GS} V _{GSM}	± 20 ± 25	Vdc Vpk
Drain Current – Continuous – Continuous @ 100°C – Single Pulse (t _p ≤ 10 μs)	I _D I _D I _{DM}	1.7 1.4 6.0	Adc Adc Apk
Total PD @ T _A = 25°C mounted on 1" sq. Drain pad on FR-4 bd material Total PD @ T _A = 25°C mounted on 0.70" sq. Drain pad on FR-4 bd material Total PD @ T _A = 25°C mounted on min. Drain pad on FR-4 bd material Derate above 25°C	P _D	2.0 1.7 0.9 6.3	Watts mW/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-55 to 175	°C
Single Pulse Drain-to-Source Avalanche Energy – Starting T _J = 25°C (V _{DD} = 25 Vdc, V _{GS} = 10 Vdc, Peak I _L = 3.4 Apk, L = 10 mH, R _G = 25 Ω)	E _{AS}	58	mJ
Thermal Resistance – Junction to Ambient on 1" sq. Drain pad on FR-4 bd material – Junction to Ambient on 0.70" sq. Drain pad on FR-4 bd material – Junction to Ambient on min. Drain pad on FR-4 bd material	R _{θJA} R _{θJA} R _{θJA}	70 88 159	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T _L	260	°C

This document contains information on a new product. Specifications and information herein are subject to change without notice. E-FET and TMOS V are trademarks of Motorola, Inc. TMOS is a registered trademark of Motorola, Inc.

MMFT3055V

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Drain-to-Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 0.25 mAdc) Temperature Coefficient (Positive)	V _{(BR)DSS}	60 —	— 63	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V _{DS} = 60 Vdc, V _{GS} = 0 Vdc) (V _{DS} = 60 Vdc, V _{GS} = 0 Vdc, T _J = 150°C)	I _{DSS}	— —	— —	10 100	μAdc
Gate-Body Leakage Current (V _{GS} = ± 20 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	100	nAdc

ON CHARACTERISTICS (1)

Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 250 μAdc) Threshold Temperature Coefficient (Negative)	V _{GS(th)}	2.0 —	2.8 5.6	4.0 —	Vdc mV/°C
Static Drain-to-Source On-Resistance (V _{GS} = 10 Vdc, I _D = 0.85 Adc)	R _{DS(on)}	—	0.115	0.13	Ohm
Drain-to-Source On-Voltage (V _{GS} = 10 Vdc, I _D = 1.7 Adc) (V _{GS} = 10 Vdc, I _D = 0.85 Adc, T _J = 150°C)	V _{DS(on)}	— —	— —	0.27 0.25	Vdc
Forward Transconductance (V _{DS} = 8.0 Vdc, I _D = 1.7 Adc)	g _{FS}	1.0	2.7	—	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 25 Vdc, V _{GS} = 0 Vdc, f = 1.0 MHz)	C _{iss}	—	360	500	pF
Output Capacitance		C _{oss}	—	110	150	
Transfer Capacitance		C _{rss}	—	25	50	

SWITCHING CHARACTERISTICS (2)

Turn-On Delay Time	(V _{DD} = 30 Vdc, I _D = 1.7 Adc, V _{GS} = 10 Vdc, R _G = 9.1 Ω)	t _{d(on)}	—	8.0	20	ns
Rise Time		t _r	—	9.0	20	
Turn-Off Delay Time		t _{d(off)}	—	32	60	
Fall Time		t _f	—	18	40	
Gate Charge	(V _{DS} = 48 Vdc, I _D = 1.7 Adc, V _{GS} = 10 Vdc)	Q _T	—	13	20	nC
		Q ₁	—	2.0	—	
		Q ₂	—	5.0	—	
		Q ₃	—	4.0	—	

SOURCE-DRAIN DIODE CHARACTERISTICS

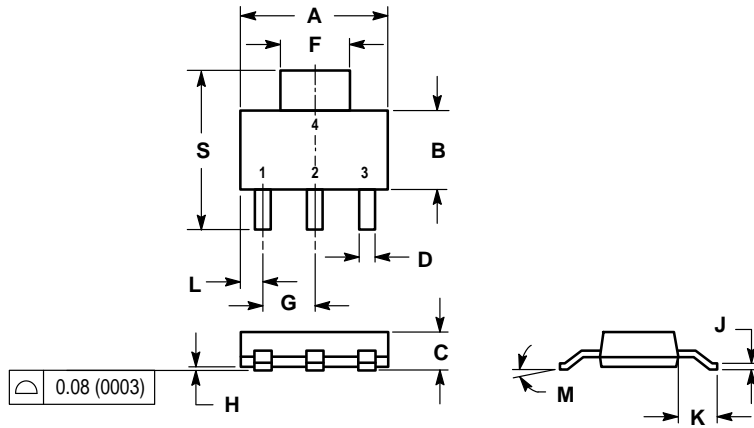
Forward On-Voltage (1)	(I _S = 1.7 Adc, V _{GS} = 0 Vdc) (I _S = 1.7 Adc, V _{GS} = 0 Vdc, T _J = 150°C)	V _{SD}	— —	0.85 0.7	1.6 —	Vdc
Reverse Recovery Time	(I _S = 1.7 Adc, V _{GS} = 0 Vdc, dI _S /dt = 100 A/μs)	t _{rr}	—	40	—	ns
		t _a	—	34	—	
		t _b	—	6.0	—	
Reverse Recovery Stored Charge		Q _{RR}	—	0.089	—	μC

INTERNAL PACKAGE INDUCTANCE

Internal Drain Inductance (Measured from the drain lead 0.25" from package to center of die)	L _D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)	L _S	—	7.5	—	nH

- (1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
 (2) Switching characteristics are independent of operating junction temperature.

PACKAGE DIMENSIONS




- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.249	0.263	6.30	6.70
B	0.130	0.145	3.30	3.70
C	0.060	0.068	1.50	1.75
D	0.024	0.035	0.60	0.89
F	0.115	0.126	2.90	3.20
G	0.087	0.094	2.20	2.40
H	0.0008	0.0040	0.020	0.100
J	0.009	0.014	0.24	0.35
K	0.060	0.078	1.50	2.00
L	0.033	0.041	0.85	1.05
M	0°	10°	0°	10°
S	0.264	0.287	6.70	7.30

- STYLE 3:
 PIN 1. GATE
 2. DRAIN
 3. SOURCE
 4. DRAIN

CASE 318E-04
 ISSUE H

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