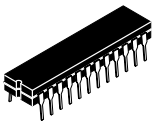
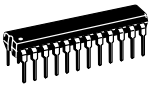
4-Bit Arithmetic Logic Unit/ Function Generator

MC10H181



L SUFFIX
CERAMIC PACKAGE
CASE 758–02



P SUFFIX
PLASTIC PACKAGE
CASE 724–03

FN SUFFIX
PLCC
CASE 776–02

The MC10H181 is a high–speed arithmetic logic unit capable of performing 16 logic operations and 16 arithmetic operations on two four–bit words. Full internal carry is incorporated for ripple through operation.

Arithmetic logic operations are selected by applying the appropriate binary word to the select inputs (S0 through S3) as indicated in the tables of arithmetic/logic functions. Group carry propagate (P_G) and carry generate (G_G) are provided to allow fast operations on very long words using a second order look–ahead. The internal carry is enabled by applying a low level voltage to the mode control input (M).

When used with the MC10H179, full–carry look–ahead, as a second order look–ahead block, the MC10H181 provides high–speed arithmetic operations on very long words.

This 10H part is a functional/pinout duplication of the standard MECL 10K family part with 100% improvement in propagation delay and no increase in power supply current.

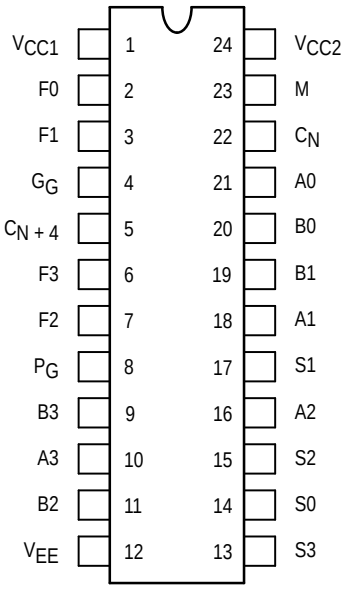
- Improved Noise Margin, 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K – Compatible

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	–8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	–55 to +150 –55 to +165	°C °C

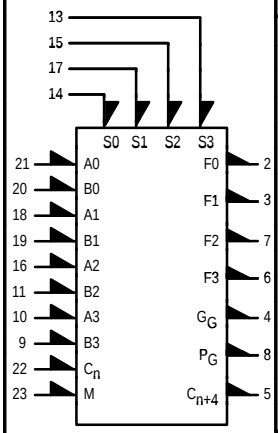
NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package. For PLCC pin assignment, see the Pin Conversion Tables on page 6–11 of the Motorola MECL Data Book (DL122/D).

LOGIC DIAGRAM

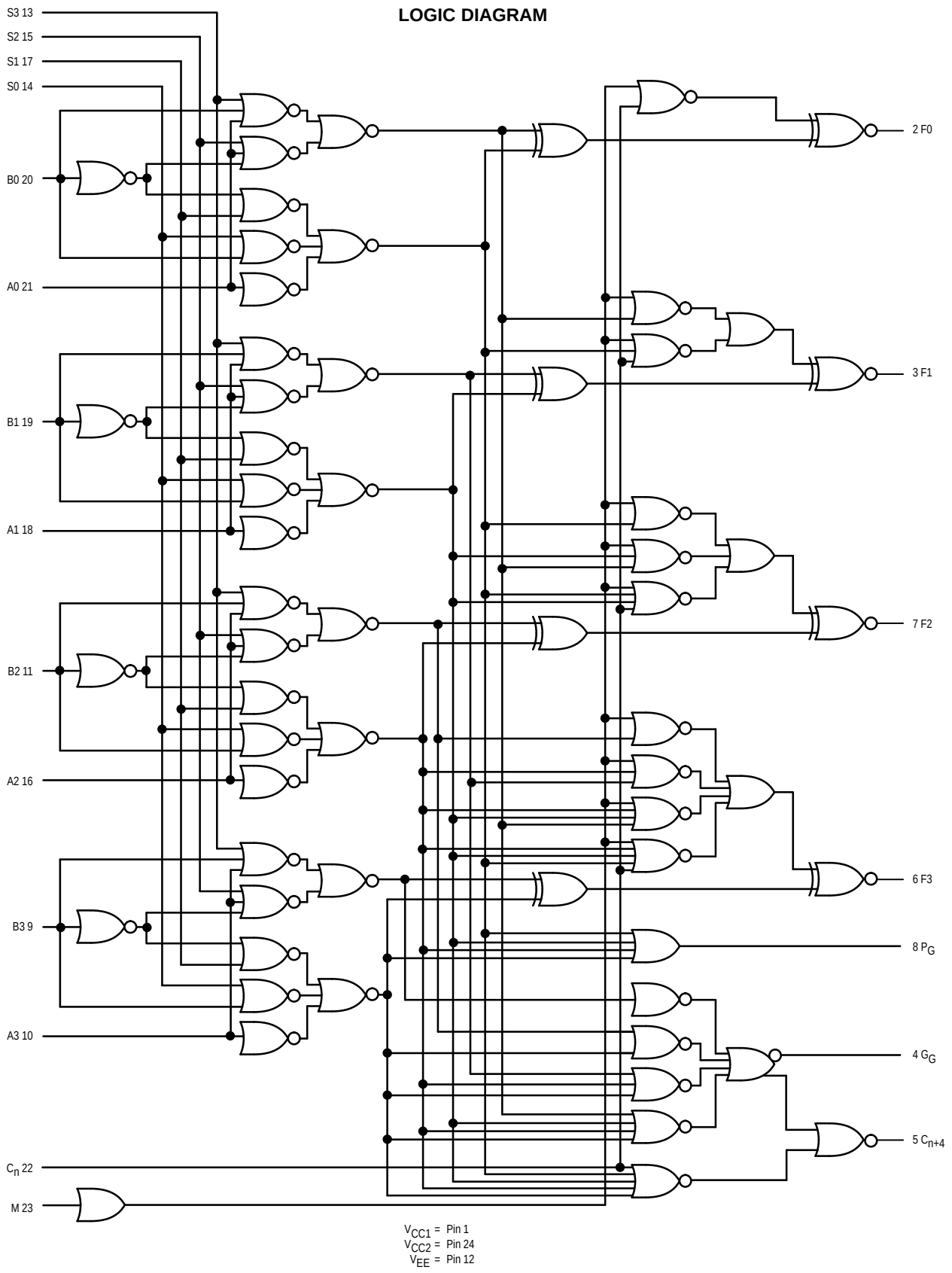


FUNCTION SELECT TABLE

Function Select S3	S2	S1	S0	Logic Functions M is High C = D.C. F	Arithmetic Operation M is Low C_n is low F
L	L	L	L	$F = \overline{A}$	F = A
L	L	L	H	$F = \overline{A} + B$	F = A plus (A • B)
L	L	H	L	$F = A + \overline{B}$	F = A plus (A • $\overline{B}$)
L	L	H	H	F = Logical "1"	F = A times 2
L	H	L	L	$F = \overline{A \cdot B}$	F = (A + B) plus 0
L	H	L	H	$F = \overline{B}$	F = (A + B) plus (A • $\overline{B}$)
L	H	H	L	$F = A \odot B$	F = A plus B
L	H	H	H	$F = A + \overline{B}$	F = A plus (A + B)
H	L	L	L	$F = \overline{A} \cdot B$	F = (A + $\overline{B}$) plus 0
H	L	L	H	$F = A \oplus B$	F = A minus B minus 1
H	L	H	L	F = B	F = (A + $\overline{B}$) plus (A • $\overline{B}$)
H	L	H	H	F = A + B	F = A plus (A + $\overline{B}$)
H	H	L	L	F = Logical "0"	F = minus 1 (two's complement)
H	H	L	H	$F = A \cdot \overline{B}$	F = (A • $\overline{B}$) minus 1
H	H	H	L	F = A • B	F = (A • B) minus 1
H	H	H	H	F = A	F = A minus 1

MOTOROLA

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5.0%) (See Note)

Characteristic	Symbol	0°		+25°		+75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	—	159	—	145	—	159	mA
Input Current High	I_{inH}							µA
Pin 22		—	720	—	450	—	450	
Pins 14,23		—	405	—	255	—	255	
Pins 13,15,17		—	515	—	320	—	320	
Pins 10,16,18,21		—	475	—	300	—	300	
Pins 9,11,19,20		—	465	—	275	—	275	
Input Current Low Pins 9–11, 13–22	I_{inL}	0.5	—	0.5	—	0.3	—	µA
High Output Voltage	V_{OH}	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
Low Output Voltage	V_{OL}	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
High Input Voltage	V_{IH}	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
Low Input Voltage	V_{IL}	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

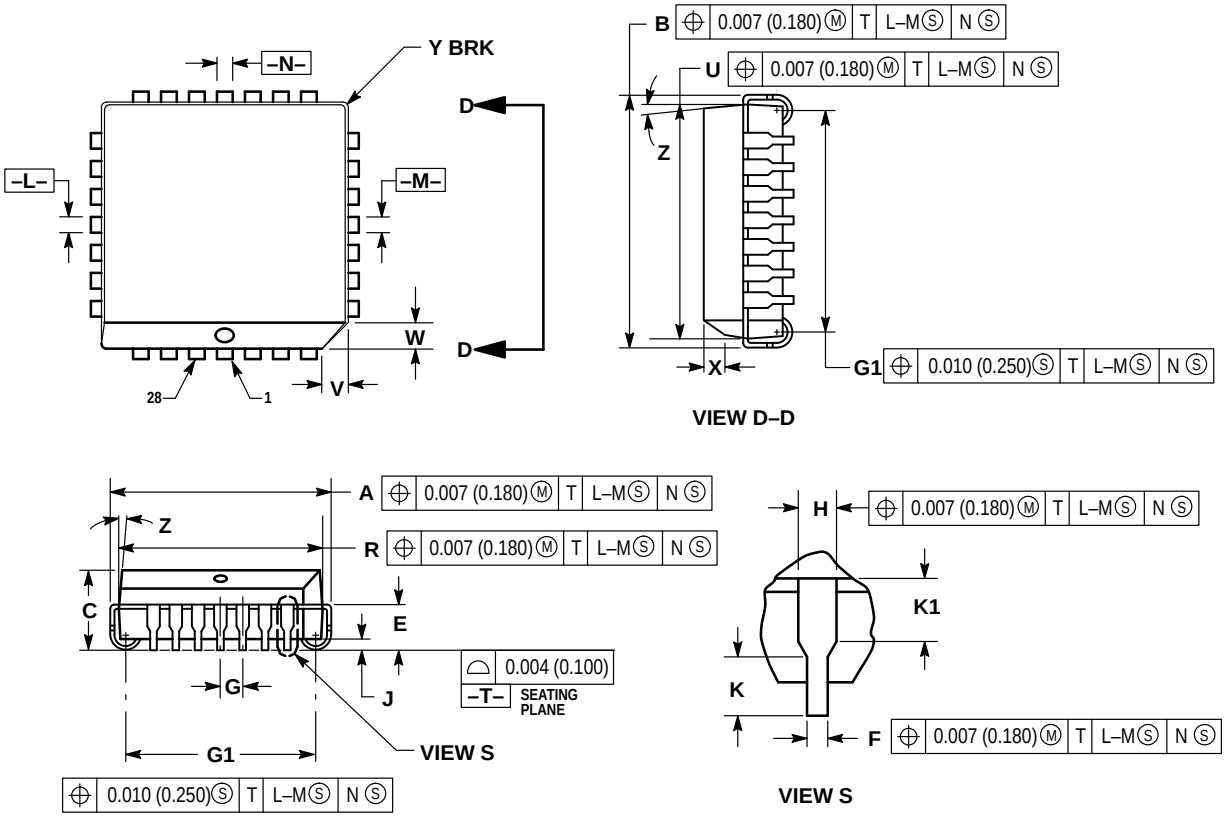
AC PARAMETERS

Characteristic	Symbol	Input	Output	Conditions †	AC Switching Characteristics						
					0°C		+25°C		+75°C		Unit
					Min	Max	Min	Max	Min	Max	
Propagation Delay	t+ +, t– –	C_n	C_{n+4}	A0,A1,A2,A3	0.7	2.0	0.7	2.0	0.7	2.2	ns
Rise Time, Fall Time	t+, t–	C_n	C_{n+4}	A0,A1,A2,A3	0.6	2.0	0.6	2.0	0.7	2.2	ns
Propagation Delay	t+ +, t+ –,	C_n	F1	A0							ns
	t– +, t– –	C_n	F1		1.0	3.0	1.0	3.0	1.2	3.3	
Rise Time, Fall Time	t+, t–	C_n	F1		0.7	2.2	0.7	2.2	0.7	2.4	
Propagation Delay	t+ +, t+ –,	A1	F1								ns
	t– +, t– –	A1	F1		1.5	3.7	1.5	3.7	1.6	4.0	
Rise Time, Fall Time	t+, t–	A1	F1		0.7	2.0	0.7	2.0	0.7	2.2	
Propagation Delay	t+ +, t– –	A1	P_G	S0,S3	1.5	3.7	1.5	3.7	1.6	4.0	ns
Rise Time, Fall Time	t+, t–	A1	P_G	S0,S3	0.9	2.4	0.9	2.4	0.9	2.6	ns
Propagation Delay	t+ +, t– –	A1	G_G	A0,A2,A3,C_n	1.5	3.7	1.5	3.7	1.6	3.9	ns
Rise Time, Fall Time	t+, t–	A1	G_G	A0,A2,A3,C_n	0.7	2.2	0.7	2.2	0.7	2.4	ns
Propagation Delay	t+ –, t– +	A1	C_{n+4}	A0,A2,A3,C_n	1.5	3.6	1.5	3.6	1.6	3.9	ns
Rise Time, Fall Time	t+, t–	A1	C_{n+4}	A0,A2,A3,C_n	0.5	2.0	0.5	2.0	0.5	2.2	ns
Propagation Delay	t+ +, t– +	B1	F1	S3,C_n	2.0	4.5	2.0	4.5	2.1	4.8	ns
Rise Time, Fall Time	t+, t–	B1	F	S3,C_n	0.7	2.3	0.7	2.3	0.7	2.5	ns
Propagation Delay	t+ +, t– –	B1	P_G	S0,A1	1.5	3.8	1.5	3.8	1.6	4.0	ns
Rise Time, Fall Time	t+, t–	B1	P_G	S0,A1	0.7	2.2	0.7	2.2	0.7	2.4	ns
Propagation Delay	t+ +, t– –	B1	G_G	S3,C_n	1.5	3.7	1.5	3.7	1.6	4.0	ns
Rise Time, Fall Time	t+, t–	B1	G_G	S3,C_n	0.7	2.2	0.7	2.2	0.7	2.4	ns
Propagation Delay	t+ –, t– +	B1	C_{n+4}	S3,C_n	2.0	4.0	2.0	4.0	2.1	4.3	ns
Rise Time, Fall Time	t+, t–	B1	C_{n+4}	S3,C_n	0.5	2.0	0.5	2.2	0.5	2.2	ns
Propagation Delay	t+ +, t+ –	M	F1	—	1.5	4.2	1.5	4.2	1.6	4.5	ns
Rise Time, Fall Time	t+, t–	M	F1	—	0.8	2.3	0.8	2.3	0.8	2.5	ns
Propagation Delay	t+ –, t– +	S1	F1	A1,B1	1.5	4.5	1.5	4.5	1.6	4.8	ns
Rise Time, Fall Time	t+, t–	S1	F1	A1,B1	0.7	2.0	0.7	2.0	0.7	2.2	ns
Propagation Delay	t– +, t+ –	S1	P_G	A3,B3	1.5	4.0	1.5	4.0	1.6	4.3	ns
Rise Time, Fall Time	t+, t–	S1	P_G	A3,B3	0.7	2.0	0.7	2.2	0.7	2.4	ns
Propagation Delay	t+ –, t– +	S1	C_{n+4}	A3,B3	1.5	4.1	1.5	4.1	1.6	4.4	ns
Rise Time, Fall Time	t+, t–	S1	C_{n+4}	A3,B3	0.7	2.2	0.7	2.2	0.7	2.4	ns
Propagation Delay	t+ –, t– +	S1	G_G	A3,B3	1.3	4.5	1.3	4.5	1.4	4.8	ns
Rise Time, Fall Time	t+, t–	S1	G_G	A3,B3	0.5	3.2	0.5	3.2	0.5	3.4	ns

† Logic high level (+1.11 Vdc) applied to pins listed. All other input pins are left floating or tied to +0.31 Vdc.
$V_{CC1} = V_{CC2}$ = +2.0 Vdc, V_{EE} = –3.2 Vdc

OUTLINE DIMENSIONS

FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776–02
ISSUE D

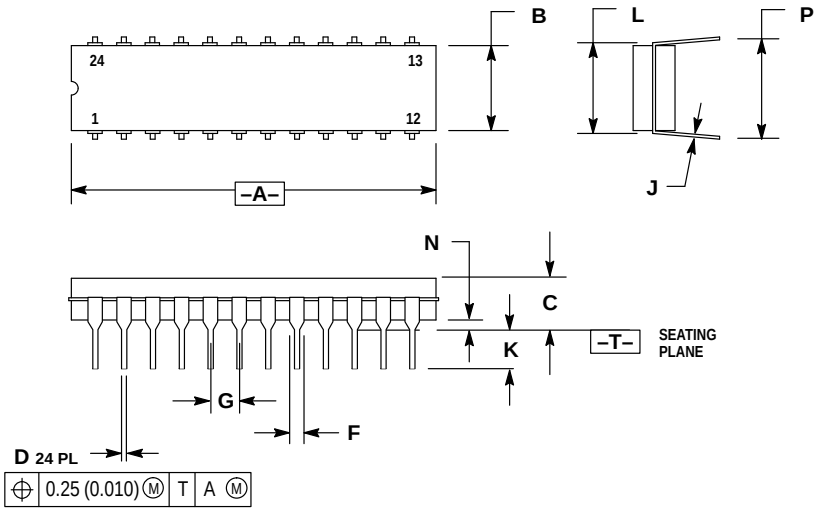


NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

OUTLINE DIMENSIONS

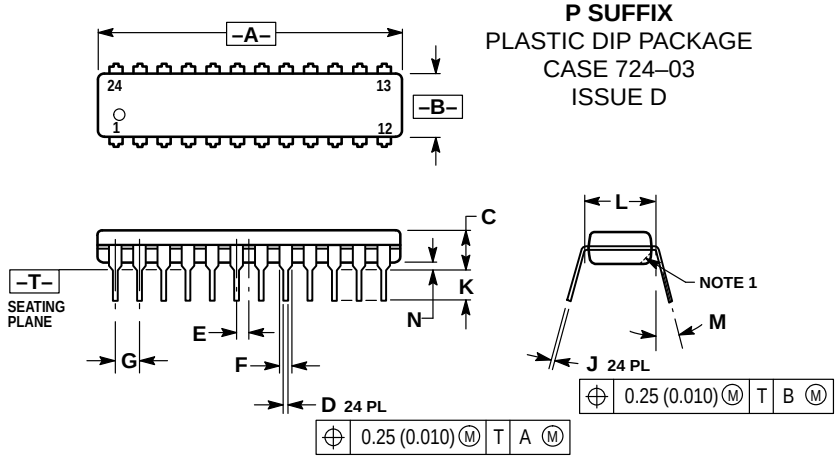
L SUFFIX
CERAMIC DIP PACKAGE
CASE 758–02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.240	1.285	31.50	32.64
B	0.285	0.305	7.24	7.75
C	0.160	0.200	4.07	5.08
D	0.015	0.021	0.38	0.53
F	0.045	0.062	1.14	1.57
G	0.100 BSC		2.54 BSC	
J	0.008	0.013	0.20	0.33
K	0.100	0.165	2.54	4.19
L	0.300	0.310	7.62	7.87
N	0.020	0.050	0.51	1.27
P	0.360	0.400	9.14	10.16

P SUFFIX
PLASTIC DIP PACKAGE
CASE 724–03
ISSUE D



NOTES:
1. CHAMFERED CONTOUR OPTIONAL.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.230	1.265	31.25	32.13
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.020	0.38	0.51
E	0.050 BSC		1.27 BSC	
F	0.040	0.060	1.02	1.52
G	0.100 BSC		2.54 BSC	
J	0.007	0.012	0.18	0.30
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

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