Order this document by MC13282A/D

MOTOROLA

MC13282A

Advance Information

100 MHz Video Processor with OSD Interface

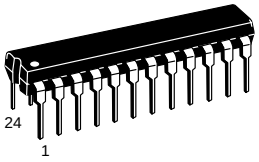
The MC13282A is a three channel wideband amplifier designed for use as a video pre–amp in high resolution RGB color monitors.

Features:

- 4.0 Vpp Output with 100 MHz Bandwidth
- 3.5 ns Rise/Fall Time
- Subcontrast Control for Each Channel
- Blanking and Clamping Inputs
- Contrast Control
- OSD Interface with 50 MHz Bandwidth
- OSD Contrast Control
- Package: NDIP–24

100 MHz VIDEO PROCESSOR WITH OSD INTERFACE

SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 724

ABSOLUTE MAXIMUM RATINGS

Rating	Pin	Value	Unit
Power Supply Voltage – V_{CC}	9	–0.5, 10	Vdc
Power Supply Voltage – Video V_{CC}	17	–0.5, 10	Vdc
Voltage at Video Amplifier Inputs	2, 4, 6, 8, 10, 12	–0.5, +5.0	Vdc
Collector–Emitter Current (Three Channels)	17	120	mA
Storage Temperature	–	–65 to +150	°C
Junction Temperature	–	150	°C

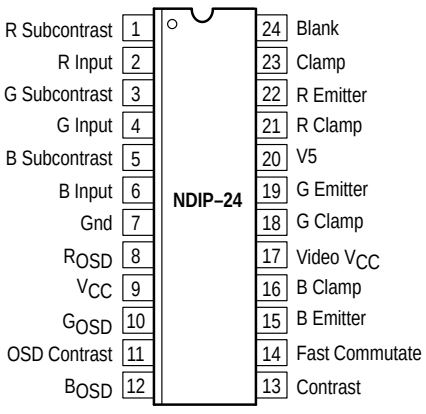
NOTES: 1. Devices should not be operated at these limits. Refer to "Recommended Operating Conditions" section for actual device operation.

2. ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Pin	Min	Typ	Max	Unit
Power Supply Voltage	9, 17	7.6	8.0	8.4	Vdc
Contrast Control	13	0	–	5.0	Vdc
Subcontrast Control	1, 3, 5	0	–	5.0	Vdc
Blanking Input Signal Amplitude	24	0	–	5.0	V
Clamping Input Signal Amplitude	23	0	–	5.0	V
Video Signal Amplitude (with 75 Ω Termination)	2, 4, 6	–	0.7	1.0	Vpp
OSD Signal Input	8, 10, 12	–	TTL	–	V
Collector–Emitter Current (Total for Three Channels)	17	0	–	50	mA
Clamping Pulse Width	23	500	–	–	ns
Operating Ambient Temperature	–	0	–	70	°C

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13282AP	T_A = 0° to +70°C	Plastic DIP

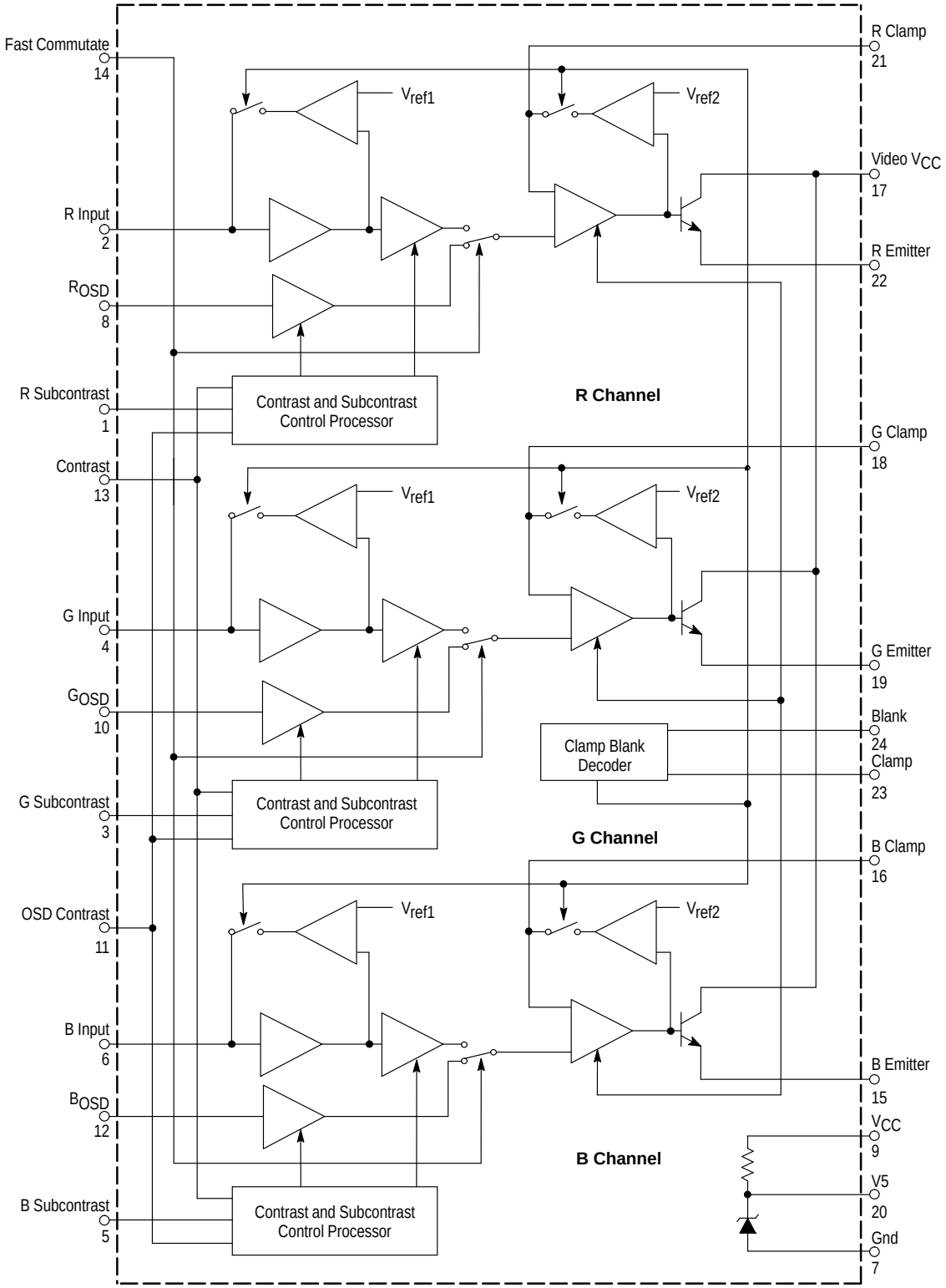
This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (Refer to Test Circuit Figure 1, T_A = 25°C, V_{CC} = 8.0 Vdc.)

Characteristic	Condition	Pin	Min	Typ	Max	Unit
Input Impedance	–	2, 4, 6	100	–	–	kΩ
Internal DC Bias Voltage			–	2.4	–	Vdc
Output Signal Amplitude	V2, V4, V6 = 0.7 Vpp V1, V3, V5, V13 = 5.0 V V14 = 0 V	15, 19, 22	3.6	4.0	–	Vpp
Voltage Gain			–	5.6	–	V/V
Contrast Control	V13 = 5.0 to 0 V V1, V3, V5 = 5.0 V	13	–	–26	–	dB
Subcontrast Control	V1, V3, V5 = 5.0 to 0 V V13 = 5.0 V	1, 3, 5	–	–26	–	dB
Emitter DC Level	–	15, 19, 22	1.0	1.2	1.4	Vdc
Blanking Input Threshold	–	24	–	1.25	–	V
Clamping Input Threshold	–	23	–	3.75	–	V
Video Rise Time	V2, V4, V6 = 0.7 Vpp V_{out} = 4.0 Vpp R_L > 300 Ω, C_L < 5.0 pF	15, 19, 22	–	3.5	–	ns
Video Fall Time			–	3.5	–	
Video Bandwidth	V2, V4, V6 = 0.7 Vpp V1, V3, V5, V13 = 5.0 V V14 = 0 V R_L > 300 Ω, C_L < 5.0 pF	15, 19, 22	–	100	–	MHz
OSD Rise Time	V8, V10, V12 = TTL Level V11 = 5.0 V, V14 = 5.0 V	15, 19, 22	–	7.0	–	ns
OSD Fall Time			–	7.0	–	
OSD Bandwidth	V8, V10, V12 = TTL Level V11 = 5.0 V, V14 = 5.0 V	15, 19, 22	–	50	–	MHz
OSD Propagation Delay	–	–	–	17	–	ns
Power Supply Current	V_{CC}, Video V_{CC} = 8.0 V	9, 17	–	70	–	mA

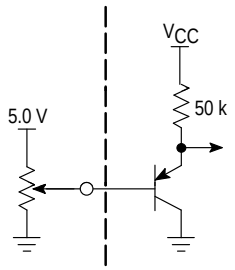
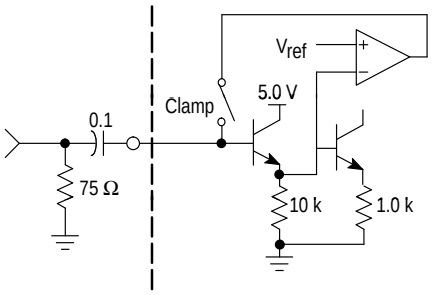
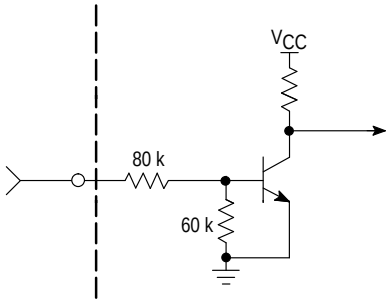
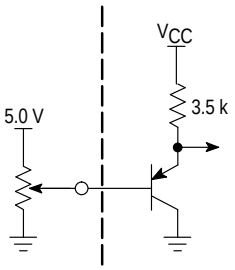
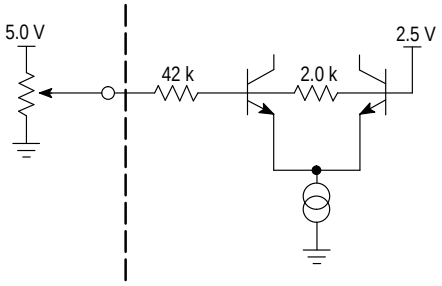
NOTE: It is recommended to use a double sided PCB layout for high frequency measurement (e.g., rise/fall time, bandwidth).

Figure 1. Internal Block Diagram

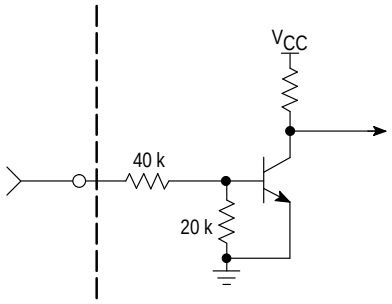
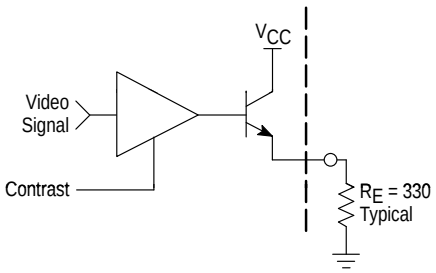
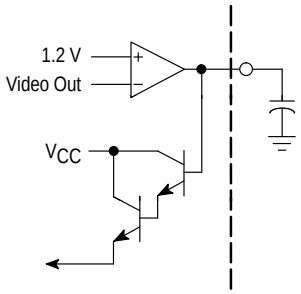
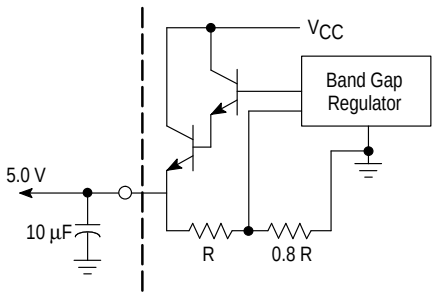


This device contains 272 active transistors.

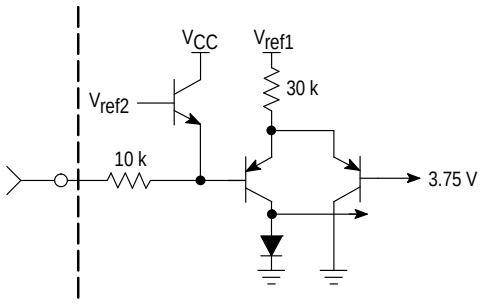
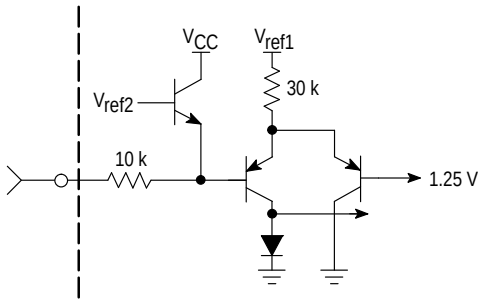
PIN FUNCTION DESCRIPTION

Pin	Name	Equivalent Internal Circuit	Description
1 3 5	R Subcontrast Control G Subcontrast Control B Subcontrast Control		These pin provides a maximum of 26 dB attenuation to vary the gain of each video amplifier separately. Input voltage is from 0 to 5.0 V. Increasing the voltage will increase the contrast level.
2 4 6	R Input G Input B Input		The input coupling capacitor is used for input clamping storage. The maximum source impedance is 100 Ω. Input polarity of the video signal is positive. Nominal 0.7 Vpp input signal is recommended (maximum 1.0 Vpp).
7	Ground		Ground pin. Connect to a clean, solid ground.
8 10 12	R_{OSD} Input G_{OSD} Input B_{OSD} Input		These inputs are standard TTL level.
9	V_{CC}		Connect to 8.0 Vdc supply, ±5%. Decoupling is required at this pin.
11	OSD Contrast		On Screen Display contrast control. Input voltage is from 0 to 5.0 V. Increasing the voltage will increase the contrast of the OSD signal.
13	Contrast		Overall Contrast Control for the three channels. The input range is 0 V to 5.0 V. An increase of voltage increases the contrast.

PIN FUNCTION DESCRIPTION (continued)

Pin	Name	Equivalent Internal Circuit	Description
14	Fast Commutate		This pin is used in conjunction with the RGB OSD inputs. It is a high speed switch used for overlaying text on picture. A logic low selects Pins 2, 4, 6. A logic high selects Pins 8, 10, 12.
15 19 22	B Emitter Output G Emitter Output R Emitter Output		The video outputs are configured as emitter–followers with a driving capability of about 15 mA each. The dc voltage at these three emitters is set to 1.2 V (black level). The dc current through the output stage is determined by the emitter resistors (typically 330 Ω).
16 18 21	B Clamp Capacitor G Clamp Capacitor R Clamp Capacitor		A 100 nF capacitor is connected to each of these pins. The capacitor is used for video output dc restoration.
17	Video V_{CC}		Connect to 8.0 V dc supply, ±5%. This V_{CC} is for the video output stage. It is internally connected to the collectors of the output transistors.
20	5.0 V_{ref} (V5)		5.0 V regulator. Minimum 10 µF capacitor is required for noise filtering and compensation. It can source up to 20 mA but not sink current. Output impedance is ≈ 10 Ω. Recommended for use as a voltage reference only.

PIN FUNCTION DESCRIPTION (continued)

Pin	Name	Equivalent Internal Circuit	Description
23	Clamp		This pin is used for video clamping. The threshold clamping level is 3.75 V.
24	Blank		This pin is used for video blanking. The threshold blanking level is 1.25 V.

FUNCTIONAL DESCRIPTION

The MC13282A is composed of three video amplifiers, clamping and blanking circuitry with contrast and subcontrast controls and OSD interface. Each video amplifier is designed to have a –3.0 dB bandwidth of 100 MHz with a gain of up to about 5.6 V/V, or 15 dB.

Video Input

The video input stages are high impedance and designed to accept a maximum signal of 1.0 Vpp with 75 Ω termination (typically) provided externally. During the clamping period, a current is provided to the input capacitor by the clamping circuit which brings the input to a proper dc level (nominal 2.0 V). The blanking and clamping signals are to be provided externally, with their thresholds sitting at 1.25 V and 3.75 V, respectively.

Video Output

The video output stages are configured as emitter–followers, with a driving capability of about 15 mA for each channel. The dc voltage at these three emitters is set to 1.2 V (black level). The dc current through each output stage is determined by the emitter resistor (typically 330 Ω).

Contrast Control

The contrast control varies the gain of three video amplifiers from a minimum of 0.3 V/V to a maximum of 5.6 V/V when all subcontrast levels are set to 5.0 V.

Subcontrast Control

Each subcontrast control provides a maximum of 26 dB attenuation on each video amplifier separately.

OSD Interface

The three OSD inputs are TTL compatible and have a typical bandwidth of 50 MHz. A fast commutate pin is provided to select either the video or the OSD inputs as the source for the outputs. OSD contrast control is also provided to set the amount of gain required when OSD inputs are selected.

Clamp Pulse Input

The clamping pulse is provided externally, and the pulse width must be no less than 500 ns.

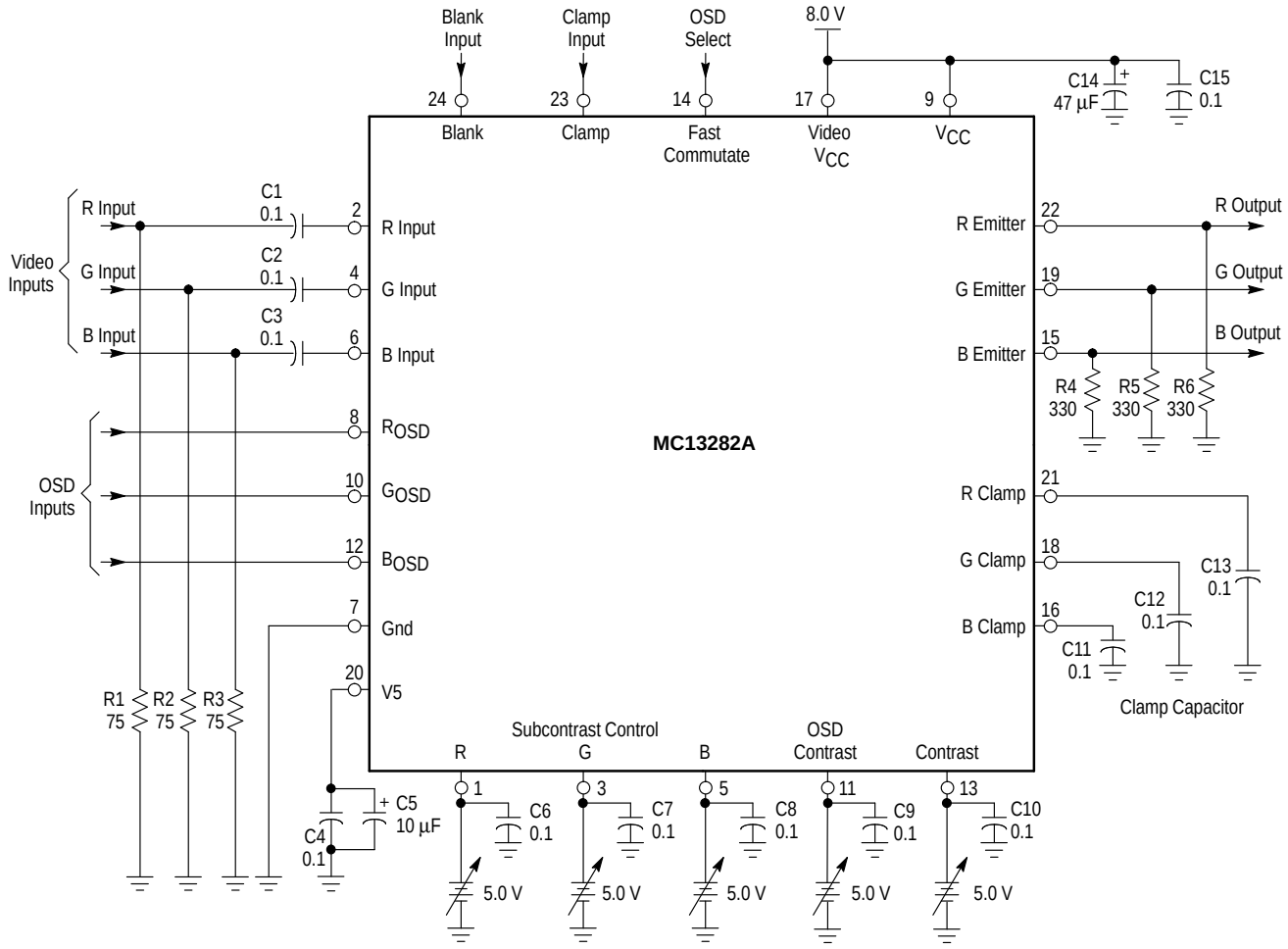
Blank Pulse Input

The blanking pulse is used to blank the video signal during the horizontal sync period, or used as a control pin for video mute function.

Power Supplies

V_{CC} and Video V_{CC} supplies are to be 8.0 V ±5%.

Figure 2. Test Circuit



APPLICATION INFORMATION

PCB Layout

Care should be taken in the PCB layout to minimize the noise effects. The most sensitive pins are V_{CC} (9), Video V_{CC} (17), V5 (20), Clamp (16, 18, 21). It is strongly recommended to make a ground plane and connect V_{CC}/Video V_{CC} and ground traces to the power supply directly. Separate power supply traces, should be used for V_{CC} and Video V_{CC} and decoupling capacitors should be connected as close as possible to the device. Multi–layer ceramic and tantalum capacitors are recommended. Pin 20 (V5) is designed as a 5.0 V voltage reference for contrast, RGB subcontrast and OSD contrast controls, so the same precaution for V_{CC} should be also applied at this pin. The Clamp capacitors at Pins 16,18 and 21 should be connected to ground close to IC's ground Pin 7 or power supply ground. The copper trace of the video signal inputs and outputs should be as short as possible and separated by ground traces to avoid any RGB cross–interference. A double sided PCB should be used to optimize the device's performance.

RGB Input and Output

The RGB output stages are designed as emitter–followers to drive the CRT driver circuitry directly. The emitter resistors used is 330 Ω (typically) and the driving current is 15 mA maximum for each channel. The loading impedance connected to the output stages should be greater than 330 Ω and less than 5.0 pF for optimum performance (e.g., rise/fall time, bandwidth, etc.). Decreasing the resistive load will reduce the rise/fall time by increasing the driving current, but the output stage may be damaged due to increasing power dissipation at the same time. The frequency response is affected by the loading capacitance. The typical value is 3.0 to 5.0 pF. Figure 4 shows a typical interface with a video output driver. For a high resolution color monitor application, it is recommended to use coaxial cable or shielded cable for input signal connections.

Clamp and Blank Input

The clamp input is normally (except for Sync–on–Green) connected to a positive horizontal sync pulse, and has a threshold level of 3.75 V. It is used as a timing reference for the dc restoration process, so it cannot be left open. If Sync–on–Green timing mode is used, the clamping pulse should be located at horizontal back porch period instead of horizontal sync tip. Otherwise, the black level will be clamped at an incorrect voltage.

The blank input is used as a video mute, or horizontal blanking control, and is normally connected to a blanking

pulse generated from the flyback or from an MCU. The threshold level of 1.25 V. The blanking pulse width should be equal to the flyback retrace period to make sure that the video signal is blanked properly during retrace. It is necessary to limit the amplitude, and avoid any negative undershoots if the flyback pulse is used. This Blanking input pin cannot accept a negative voltage. This pin should be grounded if it is not used.

OSD interface

Figure 3 show a typical application with an OSD device (MC141540). The MC141540 OSD and FC outputs are TTL compatible, and therefore interface directly with MC13282A. Level shifting circuitry is not needed. The MC141540 is a digital device, controlled by an MCU. Therefore, separate power supply runs to the MC141540 and to the MC13282A are recommended. Care should be taken in the PC board layout to prevent digital noise from entering the analog portions of MC13282A.

Normally the OSD switching is done during the active video time. It is recommended that the Fast Commutate pin not be activated during the horizontal sync time.

Figure 3. Interfacing with OSD Device

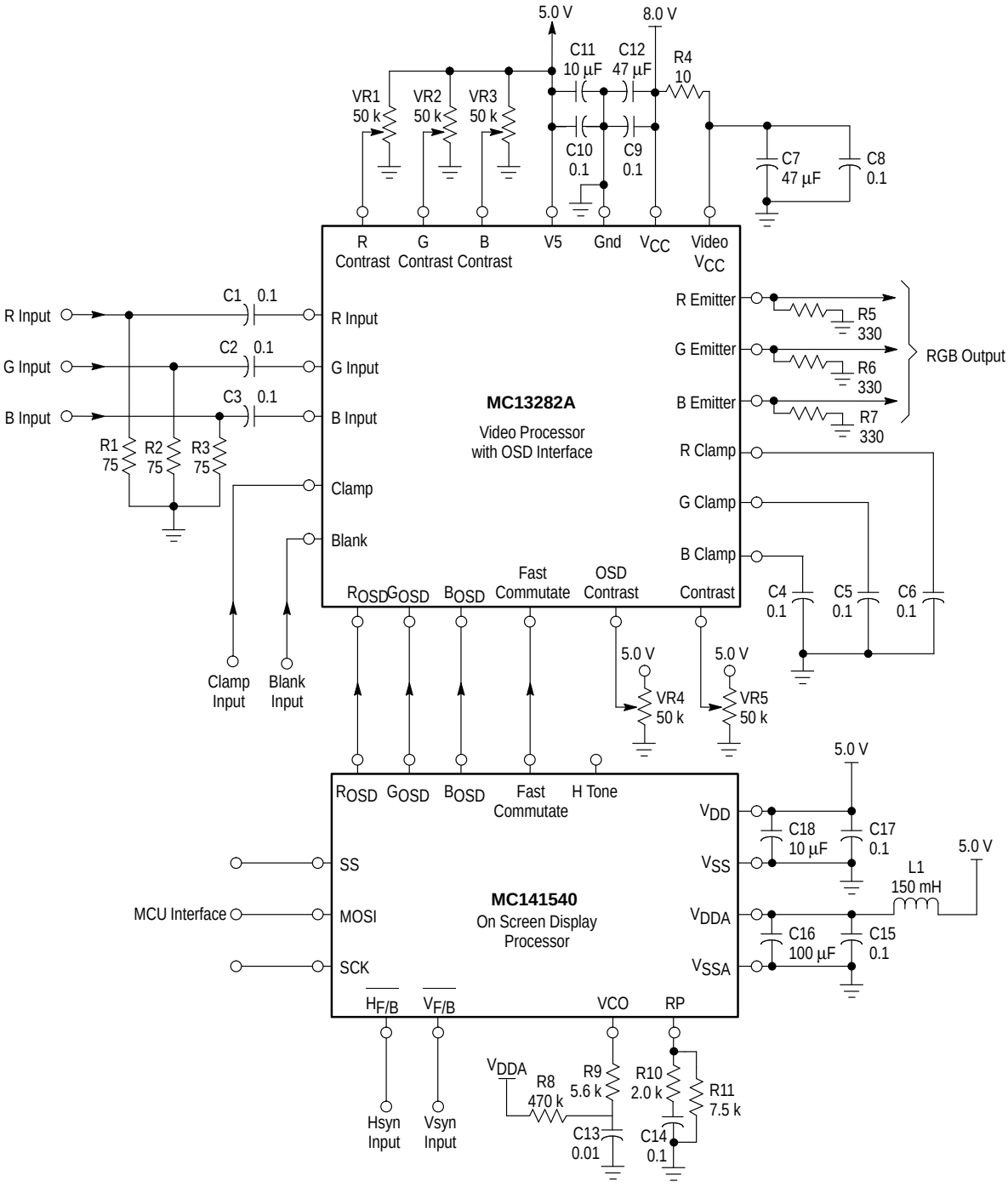


Figure 4. Interfacing with Video Output Drivers

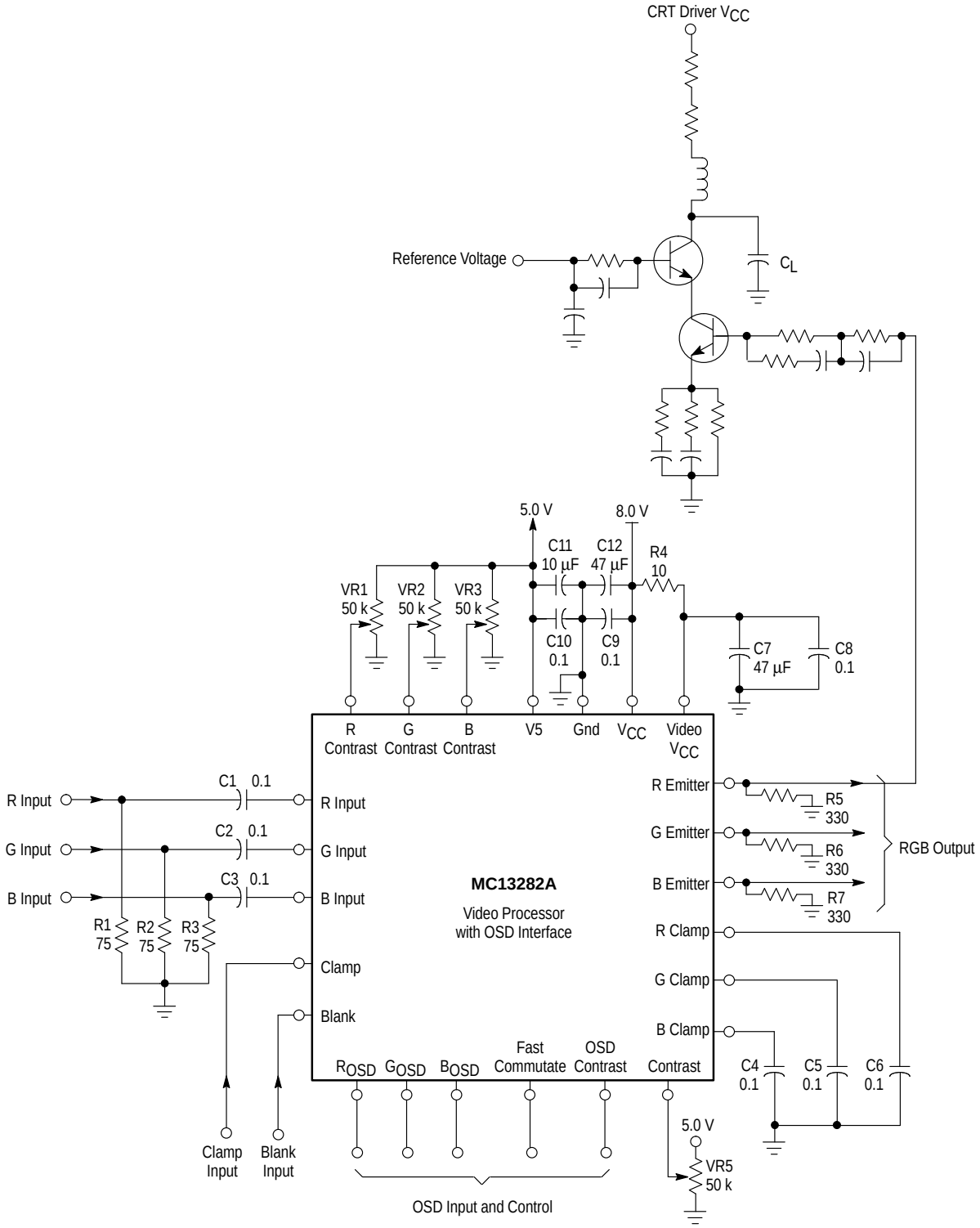


Figure 5. RGB In/Out Linearity

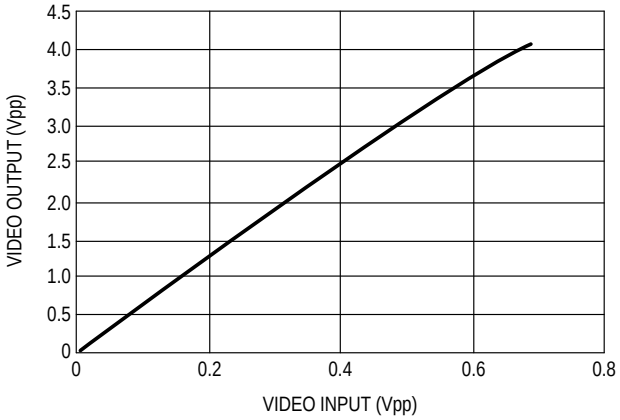


Figure 6. Color Contrast

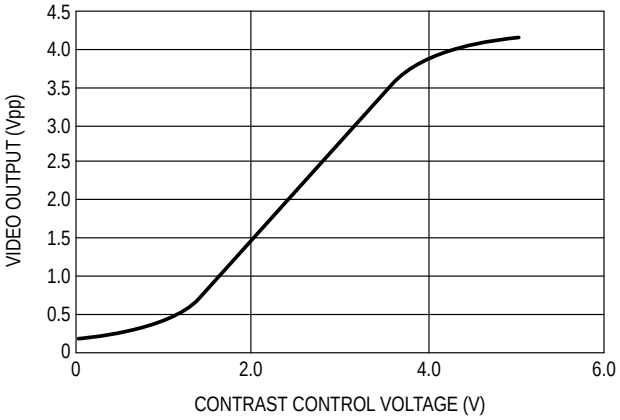


Figure 7. Subcontrast Control

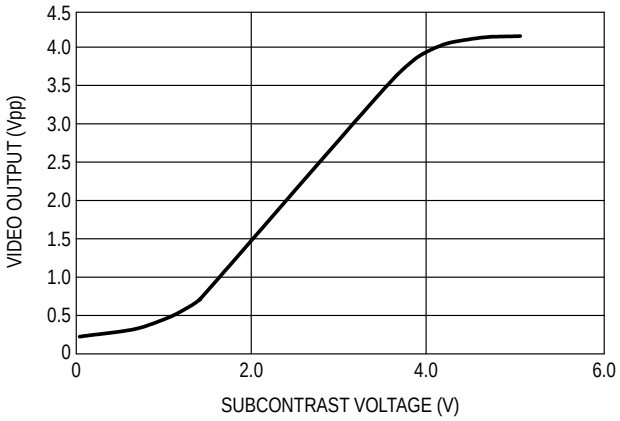


Figure 8. OSD Contrast Control

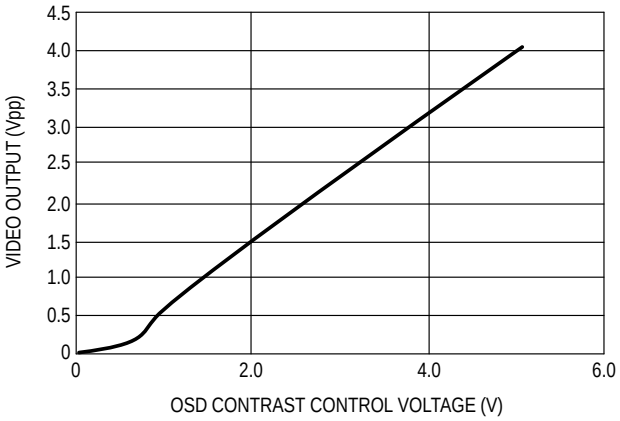


Figure 9. Crosstalk From Green to Red and Blue Channels

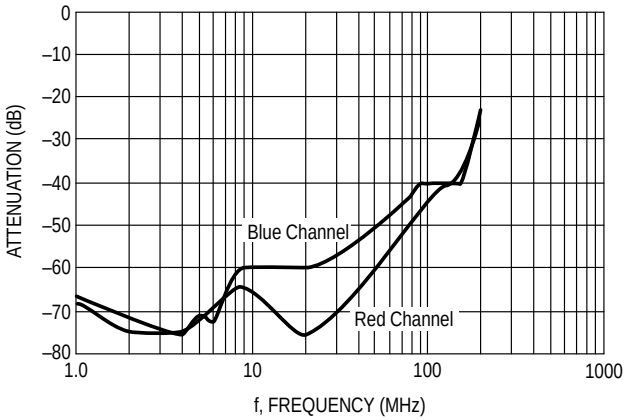
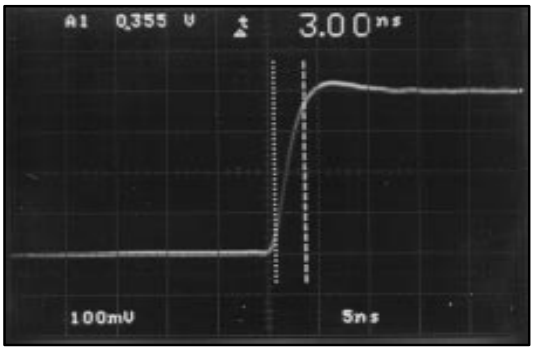
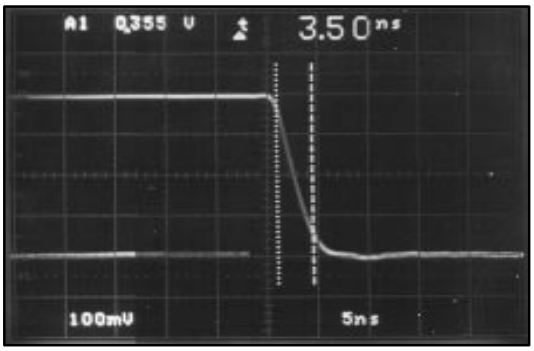


Figure 10. Rise Time



100 mV/DIV
5.0 ns/DIV
10x PROBE

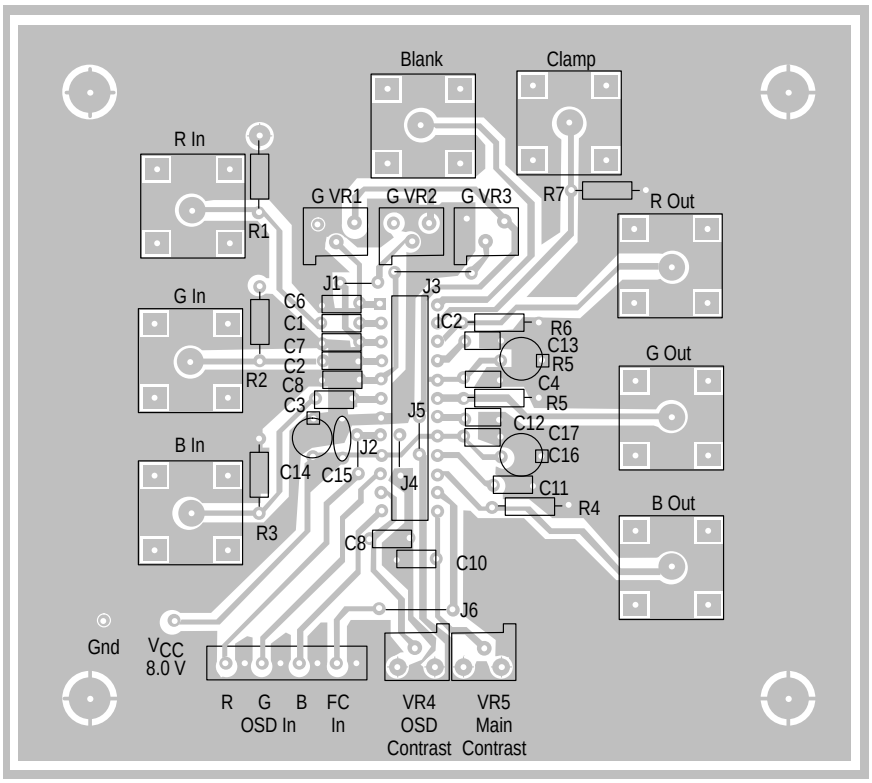
Figure 11. Fall Time



100 mV/DIV
5.0 ns/DIV
10x PROBE

NOTE: Recommended to use a double sided PCB without any socket for rise/fall time measurements, using an input pulse with 1.5 ns rise/fall time and an active probe with 1.7 pF capacitance loading.

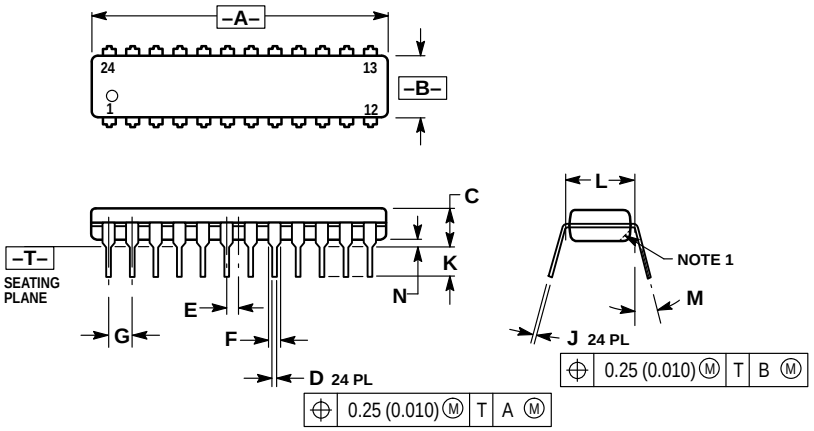
Figure 12. Single Sided PCB Layout (Component Side)



NOTE: J = Jumper

OUTLINE DIMENSIONS

P SUFFIX
PLASTIC PACKAGE
CASE 724–03
ISSUE D



NOTES:
1. CHAMFERED CONTOUR OPTIONAL.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.230	1.265	31.25	32.13
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.020	0.38	0.51
E	0.050 BSC		1.27 BSC	
F	0.040	0.060	1.02	1.52
G	0.100 BSC		2.54 BSC	
J	0.007	0.012	0.18	0.30
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

How to reach us:
USA / EUROPE / Locations Not Listed: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447 or 602–303–5454

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–81–3521–8315

ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298