Product Preview
# Advanced PAL Comb Filter-II (APCF-II)

The Advanced PAL Comb Filter–II is a video signal processor for VCRs, LDPs, and TVs. It separates the Luminance Y and Chrominance C signal from the NTSC/PAL composite signal by using digital signal processing techniques which minimize dot–crawl and cross–color. The built–in 4xFSC PLL circuit allows a subcarrier signal input, which generates 4xFSC clock for video signal processing. This filter allows a video signal input of an extended frequency bandwidth by using a 4xFSC clock. The built–in vertical enhancer circuit reduces noise and dot crawl on the Luminance Y signal. The built–in A/D and D/A converters allow easy connection to analog video circuits.

- Built–In High Speed 8–Bit A/D Converter
- Four Line Memories (4540 Bytes)
- Advanced Comb–II Process
- Built–In Vertical Enhancer
- Vertical Dot Reduction Process
- Two Built–In High Speed 8–Bit D/A Converters
- Built–In 4xFSC PLL Circuit
- Built–In Clamp Circuit
- Digital Interface Mode
- On–Chip Reference Voltage for A/D Converter
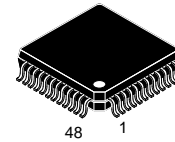
MC141627

FT SUFFIX
QFP PACKAGE
CASE 898

48   1

ORDERING INFORMATION
MC141627FT   Quad Flat Package (QFP)

PIN ASSIGNMENT
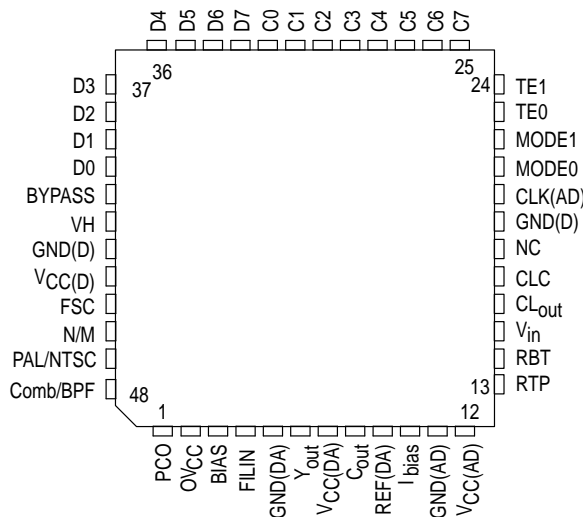
NC = NO CONNECTION

MOTOROLA

BLOCK DIAGRAM
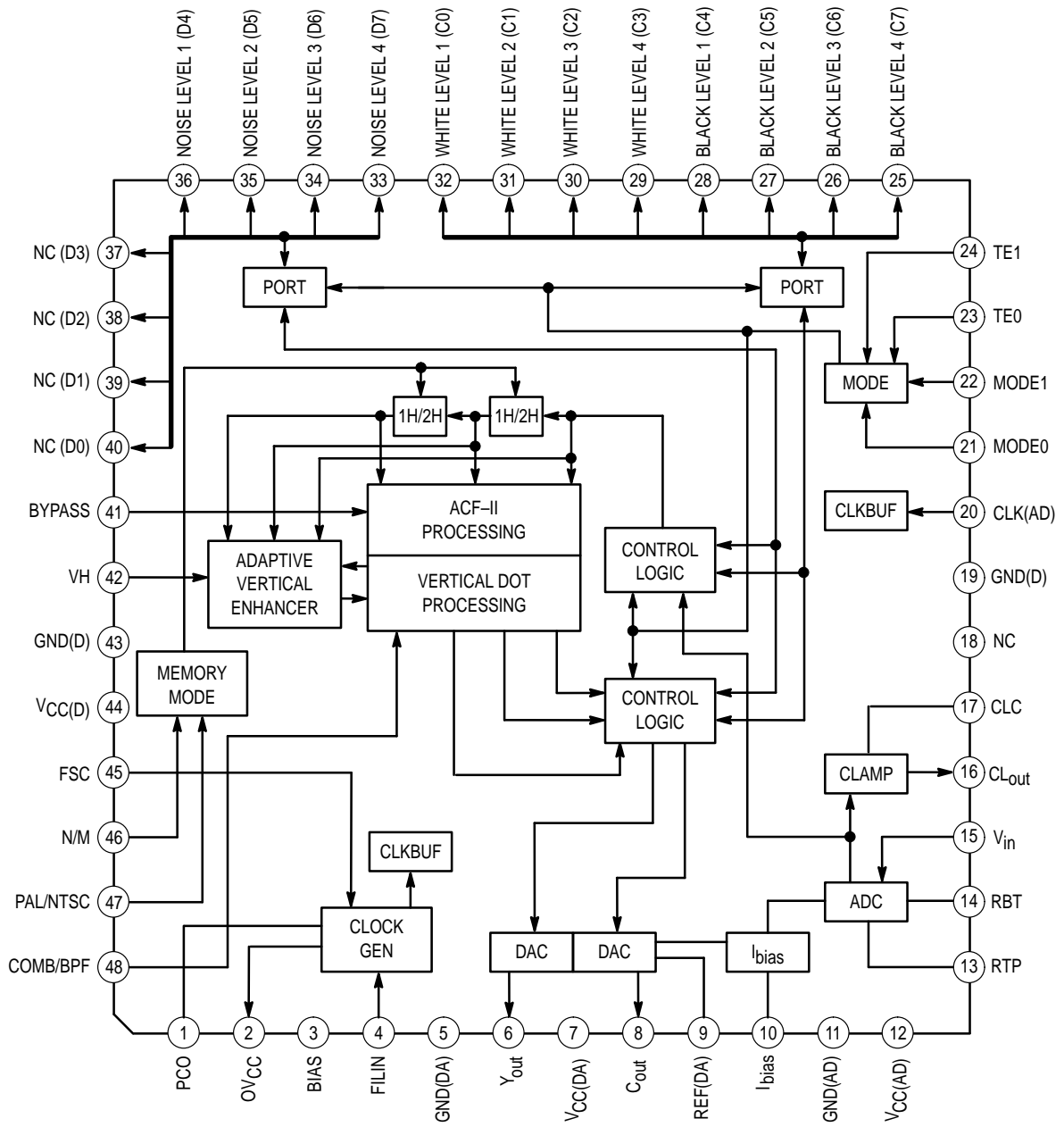
*( ): Digital input mode

ABSOLUTE MAXIMUM RATINGS*

Characteristic	Symbol	Value	Unit
DC Supply Voltage (Referenced to GND)	V_{CC}	− 0.5 to + 7.0	V
DC Input Voltage (Referenced to GND)	V_{in}	− 1.5 to V_{CC} + 1.5	V
DC Output Voltage (Referenced to GND)	V_{out}	− 0.5 to V_{CC} + 0.5	V
DC Input Current (per Pin)	I_{in}	± 20	mA
DC Output Current (per Pin)	I_{out}	± 25	mA
Power Dissipation	P_D	750	mW
Storage Temperature	T_{stg}	− 65 to + 150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

GENERAL ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C, Unless Otherwise Noted)

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{CC}*	4.75	5.0	5.25	V	
Operating Supply Current (at Normal Mode)	I_{CC}	—	65	100	mA	
Operating Power Dissipation (at Normal Mode)	P_D	—	325	525	mW	
Ambient Operating Temperature	T_A	− 20	—	75	°C	

*$V_{CC(AD)}$, $V_{CC(DA)}$, $V_{CC(D)}$ voltage.

CLOCK INPUT ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C, Unless Otherwise Noted)

Characteristic		Symbol	Min	Typ	Max	Unit	Notes
Subcarrier Input Frequency		f_c	—	4.43618	—	MHz	1
Clock Frequency		CLK	—	17.734475	—	MHz	2
FSC Clock Input Level		V_{fc}	1	—	—	V p–p	3
High Level Input Voltage	CLK(AD)	V_{ICH}	3.5	—	—	V	4
Low Level Input Voltage	CLK(AD)	V_{ICL}	—	—	1.1	V	4
Clock Duty Cycle	CLK/CLK(AD)	Dty	45	50	55	%	4

NOTES:
1. Color subcarrier input [FSC = (455/2) fh] locked on the burst signal of the input video signal. AC coupling input by external capacitor.
2. The internal circuit operates by 4 times clock using FSC pin input at normal (FSC) mode.
   The internal circuit operates by FSC pin input clock at expected normal (FSC) mode.
3. Sine wave input.
4. CLK(AD) is available only during digital input comb filter mode.

ADC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Resolution	—	—	—	8	Bits
Integral Nonlinearity	INL	—	± 1.0	± 1.5	LSB
Differential Nonlinearity	DNL	—	± 0.5	± 1.0	LSB
Top Reference Level	V_{TPS}	2.4	2.5	2.6	V
Bottom Reference Level	V_{BTS}	0.4	0.5	0.6	V
Maximum Analog Input Range During Self Reference	V_{ins}	1.9	2.0	2.1	V p–p

DIGITAL ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic		Symbol	Min	Typ	Max	Unit
High Level Input Voltage	MODE0, MODE1, TE0, TE1, BK, VH, C0 – C7, D0 – D7	V_{IH}	3.15	—	—	V
Low Level Input Voltage	MODE0, MODE1, TE0, TE1, BK, VH, C0 – C7, D0 – D7	V_{IL}	—	—	1.1	V
Input Leakage Current [V_{in} = $V_{CC(D)}$ or GND(D)]	MODE0, MODE1, TE0, TE1, BK, VH, C0 – C7, D0 – D7	I_{inl}	—	—	± 10	µA
Data Setup Time (at Digital Input Comb Filter Mode)	D0 – D7	t_{ds}	0	—	—	ns
Data Hold Time (at Digital Input Comb Filter Mode)	D0 – D7	t_{dh}	20	—	—	ns
Data Input Rise Time (at Digital Input Comb Filter Mode)	D0 – D7	t_r	—	—	10	ns
Data Input Fall Time (at Digital Input Comb Filter Mode)	D0 – D7	t_f	—	—	10	ns

FILTERING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Y/C Separation	—	40	—	—	dB
Band–Pass Filter Bandwidth (at – 3 dB) [( ): NTSC]	—	—	± 0.90 (± 0.75)	—	MHz

DAC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Resolution	—	—	—	8	Bits
Integral Nonlinearity	INL	—	—	± 1	LSB
Differential Nonlinearity	DNL	—	—	± 0.5	LSB
Analog Output Voltage, Y_{out}	V_{YO}	1.1	1.2	1.3	V p–p
Analog Output Voltage, C_{out}	V_{CO}	1.1	1.2	1.3	V p–p
Full Scale Voltage, Y_{out}	V_{YFS}	1.3	1.5	1.7	V
Full Scale Voltage, C_{out}	V_{CFS}	1.3	1.5	1.7	V
Zero Scale Voltage, Y_{out}	V_{YZS}	0.1	0.3	0.5	V
Zero Scale Voltage, C_{out}	V_{CZS}	0.1	0.3	0.5	V
Output Impedance	Z_O	—	100	300	Ω

ADC – DAC GENERAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Voltage Gain		—	– 4.4	—	dB
Output Bandwidth (at – 3 dB at PAL)		6.4	7.3	—	MHz
Differential Gain	DG	—	—	5	%
Differential Phase	DP	—	—	5	Deg
Bias Current (at I_{bias} = 10 kΩ)	I_{bias}	—	135	—	μA

CLAMP CIRCUIT CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Clamp Mode Output Voltage*	V_{clys}	—	0.6	—	V

* Output of CL_{out} when connecting $V_{in} – CL_{out}$.

BK/VH CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Bypass Switching Time, at Normal Mode		—	9	—	Clock
VH Switching Time, at Normal Mode		—	4	—	Clock
Comb/BPF Switching Time, at Normal Mode		—	16	—	Clock

VERTICAL ENHANCER LEVEL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Noise Slice Level, at Normal Mode		0	6	15	Bits
White Enhance Level, at Normal Mode		0	10	15	Bits
Black Enhance Level, at Normal Mode		0	11	15	Bits

GENERAL SIGNAL DELAY (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

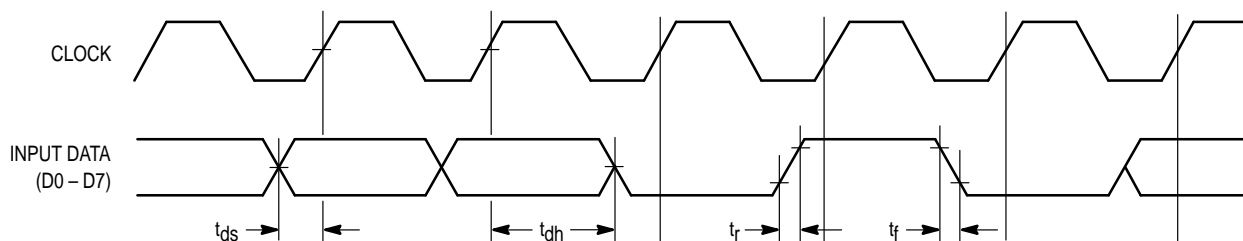| Characteristic	Symbol	Min	Typ	Max	Unit
PAL B/G/H/I Mode (2299.5 Clock)		—	129.66	—	μs
NTSC Mode (939.5 Clock)		—	65.62	—	μs
PAL N Mode (1867.5 Clock)		—	130.34	—	μs
PAL M Mode (1851.5 Clock)		—	129.45	—	μs

Figure 1. Digital Signal Input Timing Diagram (During Digital Input Comb Filter Mode)

Clamp Circuit Characteristics (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Clamp Mode Output Voltage, V_{cly} (Non–input when connecting $V_{in} – CL_{out}$)

$$V_{cly} = (V_{TP} – V_{BT}) (N + 1) / 256 + V_{BT} ± 50 \text{ mV}$$

where N = Clamp Code Input (N < 255)

- If the calculated value of the output voltage, $V_{cly} > V_{clys}$, then $V_{cly} = V_{clys}$

- Clamp Value N is fixed, N = 4.

PIN DESCRIPTIONS

Pin	Pin Name	Function
1	PCO	Phase comparator output.
2	OV_{CC}	Power supply for VCO.
3	BIAS	Reference for VCO. Generally connected to GND(D) through an external resistor.
4	FILIN	VCO controlled voltage input. Generally connected to PCO through an external loop filter.
5	GND(DA)	GND for D/A converter.
6	Y_{out}	Luminance signal output.
7	$V_{CC(DA)}$	Power supply for D/A converter.
8	C_{out}	Chrominance signal output.
9	REF(DA)	Reference for D/A converter. Generally connected to GND(DA) through a multi–layer ceramic capacitor (0.1 µF).
10	I_{bias}	Bias circuit current control for A/D, D/A converters. Generally connected to GND(DA) through an external resistor.
11	GND(AD)	GND for A/D converter.
12	$V_{CC(AD)}$	Power supply for A/D converter.
13	RTP	Top reference for A/D converter. Supplies top reference voltage internally.
14	RBT	Bottom reference for A/D converter. Supplies bottom reference voltage internally.
15	V_{in}	A/D converter input.
16	CL_{out}	Voltage output for clamp. Clamps an input signal by connecting with V_{in} and inputs the video signal by ac coupling.
17	CLC	Clamp time constant setting pin.
18	NC	No connection.
19	GND(D)	GND for digital circuit.
20	CLK(AD)	CLK input for A/D converter. Available only during digital input comb filter mode and a portion of test mode. Input level is CMOS level.
21, 22	MODE0, MODE1	Mode inputs. GND level during normal (FSC) mode.
23, 24	TE0, TE1	Test mode inputs. Generally GND level.
25	C7	Vertical enhancer level at normal mode. Generally $V_{CC(D)}$ level.
26 – 28	C6 – C4	Vertical enhancer level at normal mode. Generally GND(D) level.
29	C3	Vertical enhancer level at normal mode. Generally $V_{CC(D)}$ level.
30 – 32	C2 – C0	Vertical enhancer level at normal mode. Generally GND(D) level.
33	D7	Vertical enhancer level at normal mode. Generally $V_{CC(D)}$ level.
34 – 36	D6 – D4	Vertical enhancer level at normal mode. Generally GND(D) level.
37 – 40	D3 – D0	NC pin at normal mode. Generally GND(D) level.
41	Bypass	Non–YC separation processing mode. Generally GND(D) level.
42	VH	Vertical enhancer circuit mode. Generally GND(D) level.
43	GND(D)	GND for digital circuit.
44	$V_{CC(D)}$	Power supply for digital circuit.
45	FSC	CLK input. ac coupling input by external capacitor. Normal (FSC) mode: Subcarrier. Normal (4xFSC) mode: 4*Subcarrier.
46	N/M	PAL N/PAL M setting pin. Generally GND level.
47	PAL/NTSC	PAL/NTSC setting pin. Generally GND level (PAL mode).
48	Comb/BPF	Comb/BPF setting pin. Generally GND level (comb filter mode).

DEVICE DESCRIPTION

INTRODUCTION

The Advanced PAL Comb Filter–II is a video signal processor for VCRs, LDPs, and TVs. It separates the Luminance Y and Chrominance C signal from the NTSC/PAL composite signal by using digital signal processing techniques which minimize dot–crawl and cross–color. The built–in 4xFSC PLL circuit allows a subcarrier signal input, which generates a 4xFSC clock for video signal processing. This filter allows a video signal input of an extended frequency bandwidth by using a 4xFSC clock. The built–in vertical enhancer circuit reduces noise and dot crawl on the Luminance Y signal. The built–in A/D and D/A converters allow easy connection to analog video circuits.

DESCRIPTION

The simplified block diagram of the Advanced Comb Filter–II chip is shown at the beginning of this data sheet. There are five major functions represented in this block diagram. The first block is the A/D conversion block. The high speed 8–bit binary analog–to–digital converter converts the incoming analog video signal to an 8–bit binary data stream. The conversion frequency is 14.3 MHz/17.7 MHz for NTSC/PAL, which is four times the color subcarrier frequency.

The second block contains the Advanced Comb Filter–II algorithm. The digital data from the A/D converter is processed by the algorithm of the Advanced Comb Filter–II. The composite video is filtered by the band–pass filter (BPF) and separated into the Luminance Y and Chrominance C signals.

The third block is the vertical enhancer circuit block. By comparing pixel information from the vertical dot processing block, the vertical enhancer emphasizes the vertical picture outline.

The fourth block is the digital–to–analog conversion block. Two 8–bit D/A converters convert the luminance and chrominance into analog outputs. The conversion frequency is four times the subcarrier signal (14.3 MHz/17.7 MHz). The chrominance analog output is biased with a dc offset of half the value of the D/A converter reference.

The fifth block is a 4xFSC PLL CLK generation circuit. This block generates a clock signal that is four times the subcarrier signal. This signal is locked to the signal input on the FSC pin. This signal may be selected to equal FSC or 4xFSC.

A/D Converter

The composite video signal input is converted to the digital code by the high speed 8–bit A/D converter. The A/D converter reference has a self–bias function which generates V_{TP} = 2.5 V, V_{BT} = 0.5 V. This allows the A/D converter to function without an external reference circuit.

Clamp Voltage Regulating Circuit

The input video signal may be either dc or ac coupled. By connecting V_{in} to CL_{out}, the internal clamp circuit will provide dc restoration. The clamp voltage regulating circuit sync tip clamps the input video signal and compares it to the digital value of the clamp level ($04) with the A/D converter output code. The clamp voltage, CL_{out}, sets the dc input level when V_{in} and CL_{out} are interconnected.

Advanced Comb Filter–II

The Advanced PAL Comb Filter–II is a digital comb filter developed for use in the NTSC/PAL system. The vertical correlation circuit provides high picture quality and high resolution and requires no adjustment for its Y/C separation. The clock frequency is 14.3 MHz, which is four times the NTSC subcarrier.

The BYPASS pin can be used to select between the composite signal output without Y/C separation and the Y/C signal output. Table 1 shows the relationship of the BYPASS pin and each output.

Table 1. BYPASS Function

BYPASS Pin	Y_{out}	C_{out}
L	Luminance	Chrominance
H	Composite	Composite

Adaptive Vertical Enhancer Circuit

The vertical enhancer circuit is an adaptive enhanced processing using two line memories. The adaptive LPF of the vertical enhancer circuit minimizes noise and dot–crawl. This block does not emphasize horizontal and vertical sync signals. Table 2 shows the relationship of the VH pin and the vertical enhancer function. The coring characteristics of the vertical enhancer circuit can be set up using the digital port in normal mode.

Table 2. VH Function

VH Pin	Vertical Enhancer
L	On
H	Off

D/A Converter

The luminance and chrominance signals separated in the Advanced Comb Filter–II portion are converted to analog signals by two 8–bit D/A converters. The output voltage range is from 0.3 V to 1.5 V, 1.2 V p–p. The sampling clock of the D/A converter is 14.3 MHz/17.7 MHz.

Clock Generation Circuit

The block is a 4xFSC CLK generation circuit. It generates four times the subcarrier signal which locks the inputting subcarrier on the FSC pin at the normal (FSC) mode. At the other mode, the external 4xFSC clock should be input.
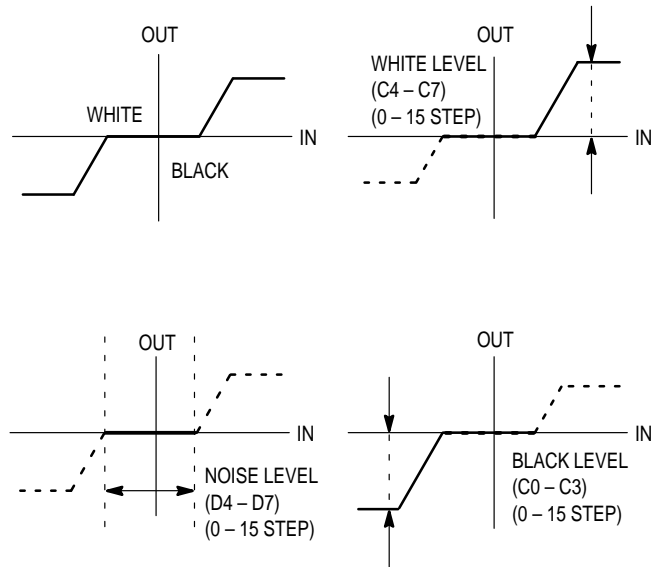
C7	C6	C5	C4	
C3	C2	C1	C0	
D7	D6	D5	D4	Level
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
H	L	H	L	10
H	L	H	H	11
H	H	L	L	12
H	H	L	H	13
H	H	H	L	14
H	H	H	H	15

Figure 2. Coring Characteristics

OPERATING MODES

The Advanced Comb Filter–II can be operated in any of three modes. These modes are fixed by a digital code input into MODE0 and MODE1. The descriptions of the four types of operating modes are:

Normal (FSC) Mode

This mode is for the normal Y/C separation. The video signal input to the A/D converter is separated into its Y and C components and output as analog information from the D/A converter outputs. The clamp circuit operates as sync tip clamp by connecting CL_{out} with V_{in}, and clamps the input video signal to the fixed value $04. The coring characteristics of the vertical enhancer circuit can be set using the digital port. This mode operates the internal 4xFSC CLK which is generated by the built–in 4xFSC PLL.

Normal (4xFSC) Mode

This mode is for the normal Y/C separation. The video signal input to the A/D converter is separated into its Y and C components and output as analog information from the D/A converter outputs. The clamp circuit operates as sync tip clamp by connecting CL_{out} with V_{in}, and clamps the input video signal to the fixed value $04. The coring characteristics of the vertical enhancer circuit can be set up on the digital port. This mode operates the external 4xFSC CLK which is input on the FSC pin.

Digital Input Comb Filtering Mode

In this mode, the MC141627 uses only the filter and D/A portion. This mode can input 8–bit digital outputs from an external circuit. The 8–bit external digital data can be input into D0 – D7, and the input data is filtered by the Advanced Comb Filter–II algorithm, and one output as an analog signal from Y_{out} and C_{out}.

Table 3. Operating Mode

Mode	MODE1	MODE0
Normal (FSC) Mode	L	L
Normal (4xFSC) Mode	L	H
Digital Input Comb Filtering Mode	H	L

APPLICATION DESIGN CONSIDERATIONS

V_{CC}, GND

To minimize noise effects for A/D, D/A, and all digital V_{CC} and GND, wire up to the power supply separation. Leave the GND line as wide and short as possible. Furthermore, the wiring impedance should be as small as possible on the layout. To bypass noise, apply a high–capacity, high–performance frequency capacitor as close as possible to both analog and digital V_{CC} and ground pins.

A 0.1 μF multi–layer ceramic capacitor and a 47 μF tantalum capacitor are recommended.

V_{in}

In order to prevent flyback noise of the video input, it is necessary to keep the bandwidth to less than one half the clock frequency by using an area filter. Here the amplifier used as an input buffer needs a wide bandwidth and driving capability. Moreover, to minimize external noise effects, an input buffer should be driven by low impedance, and the V_{in} pin should be laid out as close as possible to the pattern layout.

When using the built–in clamp circuit, connect CL_{out} with V_{in} and input signals after ac coupling by using a high–performance capacitor. In this case, keep the V_{in}, CL_{out}, coupling capacitor, and buffer–amplifier wiring as short as possible. Pay particular attention to external noise and parasitic impedance.

A/D Reference Pin

The RTP and RBT pins provide a self–bias function that internally generates $V_{TP} = 2.5$ V and $V_{BT} = 0.5$ V. Presetting the A/D converter analog input dynamic range. A stable performance is achieved by installing high–performance, high–frequency capacitance as close as possible to the RTP and RBT pins and bypassing to GND(AD).

A 0.1 μF multi–layer ceramic capacitor and a 10 μF tantalum capacitor are recommended.

CLC

The CLC pin sets the clamp circuit speed with an external capacitor and resistor.

Generally, the capacitor and resistor are arranged in a row and connected with GND(AD). Select a capacitor that minimizes the dielectric absorbing error. When the capacitor capacity is reduced, the shift speed of the VCR signal to $V_{CC(AD)}$ side is accelerated. When the resistor value is

reduced, the shift speed of the VCR signal to GND(AD) is accelerated. If the resistor value is too small at this point, sagging will appear in the VCR signal. Also, if the capacitor's capacity is too large, the clamp speed will slow down; therefore, it is very important to adjust the values of the resistor and capacitance to match the application.

D/A Reference

REF(DA) is a D/A converter reference decoupling pin for both the Y_{out} and C_{out}. Bypass to GND(DA) by applying a high–performance frequency capacitor as close to the pin as possible.

A 0.1 μF multi–ceramic capacitor is recommended.

Clock Input

The clock frequency inputs 3.58 MHz/4.43 MHz during normal (FSC) mode, and 14.31818 MHz/17.734475 MHz during the other modes. The minimum input level is 1.0 V p–p. It should be phase–locked to the subcarrier of the video signal.

The clock line should be wired with the shortest wire and be separated from other circuits to minimize cross coupling to other signals. The CLK(AD) pin is used only during digital input comb filtering mode; therefore, it should be in GND level except when the digital input comb filtering mode is selected.

I_{bias}

The I_{bias} pin is used to set up the bias current for the A/D and D/A converters. Connect an external resistor between the I_{bias} and GND(DA).

Digital Input Comb Filtering Mode

Connect CLK(AD) with the GND(D) when the A/D converter is not being used. Connect D0 – D7 with GND(D), when the D/A converter and filter are not being used. This is to eliminate any unnecessary operation of blocks which are not being used. At this point, make sure voltage is supplied to the $V_{CC(AD)}$, $V_{CC(DA)}$, and $V_{CC(D)}$. This eliminates latch–up during operating.

Latch–Up

The $V_{CC(AD)}$, $V_{CC(DA)}$, and $V_{CC(D)}$ pins are power supplies, independent from each other. Therefore, latch–up may occur when the power supply is turned on. To eliminate latch–up, turn on each power supply [$V_{CC(AD)}$, $V_{CC(DA)}$, and $V_{CC(D)}$ pins] simultaneously.

APPLICATION CIRCUIT
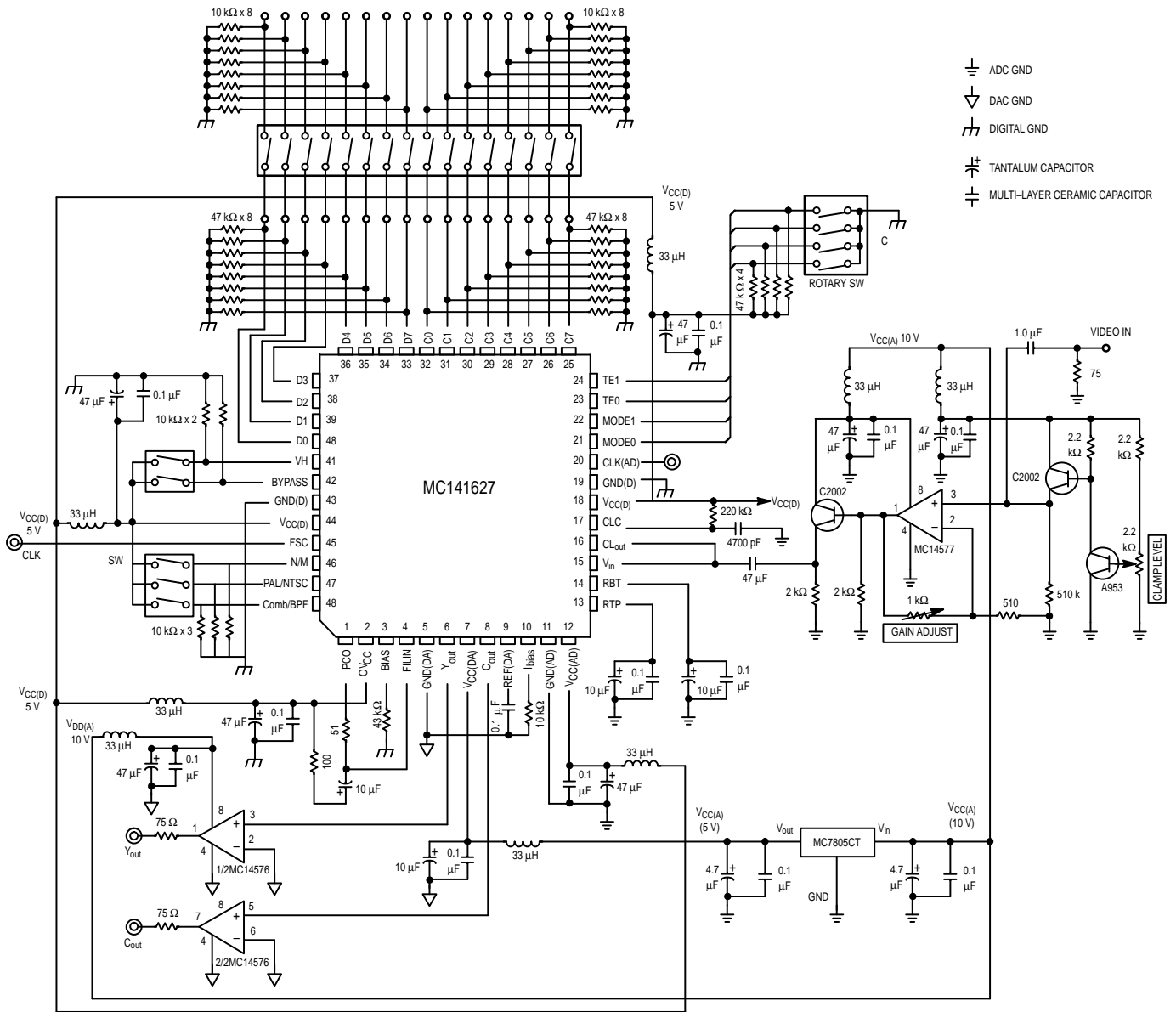
EMI SUPPRESSION

When using ICs in or near television receiver circuits, EMI (electromagnetic interference) and subsequent unwanted display artifacts and distortion are probable unless adequate EMI suppression is implemented. A common misconception is that some offending digital device is the culprit. This is erroneous in that an IC itself has insufficient surface area to produce sufficient radiation. The device, while it is the generator of interfering signals, must be coupled to an antenna before EMI is radiated. The source for the EMI is not the IC which generates the offending signals but rather the circuitry which is attached to the IC.

Potential EMI signals are generated by *all* digital devices. Whether they become a nuisance is dependent upon their frequency and whether they have a sufficient antenna. The frequency and number of these signals is affected by both circuit design within the IC and the manufacturing process. Device speed is also a major contributor of potential EMI. Because the design is determined by the anticipated application, the manufacturing process is fixed and the drive for speed ever increasing, the only effective point to implement EMI suppression is in the PC board design. The PC board usually is the antenna which radiates the EMI. The most efficient method of minimizing EMI radiation is to minimize the efficiency of this antenna.

The most common cause of inadequate EMI suppression lies with the ground system of the suspected digital devices. As pointed out previously, di/dt transitions can be significant in digital circuits. If the di/dt transitions appear in the ground system and the ground system is inductive, the harmonics present in these transitions are a source of potential EMI signals. The unfortunate result of putting digital devices on a reactive ground system is guaranteed EMI problems.

The area which should be addressed first as a potential EMI source is the ground. Without an adequate ground system, EMI cannot be effectively reduced by decoupling. If at all possible, the ground should be a complete unbroken plane. Figure 5 shows two examples of relieving ground around device pins. When relieving vias and plated through holes, large areas of ground loss should be avoided. When the relief pattern is equal to half the distance between pins, over etching and process errors may remove ground between pins. If sufficient ground around enough pins are removed, the ground system can become isolated or nearly isolated "patches" which will appear inductive. If ground, such as the vicinity of an IC, must be removed, replace with a cross hatch of ground lines with the mesh as small as possible.

If a single unbroken plane can be devoted to the ground system, EMI can usually be sufficiently suppressed by using ferrite beads on suspect EMI paths and decoupling with adequate values of capacitors. The value of the decoupling capacitor depends on the frequency and amplitude of the offending signals. Ferrite beads are available in a wide variety of shape, size and material to fit virtually any application.

Choose a ferrite bead for desired impedance at the desired frequency and construct a low pass filter using one or more appropriate capacitors in a "L", "T" or "PI" arrangement. Use only capacitors of low inductive and resistive properties such as ceramic or mica. Install filters in series with each IC pin suspected of contributing offending EMI signals and as close to the pin as possible. Analysis using a spectrum analyzer can help determine which pins are suspect.

Where PC board costs constrain the number of layers available, and if the EMI frequencies are far removed from the frequencies of operation, ferrite beads and decoupling capacitors may still be effective in reducing EMI emissions. Where only two (or in some cases, only one!) layer is used, the ground system is always reactive and poses an EMI problem. If the offending EMI and normal operating frequency differ sufficiently, filtering can still work.

An "island" is constructed in the ground system for the digital device using ferrite beads and decoupling capacitors as shown by the example in Figure 6. The ground must be cut so that the digital ground for the device is isolated from the rest of the ground system. Next choose a ferrite bead of the appropriate value. Install this bead between the isolated ground and the ground system. Install low pass filters in all suspect lines with the capacitor closest to the device pin connected to the isolated ground in all signal lines where EMI is suspect. Also cut the power to the device and insert a ferrite bead as shown in Figure 6. Finally, decouple the device between the power pin(s) and isolated ground pin(s) using a low inductive/resistive capacitor of adequate value.

The methods described above will work acceptably when the EMI frequency and the frequency of operation of the device generating the EMI differ greatly. Where the EMI is disturbing the high VHF or UHF channels and the device generating the EMI is operating within the NTSC/PAL bandwidth, the energy contained in the harmonics generating the EMI is situated well above the operating frequency and suppressing this type of EMI poses no great problem. However, if the EMI is present on low VHF channels and/or the operation of the device is outside the NTSC/PAL bandwidth, such as a 2X pixel clock or 4xFSC oscillator, compromise between video quality and suppression complexity is usually required to obtain an acceptable solution. For those cases where the operating frequency of the device is very near the frequency of the EMI disturbance, careful attention to PCB layout, multiple layer PCB and even shielding may be necessary to obtain an acceptable design.
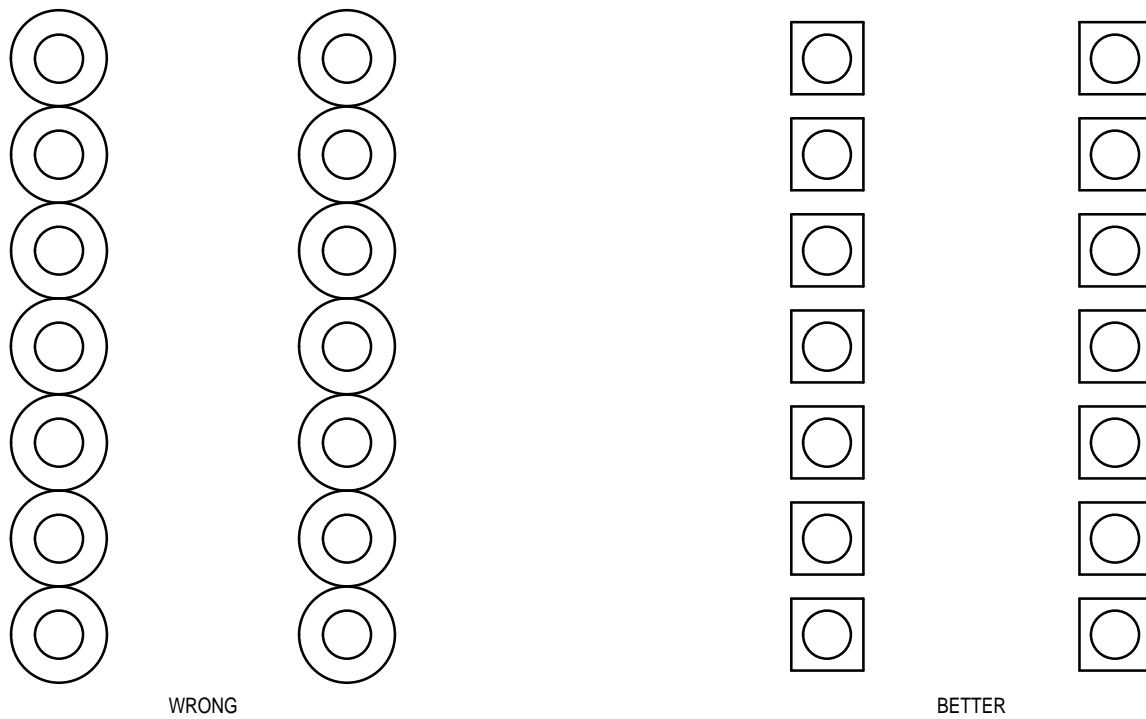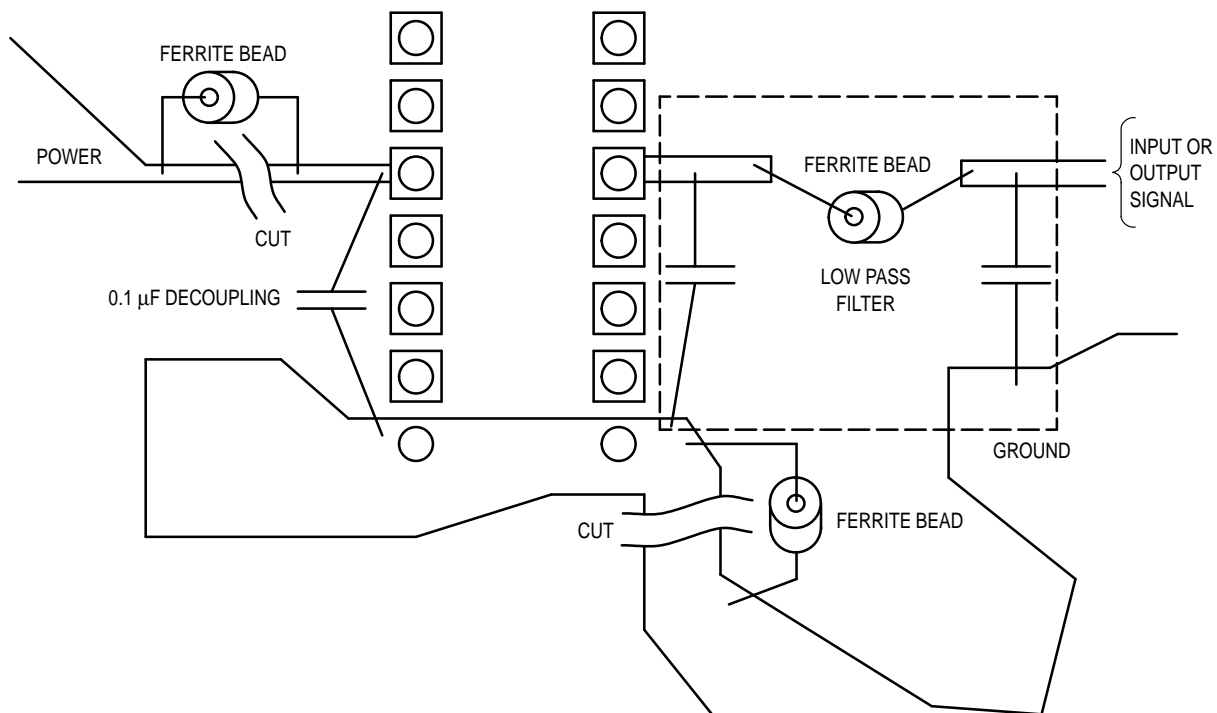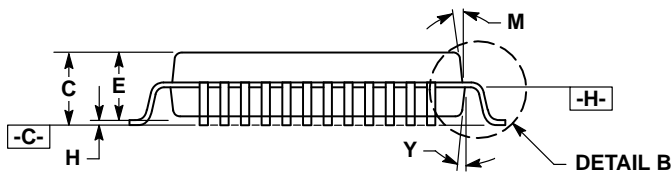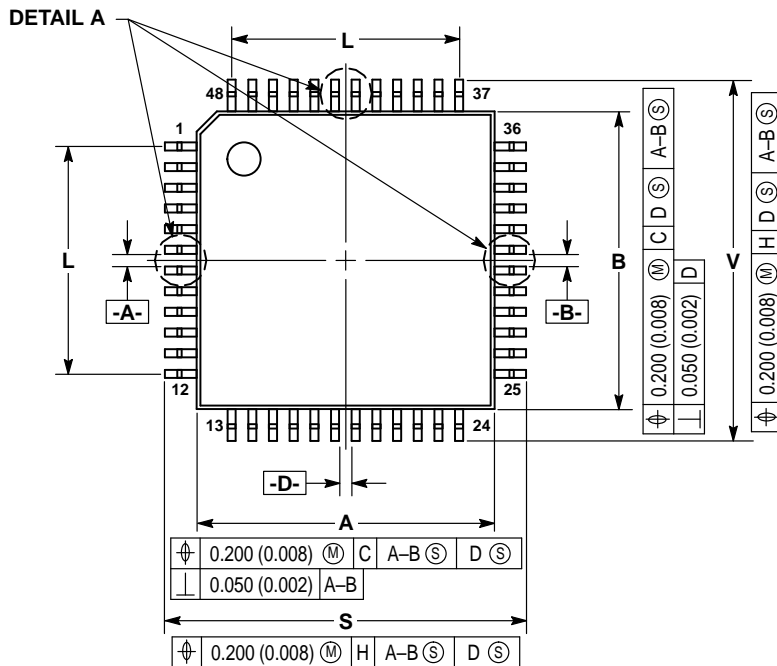
WRONG

BETTER

Figure 3.

FERRITE BEAD

POWER

CUT

0.1 µF DECOUPLING

FERRITE BEAD

LOW PASS
FILTER

INPUT OR
OUTPUT
SIGNAL

GROUND

CUT

FERRITE BEAD

Figure 4.

PACKAGE DIMENSIONS

FT SUFFIX
QFP (QUAD FLAT PACKAGE)
CASE 898–01

DETAIL A

DETAIL B

SECTION B–B
ROTATED 90°

| 0.200 (0.008) Ⓜ | H | A–B Ⓢ | D Ⓢ |

DETAIL A

| 0.200 (0.008) Ⓜ | C | A–B Ⓢ | D Ⓢ |
| 0.050 (0.002) | A–B |

| 0.200 (0.008) Ⓜ | H | A–B Ⓢ | D Ⓢ |

DETAIL B
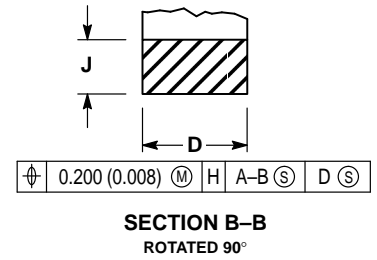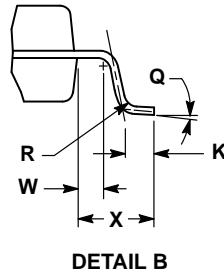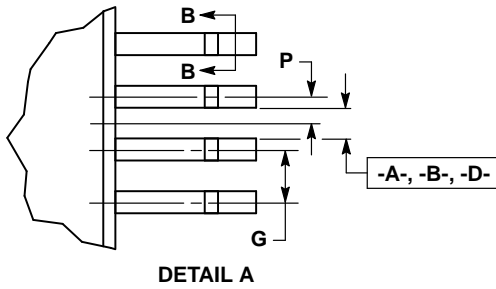
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H- .
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C- .
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H- .
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.48 (0.019).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	11.90	12.10	0.469	0.476
B	11.90	12.10	0.469	0.476
C	2.05	2.55	0.026	0.041
D	0.20	0.40	0.081	0.100
E	2.00	2.30	0.079	0.091
G	0.80 BASIC		0.031 BASIC	
H	0.00	0.30	0.000	0.011
J	0.10	0.20	0.005	0.008
K	0.65	1.05	0.026	0.041
L	8.80 BASIC		0.346 BASIC	
M	13° REF		13° REF	
P	0.40 BASIC		0.016 BASIC	
Q	0°	7°	0°	7°
R	0.13	0.30	0.006	0.011
S	14.90	15.70	0.587	0.618
V	14.90	15.70	0.587	0.618
W	0.65 REF		0.026 REF	
X	1.60 REF		0.063 REF	
Y	5° REF		5° REF	

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MOTOROLA

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MC141627/D