MC144112

Advance Information

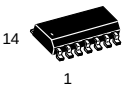
Quad Six-Bit Digital-to-Analog Converter

CMOS

The MC144112 contains four independent DACs which are controlled through a common serial data port. When all DACs are utilized, there are 24 bits in the serial data stream. However, if not all DACs are utilized, the bit stream length may be reduced by up to six bits per unused DAC.

For new designs, the MC144112 is preferred over the MC144110 and MC144111. The newer MC144112 offers a wider operating temperature range, lower operating supply voltage, and lower supply current.

- Operating Supply Voltage Range: 2.7 to 5.5 V *
- Maximum Supply Current (per Package) —
  All DAC Outputs = Zero: 1.25 mA @ 2.7 V
  2.1 mA @ 4.5 V
  All DAC Outputs = Full Scale: 30 µA @ 5.5 V
- Integral Nonlinearity: – 1 1/4 to 1/4 LSB
- Operating Temperature Range: – 40 to 85°C
- Direct R–2R Network Outputs
- Direct Interface to Motorola SPI Serial Data Port
- Digital Data Output Permits Cascading



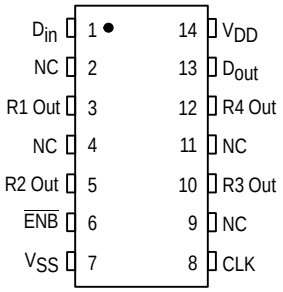
D SUFFIX
SOG PACKAGE
CASE 751A

ORDERING INFORMATION

MC144112D	SOG Package

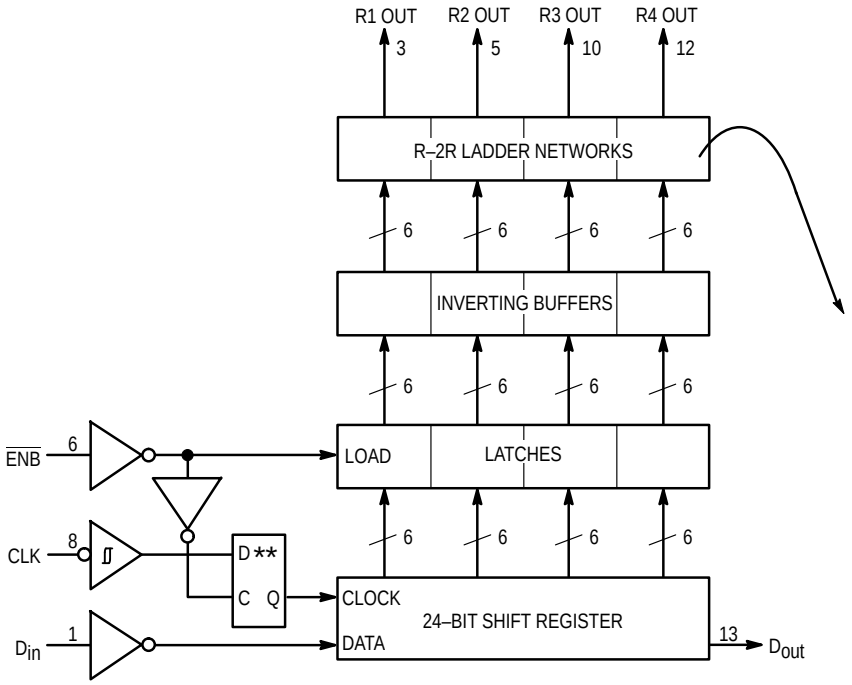
Plastic DIP availability dependent on market demand.

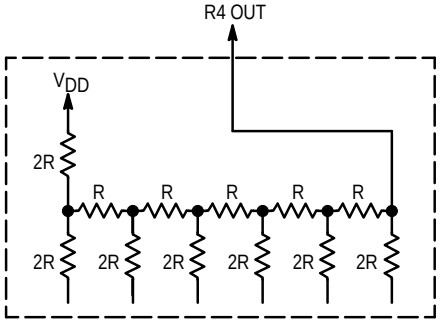
PIN ASSIGNMENT



NC = NO CONNECTION

BLOCK DIAGRAM





R–2R DETAIL

* This product is being evaluated for operation at supply voltages less than 2.7 V. Contact your Motorola representative for further information.
** Transparent Latch

This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 3
2/98 TN98030200

MOTOROLA

MAXIMUM RATINGS* (Voltages referenced to V_{SS})

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	– 0.5 to + 5.5	V
Input Voltage, All Inputs	V_{in}	– 0.5 to V_{DD} + 0.5	V
DC Input Current, per Pin	I	± 10	mA
Power Dissipation (Per Output) T_A = 70°C T_A = 85°C	P_{OH}	 50 20	mW
Power Dissipation (Per Package) T_A = 70°C T_A = 85°C	P_D	 150 50	mW
Storage Temperature Range	T_{stg}	– 65 to + 150	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields; however, it is advised that precautions be taken to avoid application of voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

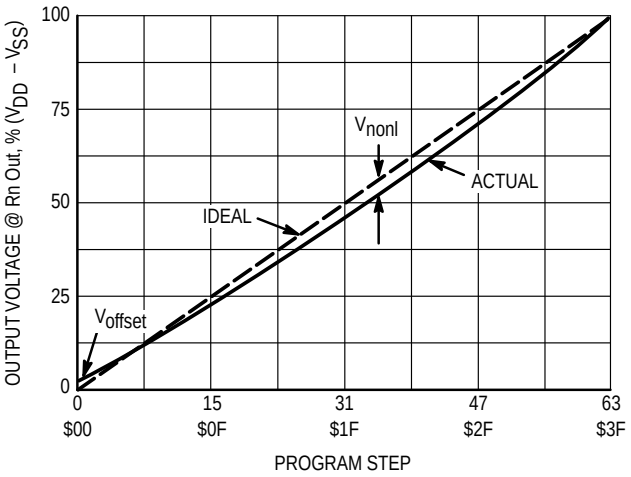
ELECTRICAL CHARACTERISTICS (Voltages referenced to V_{SS}, V_{DD} = 2.7 to 5.5 V, T_A = – 40 to 85°C unless otherwise indicated)

Symbol	Parameter	Test Conditions	V_{DD}	Min	Max	Unit
V_{IH}	High–Level Input Voltage (D_{in}, $\overline{ENB}$, CLK)		2.7 4.5 5.5	2.03 3.15 3.85	— — —	V
V_{IL}	Low–Level Input Voltage (D_{in}, $\overline{ENB}$, CLK)		2.7 4.5 5.5	— — —	0.67 1.35 1.65	V
I_{OH}	High–Level Output Current (D_{out})	$V_{out} = V_{DD} – 0.5$ V	2.7 4.5	0.3 1.1	— —	mA
I_{OL}	Low–Level Output Current (D_{out})	V_{out} = 0.5 V	2.7 4.5	1.0 1.8	— —	mA
I_{SS}	Quiescent Supply Current (per Package)	I_{out} = 0 μA, All DAC Outputs = Zero	2.7 4.5 5.5	— — —	1.25 2.10 2.50	mA
		I_{out} = 0 μA, All DAC Outputs = Full Scale	5.5	—	30	μA
I_{in}	Input Leakage Current (D_{in}, $\overline{ENB}$, CLK)	$V_{in} = V_{DD}$ or 0 V	5.5	—	1	μA
V_{nonl}	Integral Nonlinearity (Rn Out)	See Figure 1	—	– 1 1/4	1/4	LSB
V_{step}	Differential Nonlinearity (Rn Out)	See Figure 2	—	– 3/4	3/4	LSB
V_{offset}	Offset from V_{SS}	D_{in} = $00, See Figure 1	—	1/4	1 3/4	LSB

SWITCHING CHARACTERISTICS

(V_{DD} = 2.7 to 5.5 V, Voltages referenced to V_{SS}, T_A = – 40 to 85°C, C_L = 50 pF, Input $t_r = t_f$ = 20 ns unless otherwise indicated)

Symbol	Parameter	Min	Max	Unit
t_{wH}	Positive Pulse Width, CLK (Figures 3 and 4)	166	—	ns
t_{wL}	Negative Pulse Width, CLK (Figures 3 and 4)	166	—	ns
t_{su}	Setup Time, $\overline{ENB}$ to CLK (Figures 3 and 4)	135	—	ns
t_{su}	Setup Time, D_{in} to CLK (Figures 3 and 4)	55	—	ns
t_h	Hold Time, CLK to $\overline{ENB}$ (Figures 3 and 4)	135	—	ns
t_h	Hold Time, CLK to D_{in} (Figures 3 and 4)	55	—	ns
t_r, t_f	Input Rise and Fall Times, CLK	—	100	μs
C_{in}	Input Capacitance	—	10	pF
f_{clk}	Serial Data Clock Frequency (Refer to t_{wH} and t_{wL} Above) (Figures 3 and 4)	dc	3	MHz



LINEARITY ERROR (integral nonlinearity). A measure of how straight a device's transfer function is, it indicates the worst–case deviation of linearity of the actual transfer function from the best–fit straight line. It is normally specified in parts of an LSB.

Figure 1. D/A Transfer Function

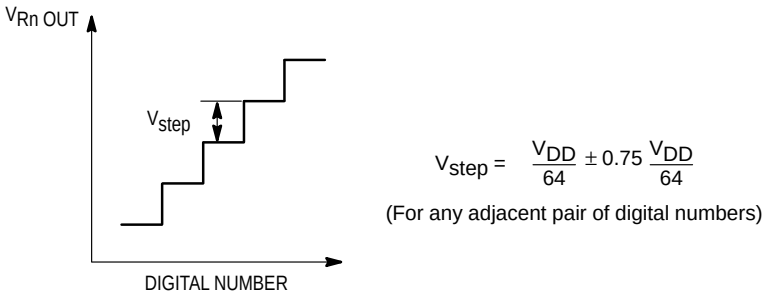


Figure 2. Definition of Step Size Variance (Differential Nonlinearity)

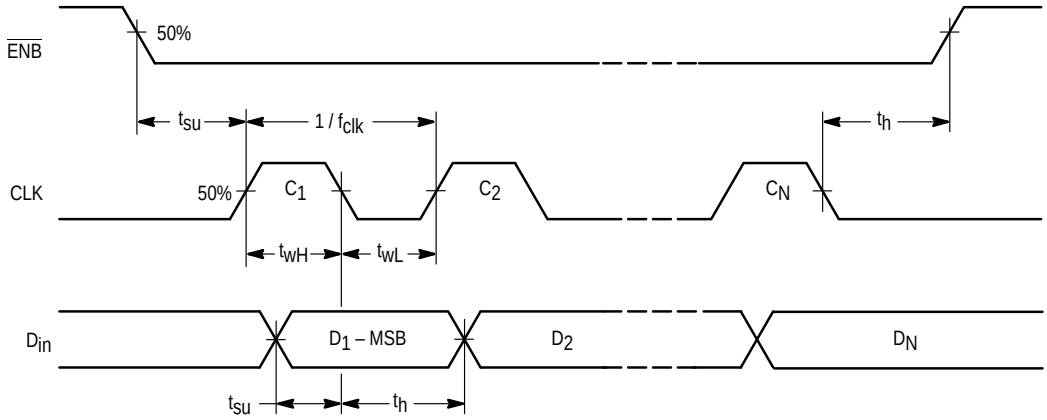


Figure 3. Serial Input, Positive Clock

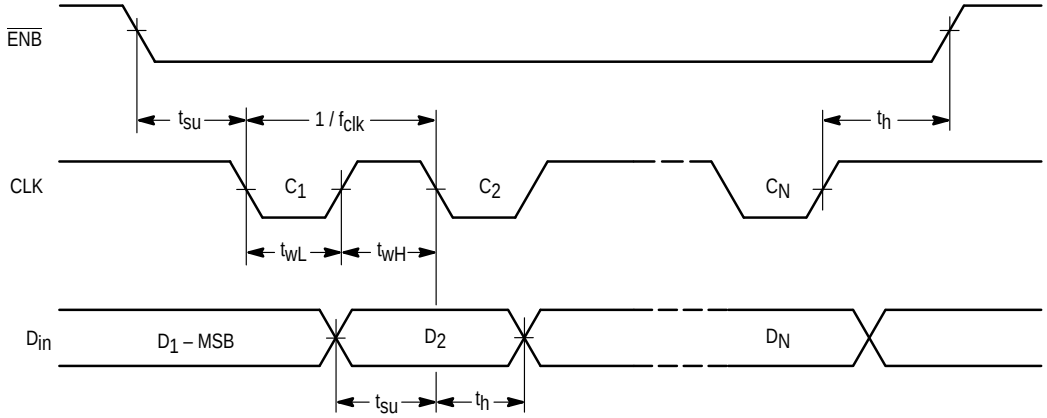


Figure 4. Serial Input, Negative Clock

PIN DESCRIPTIONS

INPUTS

D_{in}
Data Input

Four 6–bit words are entered serially, MSB first, into the digital data input, D_{in}.

The last 6–bit word shifted in determines the output level of pin R1 Out. The next–to–last 6–bit word affects pin R2 Out, etc.

$\overline{ENB}$
Negative Logic Enable

The $\overline{ENB}$ pin must be low (active) during the serial load. On the low–to–high transition of $\overline{ENB}$, data contained in the shift register is loaded into the latch.

CLK
Shift Register Clock

Data is shifted into the register on the high–to–low transition of CLK. CLK is fed into the D–input of a transparent latch, which is used for inhibiting the clocking of the shift register when $\overline{ENB}$ is high.

The MC144112 usually uses 24 CLK cycles. See Table 1 for additional information.

OUTPUTS

D_{out}
Data Output

The digital data output is primarily used for cascading the DACs and may be fed into D_{in} of the next stage.

If not used, the output should be floated.

R1 Out through R4 Out
Resistor Network Outputs

These are the R–2R resistor network outputs. These outputs may be fed to high–impedance loads. The R value of the resistor network ranges from 7 to 15 kΩ.

If not used, an output should be floated.

SUPPLY PINS

V_{SS}
Negative Supply Voltage

This pin is usually ground.

V_{DD}
Positive Supply Voltage

The voltage applied to this pin determines the analog output swing. The DAC output voltage range is from approximately V_{SS} to V_{DD}.

APPLICATIONS INFORMATION

For those applications where supply current is critical, any unused DAC channels should be programmed for full–scale output. The unused outputs are floated (no connects).

For example, with a 4.5 V supply, the worst case current when all DACs are programmed for zero output is 2.1 mA. This is 2.1 mA for the package; each DAC is drawing 1/4 of this, or 525 μA. If only two channels are needed, minimum supply current is achieved by programming the two unused channels to full–scale output (all ones). In this case, the worst case supply current is approximately two times 525 μA, or 1.05 mA.

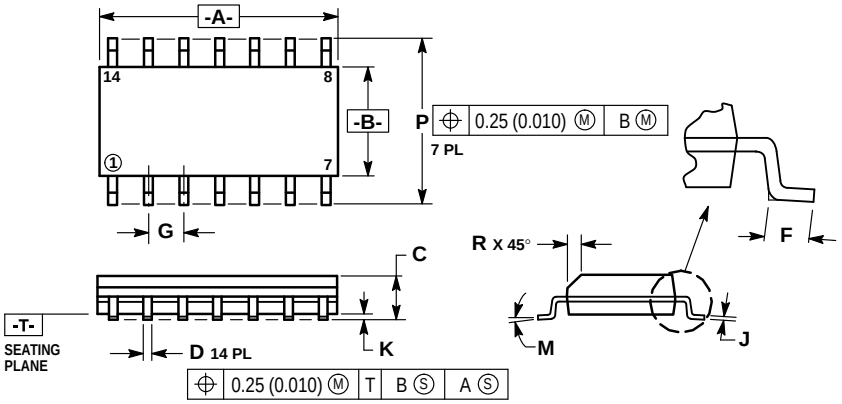
Table 1. Number of Channels vs Clocks Required

Number of Channels Required	Minimum Number of Clock Cycles*	Outputs Used
1	6	R1 Out
2	12	R1 Out, R2 Out
3	18	R1 Out, R2 Out, R3 Out
4	24	R1 Out, R2 Out, R3 Out, R4 Out

* Additional clock cycles can be used, with the leading extra bits being don't cares. For example, eight clocks can be used if one channel is needed. The first two bits are don't cares; the last six bits determine the DAC output.

PACKAGE DIMENSIONS

D SUFFIX
SOG (SMALL OUTLINE GULL–WING) PACKAGE
CASE 751A–03



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.299	0.244
R	0.25	0.50	0.010	0.019

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JAPAN: Nippon Motorola Ltd.: SPD, Strategic Planning Office, 141,
4–32–1 Nishi–Gotanda, Shagawa–ku, Tokyo, Japan. 03–5487–8488

ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298

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