Low-Voltage CMOS 16-Bit Transparent Latch
With 5V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

MC74LCX16373

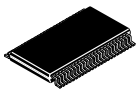
LCX

LOW–VOLTAGE CMOS 16–BIT TRANSPARENT LATCH

The MC74LCX16373 is a high performance, non–inverting 16–bit transparent latch operating from a 2.7 to 3.6V supply. The device is byte controlled. Each byte has separate Output Enable and Latch Enable inputs. These control pins can be tied together for full 16–bit operation. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX16373 inputs to be safely driven from 5V devices.

The MC74LCX16373 contains 16 D–type latches with 3–state 5V–tolerant outputs. When the Latch Enable (LEn) inputs are HIGH, data on the Dn inputs enters the latches. In this condition, the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH–to–LOW transition of LE. The 3–state outputs are controlled by the Output Enable (OEn) inputs. When OE is LOW, the outputs are enabled. When OE is HIGH, the standard outputs are in the high impedance state, but this does not interfere with new data entering into the latches.

- Designed for 2.7 to 3.6V V_{CC} Operation
- 5.4ns Maximum t_{pd}
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0V
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (20μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V



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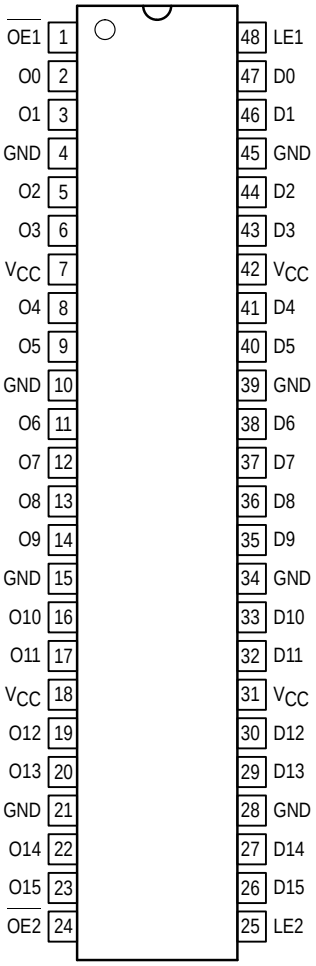
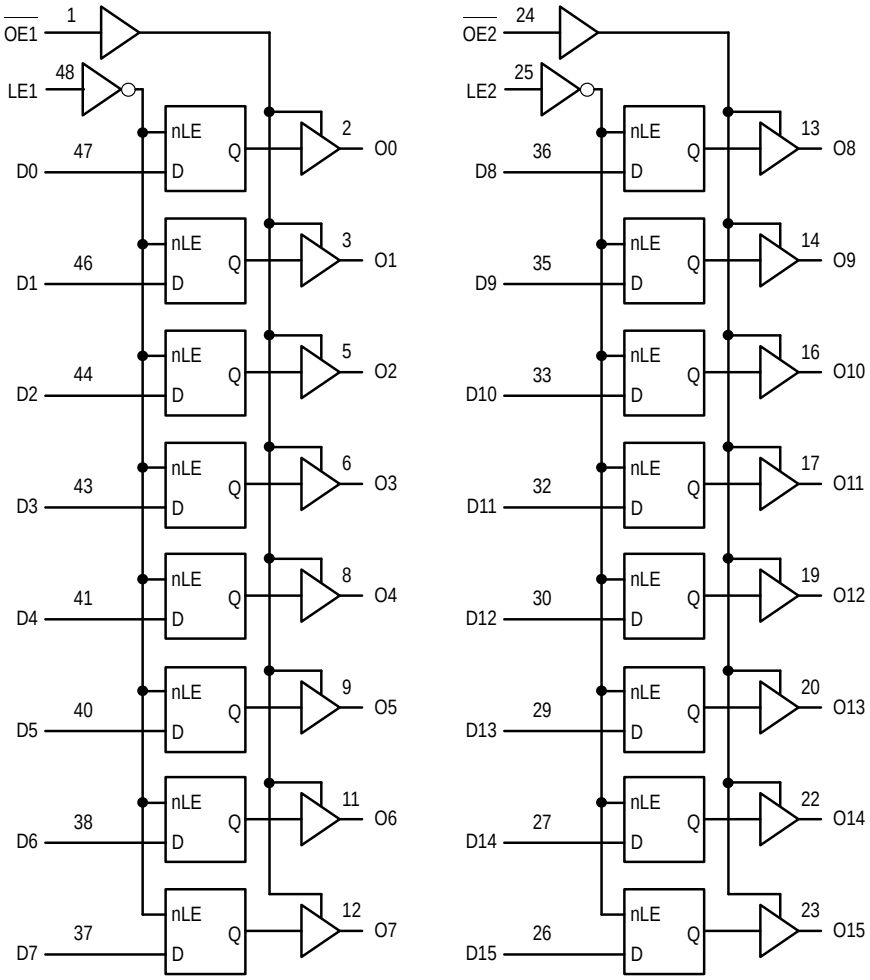
CASE 1201–01

PIN NAMES

Pins	Function
$\overline{OEn}$	Output Enable Inputs
LEn	Latch Enable Inputs
D0–D15	Inputs
O0–O15	Outputs



LOGIC DIAGRAM



Inputs			Outputs	Inputs			Outputs
LE1	**$\overline{OE1}$**	**D0:7**	**O0:7**	**LE2**	**$\overline{OE2}$**	**D8:15**	**O8:15**
X	H	X	Z	X	H	X	Z
H	L	L	L	H	L	L	L
H	L	H	H	H	L	H	H
L	L	X	O0	L	L	X	O0

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; X = High or Low Voltage Level and Transitions Are Acceptable, for I_{CC} reasons, DO NOT FLOAT Inputs

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0		V
V_I	DC Input Voltage	$–0.5 \le V_I \le +7.0$		V
V_O	DC Output Voltage	$–0.5 \le V_O \le +7.0$	Output in 3–State	V
		$–0.5 \le V_O \le V_{CC} + 0.5$	Note 1.	V
I_{IK}	DC Input Diode Current	–50	$V_I < GND$	mA
I_{OK}	DC Output Diode Current	–50	$V_O < GND$	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	–65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

1. Output in HIGH or LOW State. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	Operating Data Retention Only	2.0 1.5	3.3 3.3	3.6 3.6	V
V_I	Input Voltage		0		5.5	V
V_O	Output Voltage	(HIGH or LOW State) (3–State)	0 0		V_{CC} 5.5	V
I_{OH}	HIGH Level Output Current, V_{CC} = 3.0V – 3.6V				–24	mA
I_{OL}	LOW Level Output Current, V_{CC} = 3.0V – 3.6V				24	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 2.7V – 3.0V				–12	mA
I_{OL}	LOW Level Output Current, V_{CC} = 2.7V – 3.0V				12	mA
T_A	Operating Free–Air Temperature		–40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, V_{CC} = 3.0V		0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = –40°C to +85°C		Unit
			Min	Max	
V_{IH}	HIGH Level Input Voltage (Note 2.)	$2.7V \le V_{CC} \le 3.6V$	2.0		V
V_{IL}	LOW Level Input Voltage (Note 2.)	$2.7V \le V_{CC} \le 3.6V$		0.8	V
V_{OH}	HIGH Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; I_{OH} = –100µA	V_{CC} – 0.2		V
		V_{CC} = 2.7V; I_{OH} = –12mA	2.2		
		V_{CC} = 3.0V; I_{OH} = –18mA	2.4		
		V_{CC} = 3.0V; I_{OH} = –24mA	2.2		
V_{OL}	LOW Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; I_{OL} = 100µA		0.2	V
		V_{CC} = 2.7V; I_{OL}= 12mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 16mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 24mA		0.55	

2. These values of V_I are used to test DC electrical characteristics only.

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Characteristic	Condition	T_A = –40°C to +85°C		Unit
			Min	Max	
I_I	Input Leakage Current	$2.7V \le V_{CC} \le 3.6V$; $0V \le V_I \le 5.5V$		±5.0	µA
I_{OZ}	3–State Output Current	$2.7 \le V_{CC} \le 3.6V$; $0V \le V_O \le 5.5V$; $V_I = V_{IH}$ or V_{IL}		±5.0	µA
I_{OFF}	Power–Off Leakage Current	V_{CC} = 0V; V_I or V_O = 5.5V		10	µA
I_{CC}	Quiescent Supply Current	$2.7 \le V_{CC} \le 3.6V$; V_I = GND or V_{CC}		20	µA
		$2.7 \le V_{CC} \le 3.6V$; $3.6 \le V_I$ or $V_O \le 5.5V$		±20	µA
ΔI_{CC}	Increase in I_{CC} per Input	$2.7 \le V_{CC} \le 3.6V$; $V_{IH} = V_{CC} – 0.6V$		500	µA

AC CHARACTERISTICS ($t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω)

Symbol	Parameter	Waveform	Limits				Unit
			T_A = –40°C to +85°C				
			V_{CC} = 3.0V to 3.6V		V_{CC} = 2.7V		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	1	1.5 1.5	5.4 5.4	1.5 1.5	5.9 5.9	ns
t_{PLH} t_{PHL}	Propagation Delay LE to O_n	3	1.5 1.5	5.5 5.5	1.5 1.5	6.4 6.4	ns
t_{PZH} t_{PZL}	Output Enable Time to HIGH and LOW Level	2	1.5 1.5	6.1 6.1	1.5 1.5	6.5 6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time from HIGH and LOW Level	2	1.5 1.5	6.0 6.0	1.5 1.5	6.3 6.3	ns
t_s	Setup TIme, HIGH or LOW D_n to LE	3	2.5		2.5		ns
t_h	Hold TIme, HIGH or LOW D_n to LE	3	1.5		1.5		ns
t_w	LE Pulse Width, HIGH	3	3.0		3.0		ns
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 3.)			1.0 1.0			ns

3. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

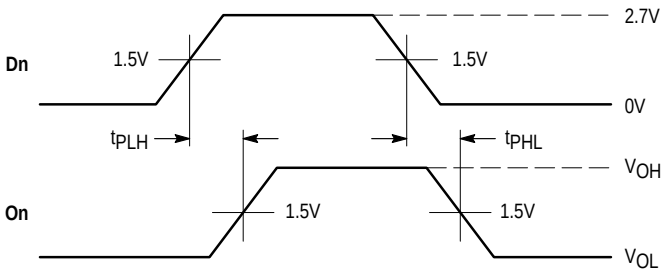
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = +25°C			Unit
			Min	Typ	Max	
V_{OLP}	Dynamic LOW Peak Voltage (Note 4.)	V_{CC} = 3.3V, C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V		0.8		V
V_{OLV}	Dynamic LOW Valley Voltage (Note 4.)	V_{CC} = 3.3V, C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V		0.8		V

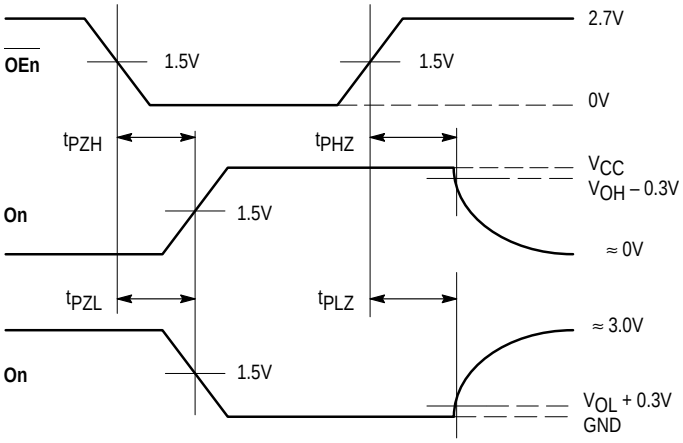
4. Number of outputs defined as “n”. Measured with “n–1” outputs switching from HIGH–to–LOW or LOW–to–HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

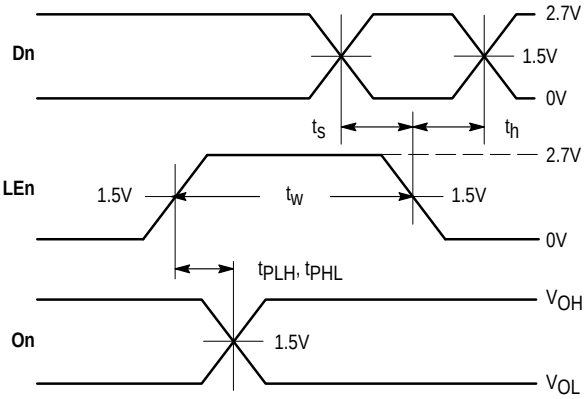
Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	10MHz, V_{CC} = 3.3V, V_I = 0V or V_{CC}	20	pF



WAVEFORM 1 – PROPAGATION DELAYS
$t_R = t_F$ = 2.5ns, 10% to 90%; f = 1MHz; t_W = 500ns

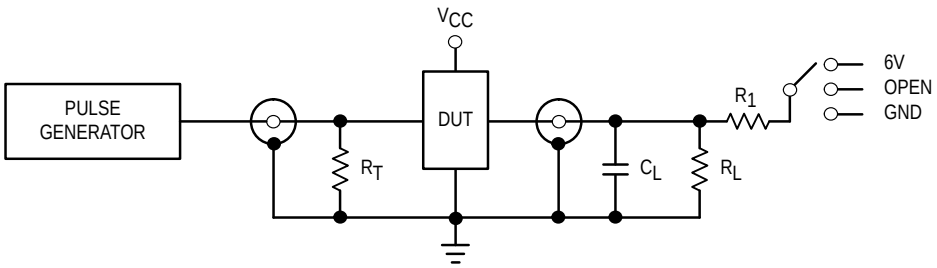


WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F$ = 2.5ns, 10% to 90%; f = 1MHz; t_W = 500ns



WAVEFORM 3 – LE to On PROPAGATION DELAYS, LE MINIMUM PULSE WIDTH, Dn to LE SETUP AND HOLD TIMES
$t_R = t_F$ = 2.5ns, 10% to 90%; f = 1MHz; t_W = 500ns except when noted

Figure 1. AC Waveforms



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V
Open Collector/Drain t_{PLH} and t_{PHL}	6V
t_{PZH}, t_{PHZ}	GND

C_L = 50pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1$ = 500Ω or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 2. Test Circuit

OUTLINE DIMENSIONS

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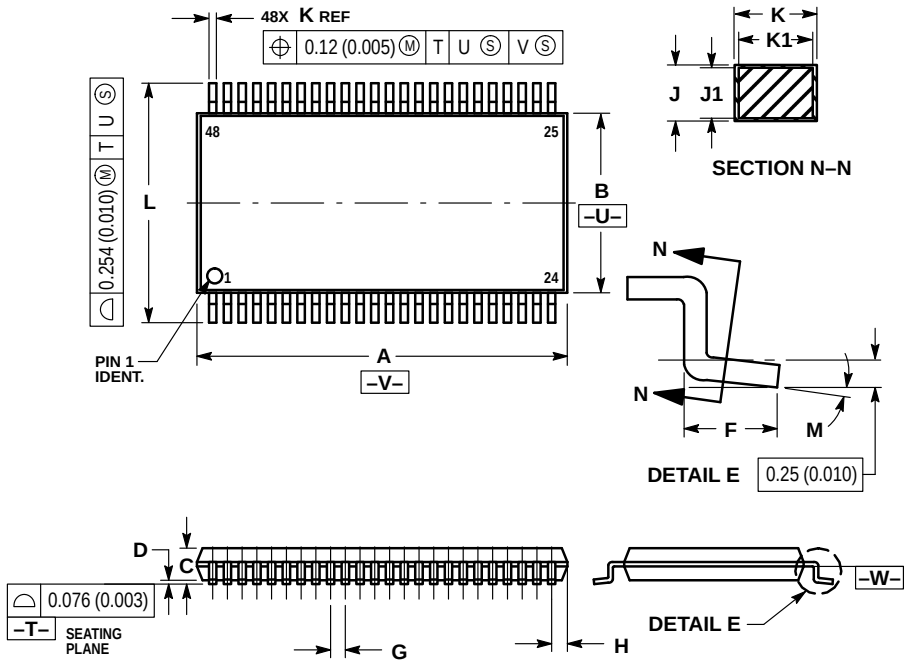
PLASTIC TSSOP PACKAGE
CASE 1201–01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.40	12.60	0.488	0.496
B	6.00	6.20	0.236	0.244
C	—	1.10	—	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.50 BSC		0.0197 BSC	
H	0.37	—	0.015	—
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.17	0.27	0.007	0.011
K1	0.17	0.23	0.007	0.009
L	7.95	8.25	0.313	0.325
M	0 °	8 °	0 °	8 °

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