MC145073

Product Preview

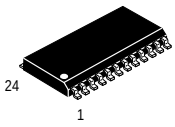
Dual 16-Bit Stereo Audio Sigma-Delta ADC

CMOS

The MC145073 is a dual–channel, 16–bit A/D converter intended for use in digital audio systems such as multimedia, DCC, DAT, and professional audio applications. It uses a sigma–delta architecture consisting of a second–order analog modulator and two stages of digital filtering for each channel. The analog modulator samples the input signal at 128 times the output data rate, performs a single–bit quantization, and shapes the quantization noise towards higher frequencies. Subsequent on–chip digital filters reject most of the shaped quantization noise and lower the data rate.

Sixteen unique user–selectable interfacing modes make the MC145073 compatible with a multitude of application interfacing requirements. A single 5 V supply and a power–down mode reduce power supply requirements, making the part attractive for portable applications.

- Single Supply, Operating Voltage Range: 4.5 to 5.5 V
- 128x OSR Sigma–Delta Modulator
- 82 dB Typical S/(N+D)
- Analog Inputs Can Be Driven as Either Differential or Single–Ended
- Clock Input May Be 128x, 256x, or 384x the Output Data Rate
- Out–of–Range Input Signals Internally Limited
- On–Chip Digital Filters:
  - 5th Order Decimate–by–32 Comb Filter
  - 121 Tap Decimate–by–4 FIR Filter
- User–Selectable Digital Filter Transition Bands
- Versatile Serial Digital Output Interface:
  - Configurable as Master or Slave
  - Data Can Be Either Left– or Right–Justified
  - Interfaces to DSP56000/1 and TMS320™ DSPs
  - I^2S or Japanese Interface Compatibility
  - CS5326 Compatible Interface Mode
  - Multiplexing of Two MC145073s Accommodated
- Power–Down Mode Consumption: 2.0 mW
- Operating Temperature Range: – 40 to 85°C

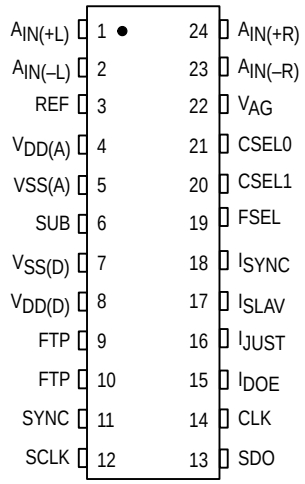


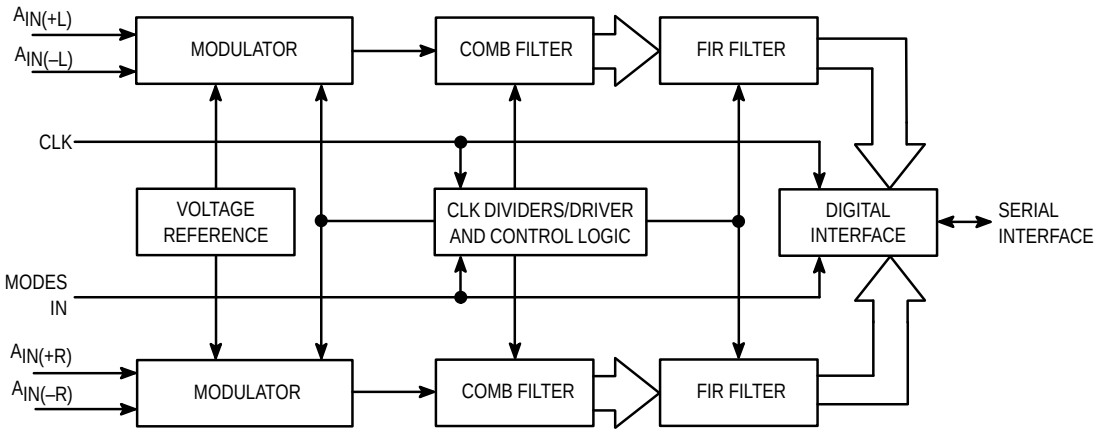
DW SUFFIX
SOG PACKAGE
CASE 751E

ORDERING INFORMATION

MC145073DW SOG Package

PIN ASSIGNMENT





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MOTOROLA

MAXIMUM RATINGS* (Voltages referenced to V_{SS}, unless otherwise stated)

Symbol	Parameter	Value	Unit
$V_{DD(A)}$	Analog Supply Voltage	6.0	V
$V_{DD(D)}$	Digital Supply Voltage	6.0	V
I_{in}	DC Input Current, per Pin	± 20	mA
$V_{in(A)}$	Analog Input Voltage	$V_{SS(A)}$ – 0.3 to $V_{DD(A)}$ + 0.3	V
$V_{in(D)}$	Digital Inputs	– 0.3 to $V_{DD(D)}$ + 0.3	V
T_{stg}	Storage Temperature	– 65 to 150	°C
T_l	Lead Temperature 1 mm From Case for 10 Seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Operation Ranges, Analog Specifications, AC Electrical Characteristics, and DC Electrical Characteristics tables.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit.

OPERATION RANGES

Symbol	Parameter	Min	Max	Unit	Note
$V_{DD(A)}$	Analog Supply Voltage	4.5	5.5	V	
$V_{DD(D)}$	Digital Supply Voltage	4.5	5.5	V	
$V_{in(A)}$	Analog Input Voltage ($A_{IN(+L)}$, $A_{IN(–L)}$, $A_{IN(+R)}$, $A_{IN(–R)}$)	—	1.9	V p–p	1
f_{CLK}	CLK Frequency	3.072	18.432	MHz	2
C_{LOAD}	Capacitive Load on Any Output	0	50	pF	
T_a	Ambient Operating Temperature	– 40	85	°C	

NOTES:
1. Differential inputs greater than 3.8 V p–p will overload the modulators. These voltages are subject to the gain error tolerance specifications in the Analog Specifications table.
2. The internal clock frequency or input sampling frequency is governed by the divide mode and output data rate. The divide mode can be either 1, 2, or 3. The output data rate ranges from 24 kHz to 48 kHz. The minimum clock frequency of 3.072 MHz is for a 24 kHz output rate in the clock divide by 1 mode. The maximum clock frequency of 18.432 MHz is for a 48 kHz output rate in the clock divide by 3 mode.

DC ELECTRICAL SPECIFICATIONS

(Voltages referenced to $V_{SS(D)}$; Full Temperature and Voltage Ranges per Operation Ranges Table, unless otherwise indicated.)

Symbol	Parameter	Min	Max	Unit
V_{IH}	Minimum High–Level Digital Input Voltage	0.7 x $V_{DD(D)}$		V
V_{IL}	Maximum Low–Level Digital Input Voltage		0.3 x $V_{DD(D)}$	V
I_{IN}	Maximum Input Leakage Current		10	μA
V_{OH}	Minimum High–Level Digital Output Voltage (I_{OH} = – 20 μA)	4.4		V
V_{OL}	Maximum Low–Level Digital Output Voltage (I_{OL} = 20 μA)		0.1	V
$I_{DDu(D)}$	Maximum Digital Power Supply Current, Operating		45	mA
$I_{DDd(D)}$	Maximum Digital Power Supply Current, Power–Down		250	μA
$I_{DDu(A)}$	Maximum Analog Power Supply Current, Operating		10	mA
$I_{DDd(A)}$	Maximum Analog Power Supply Current, Power–Down		150	μA
P_O	Power Consumption, Operating		250	mW
P_{pd}	Power Consumption, Power–Down		2.0	mW
Cin	Maximum Input Capacitance		20	pF

ANALOG SPECIFICATIONS

(Full Temperature, CLK = 6.144 MHz in div1, $V_{DD(A)} = V_{DD(D)} = 5.0$ V, 1007.8 Hz Full–Scale Input Sinewave, 1.4 V p–p @ $A_{IN(L)}$ and $A_{IN(R)}$, Common Mode Input Voltage = 2.5 V. Measured bandwidth is 23 Hz to 24 kHz, inputs driven differentially per Figure 1.)

Parameter	Min	Typ	Max	Unit
Resolution Bits	16			Bits
S/(N+D)	76	82		dB
Dynamic Range		85		dB
Total Harmonic Distortion (Vin = ± F.S.)		.003		%
Gain Error		± 5		%
Gain Drift		50		ppm/°C
Channel to Channel Isolation		90		dB
PSRR ($V_{DD(A)}$)		60		dB
PSRR ($V_{DD(D)}$)		100		dB
Input Impedance		40		kΩ
Warm–Up Time (for Reference and Bias Circuits)		1		ms

DIGITAL FILTER CHARACTERIZATION

(Over full operating ranges per Operating Ranges table. Stated values are for input/output relationships from input of comb filter to output of FIR filter.)

Parameter	Output Data Rate			Unit	Notes
	32 kHz	44.1 kHz	48 kHz		
FSEL = low					
FIR Filter Passband	0 to 13.3	0 to 18.3	0 to 20	kHz	
Maximum Passband Ripple	± 0.1	± 0.1	± 0.1	dB	
FIR Filter Transition Band	13.3 to 17	18.3 to 23.5	20 to 25.8	kHz	
FIR Filter Rejection (Min)	– 84	– 84	– 84	dB	
Maximum Alias Level (Figure 3)	– 86	– 86	– 86	dB	1, 2
Group Delay	33	33	33	Out CLKS	3
Setting Time	49	49	49	Out CLKS	3
FSEL = high					
FIR Filter Passband	0 to 14.5	0 to 20	0 to 21.7	kHz	
Maximum Passband Ripple	± 0.1	± 0.1	± 0.1	dB	
FIR Filter Transition Band	14.5 to 18.2	20 to 25.0	21.7 to 27.3	kHz	
FIR Filter Rejection (Min)	– 84	– 84	– 84	dB	
Maximum Alias Level (Figure 3)	– 86	– 86	– 86	dB	1, 2
Group Delay	33	33	33	Out CLKS	3
Setting Time	49	49	49	Out CLKS	3

NOTES:

1. There is no rejection of input signals that are multiples of the sampling frequency (nxCLKI ± Filter Bandwidth, where n = 0, 1, 2, ...).
2. The maximum alias level spec does not apply to input signals in the range of 24 to 25.8 kHz in the 48 kHz output mode, 22.05 to 23.675 kHz in the 44.1 kHz output mode, or 16 to 17.2 kHz in the 32 kHz output mode.
3. One Out CLK (output clock) is equal in length to 128 internal CLKs or one SYNC clock period.

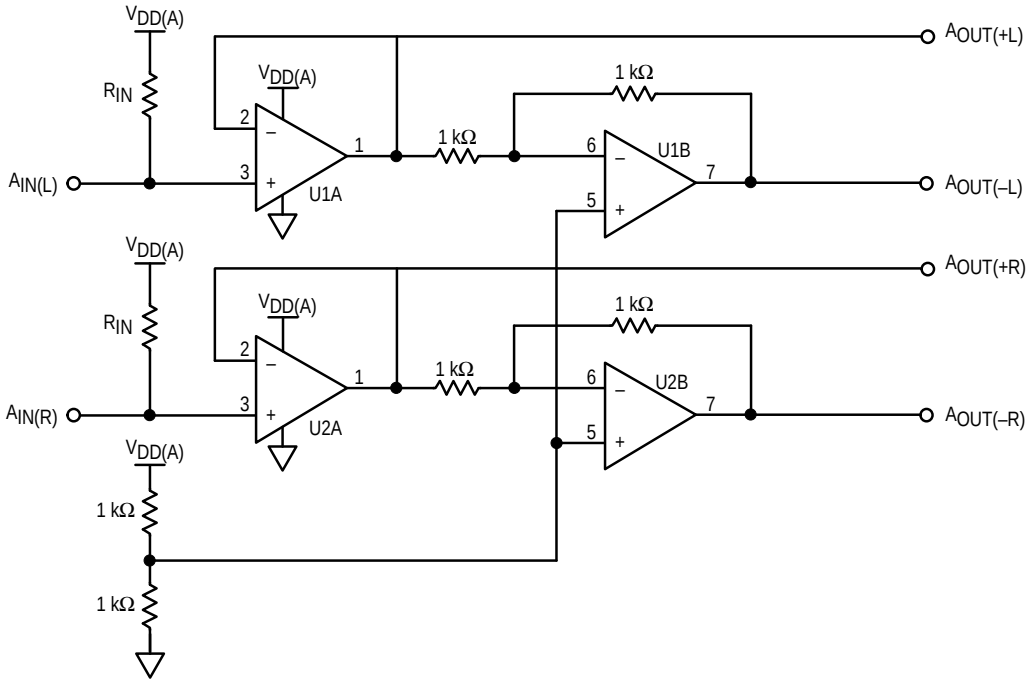


Figure 1. Input Buffer–Driver

NOTES:
1. Analog signals $A_{IN(L)}$ and $A_{IN(R)}$ are floating drivers. R_{OUT} of source is to be equal to R_{IN} of resistors.
2. U1, U2 — MC33077.

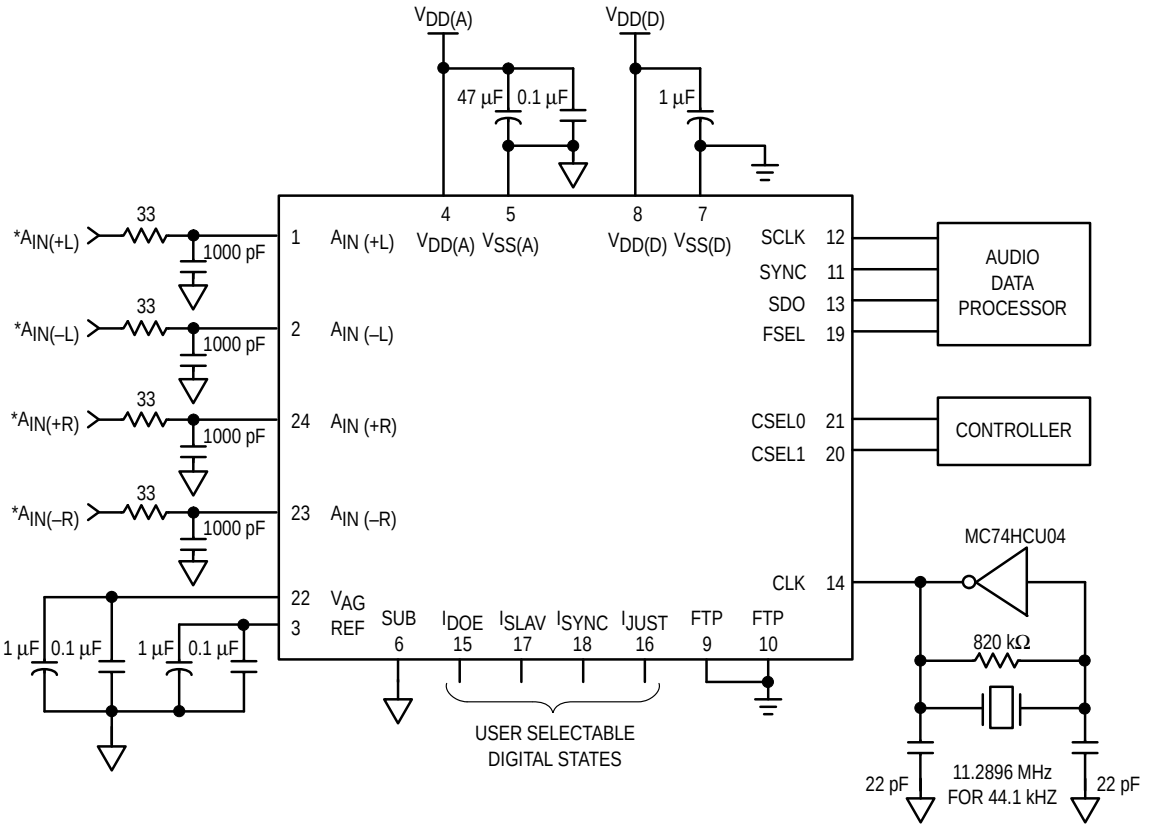


Figure 2. MC145073 A/D Application Circuit

* For best performance $A_{IN(+L)}$, $A_{IN(–L)}$ and $A_{IN(+R)}$, $A_{IN(–R)}$ should be differentially driven. $A_{IN(+L)}$ or $A_{IN(+R)}$ (and $A_{IN(–L)}$ or $A_{IN(–R)}$) can be grounded for single ended configuration. Circuit in Figure 1 depicts input buffer circuit.

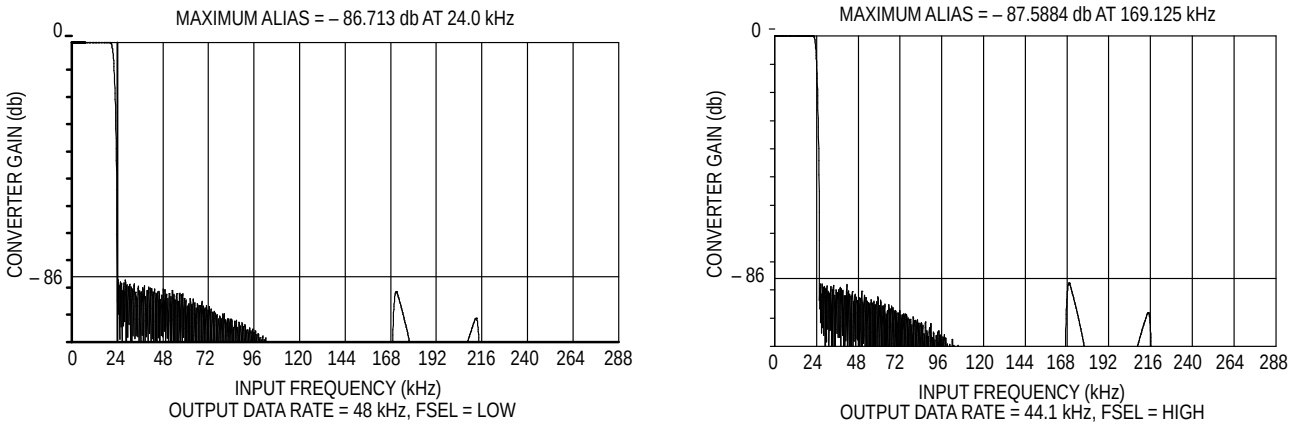


Figure 3. Digital Filter Response (Wideband)
CLKI = 6.144 MHz

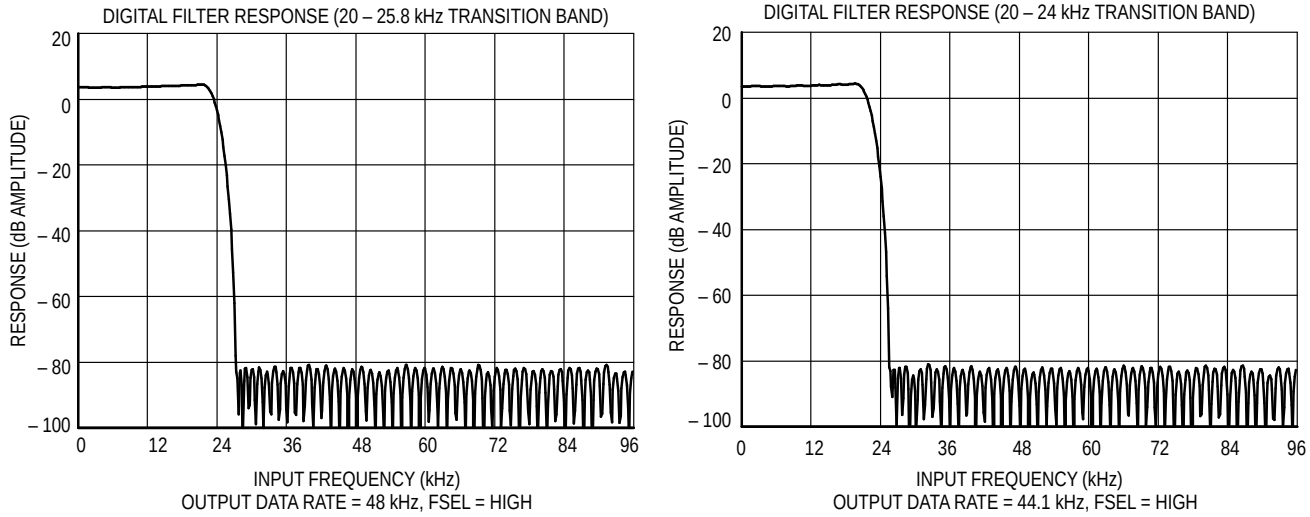


Figure 4. Digital Filter Response (Narrowband)
CLKI = 6.144 MHz

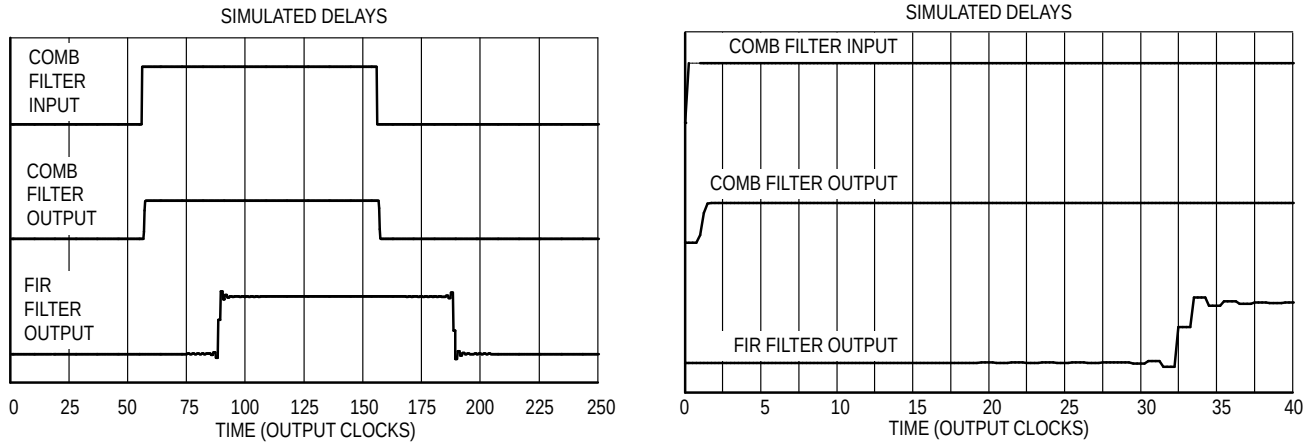


Figure 5. Group Delay and Setting Time

AC ELECTRICAL SPECIFICATIONS

(Full temperature and voltage ranges per Operation Ranges table. All timing parameters measured with respect to 30% and 70% of $V_{DD(D)}$ unless otherwise noted.)

Figure	Symbol	Parameter	Divide Ratio	Min	Max	Unit
6	$1/t_{clk}$	Master Clock (CLK) Frequency (Note 1)		3.072	18.432	MHz
6	$1/t_{clki}$	Internal Clock Frequency, CLKI (Note 1) $t_{clki} = 1/(f_{clk}/\text{Divide Ratio})$		3.072	6.144	MHz
6	t_{wch}	Master Clock High, CLK	1 2, 3	38 20		ns
6	t_{wcl}	Master Clock Low, CLK	1 2, 3	38 20		ns
7	t_{sync}	Sync Period (Master and Slave Modes)		$128 * t_{clki}$	$128 * t_{clki}$	ns
7	t_{wsh}	Sync High (Slave Mode)		20	$126 * t_{clki}$	ns
	C_{in}	Input Capacitance (Except for Left/Right Channel Inputs)			20	pF
		Master Mode: $I_{SLAV} = 0$				
8	t_{sclk}	SCLK Period		$2 * t_{clki}$	$2 * t_{clki}$	ns
8	t_{wl}/t_{wh}	SCLK Duty Cycle		0.667	1.50	
8	t_{CSY}	Propagation Delay (Note 2) CLK Falling Edge to SYNC CLK Rising Edge to SYNC CLK Falling Edge to SYNC	 1 2 3		 40 $t_{clk} + 40$ $2 * t_{clk} + 40$	 ns ns ns
8	t_{CSC}	Propagation Delay (Note 2) CLK Falling Edge to SCLK CLK Rising Edge to SCLK CLK Falling Edge to SCLK	 1 2 3		 40 $t_{clk} + 40$ $2 * t_{clk} + 40$	 ns ns ns
8	t_{CDV}	Propagation Delay (Note 2) CLK Falling Edge to Serial Data Valid, SDO CLK Rising Edge to Serial Data Valid, SDO CLK Falling Edge to Serial Data Valid, SDO	 1 2 3		 40 $t_{clk} + 40$ $2 * t_{clk} + 40$	 ns ns ns
		Slave Mode: $I_{SLAV} = 1$				
9	t_{su}	Setup Time (Note 3) SCLK to Rising Edge of CLK		15		ns
9	t_h	Hold Time (Note 3) SCLK to Rising Edge of CLK			0	ns
9	t_{sclkh}	SCLK High		20		ns
9	t_{sclkl}	SCLK Low		20		ns
9	t_{su}	Setup Time (Note 3) SYNC to Rising Edge of CLK		15		ns
9	t_h	Hold Time (Note 3) SYNC to Rising Edge of CLK			0	ns
	t_{CDV}	Propagation Delay Clk Rising Edge to Serial Data Valid, SDO	1 2 3	t_{wch} t_{clk} $t_{clk} + t_{wch}$	$t_{wch} + 40$ $2 * t_{clk} + 40$ $3 * t_{clk} + t_{wch} + 40$	

NOTES:

1. The internal clock frequency, or input sampling frequency (CLKI) is governed by the divide mode and output data rate.
   The divide mode can be either 1, 2, or 3. The output data rate ranges from 24 kHz to 48 kHz.
   The minimum clock frequency of 3.072 MHz corresponds to an output data rate of 24 kHz with the device in the clock divide by one mode.
   The maximum clock frequency of 18.432 MHz corresponds to an output data rate of 48 kHz with the device in the clock divide by three mode.
2. Propagation delay is measured with a capacitive load of 50 pF.
3. In the slave mode, SYNC or SCLK transitions can occur anywhere except 0 to – 5 ns relative to the CLK rising edge.

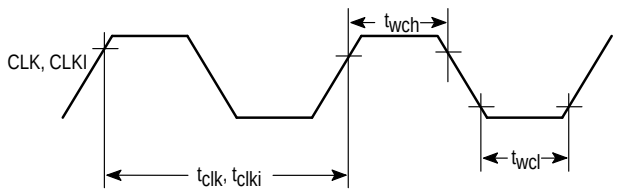


Figure 6.

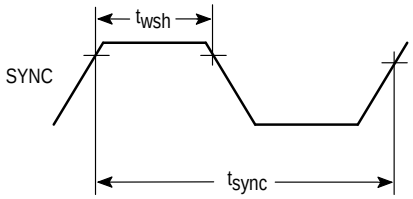


Figure 7.

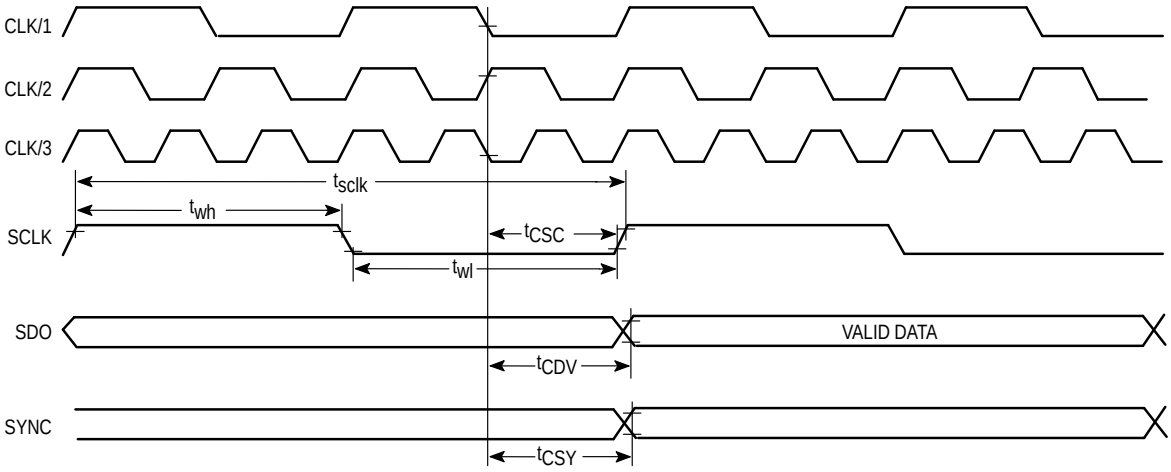


Figure 8. Serial Interface Timing (Master Mode: I_{SLAV} = 0)

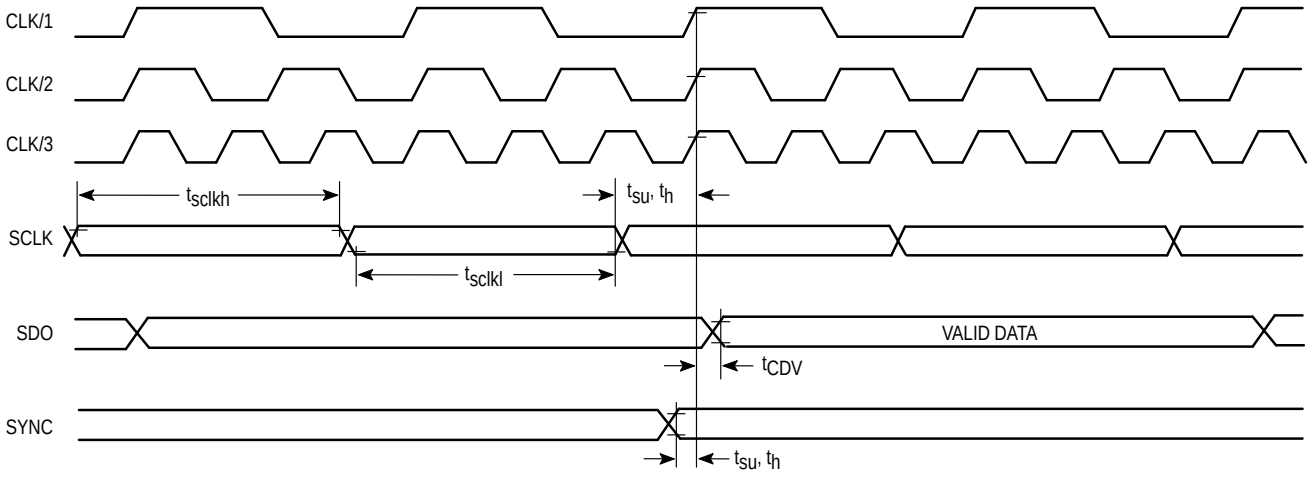


Figure 9. Serial Interface Timing (Slave Mode: I_{SLAV} = 1)

NOTE: CLK signals shown above represent the external clock at three different frequencies.

PIN DESCRIPTIONS

ANALOG PINS

$A_{IN(+L)}$, $A_{IN(–L)}$
Left Channel Analog Inputs (Pins 1, 2)

These two pins comprise the left channel analog differential inputs. The voltage range of signals applied to these pins is from $V_{SS(A)}$ to $V_{DD(A)}$. A positive full–scale input to the A/D is defined as a difference of 3.8 V p–p between $A_{IN(+L)}$ and $A_{IN(–L)}$.

$A_{IN(+R)}$, $A_{IN(–R)}$
Right Channel Analog Inputs (Pins 24, 23)

These two pins comprise the right channel analog differential inputs. The voltage range of signals applied to these pins is from $V_{SS(A)}$ to $V_{DD(A)}$. A positive full–scale input to the A/D is defined as a difference of 3.8 V p–p between $A_{IN(+R)}$ and $A_{IN(–R)}$.

REF
Output of the Internal Voltage Reference (Pin 3)

The nominal value of this internal voltage reference is 2 V. The output of the reference is brought out to this pin to facilitate filtering. For proper device operation, this pin should be decoupled to $V_{SS(A)}$ with a 1.0 μF electrolytic capacitor in parallel with a 0.1 μF ceramic capacitor. In order to economize on filtering capacitors, the REF pin can be connected to V_{AG}. However, this could result in a possible degradation of performance of the device at high signal levels.

V_{AG}
Output of the Internal Analog Ground Generator (Pin 22)

Analog ground is used to bias the internal analog circuits and is nominally 2 V. V_{AG} is brought out to this pin to facilitate filtering. This pin should be decoupled to $V_{SS(A)}$ with a 1.0 μF electrolytic capacitor in parallel with a 0.1 μF ceramic capacitor for normal device operation.

DIGITAL PINS

CLK
Master Clock Input (Pin14)

This pin is the master clock input for the device. Analog input signals to the MC145073 are sampled at a rate equal to this clock frequency divided by 1, 2, or 3, depending on the state of clock mode pins CSEL1,0. The serial data output rate is equal to the input sample rate divided by 128. For example, if CLK is running at a 12.288 MHz rate, and divide by 2 is selected, then the output data rate is (12.288 MHz/2)/128 = 48 kHz. For more detail, see the **Summary of Operating Modes** section.

SYNC
Serial Interface Frame Sync Input/Output (Pin 11)

The SYNC pin is an input or output depending on the state of the I_{SLAV} pin. The SYNC signal resets and synchronizes the serial interface transmitter and receivers, as well as most internal clocks. Left channel serial output data is transmitted when the SYNC signal is active high, and right channel data is transmitted when the SYNC signal is low. See the **Serial Interface Description** section for more information.

SCLK
Serial Interface Clock Input/Output (Pin 12)

The SCLK pin is an input or output depending on the state of the I_{SLAV} pin. Serial output data is clocked out of the MC145073 on the rising edge of SCLK. When SCLK is an input, it is reclocked by the internal sample rate clock, CLKI, before being used by the MC145073 to clock out the serial data. This reclocking ensures that rapid current changes through the SDO pin do not affect the analog performance of the device. See the **Serial Interface Description** section for more information.

SDO
Serial Interface Data Output (Pin 13)

The A/D conversion results for the left and right channels are output on this pin. Data is shifted out of the MC145073 MSB first, with the left channel data preceding the right channel data. The serial output data is clocked out on the rising edge of SCLK. See the **Serial Interface Description** section for more information.

FTP
Factory Test Mode Inputs (Pins 9, 10)

These pins should be connected to $V_{SS(A)}$ for normal device operation.

CSEL0, CSEL1
Clock Divide Mode Select Inputs (Pins 21, 20)

The device master clock input is divided by 1, 2, or 3, or the device is placed in a power–down mode depending on the state of these pins. See the **Summary of Operating Modes** section for more information.

FSEL
FIR Filter Response Select Input (Pin 19)

A low level on the FSEL input selects a FIR filter transition band from 20 to 25.8 kHz at the 48 kHz output data rate. A high level on the FSEL pin selects a filter transition band from 20 to 24 kHz at the 44.1 kHz output data rate. See the **Summary of Operating Modes** section for more information.

I_{SYNC}
Serial Interface Sync Format Select Input (Pin 18)

A low level input on the I_{SYNC} pin selects a SYNC rising edge one SCLK cycle before the initiation of a serial data transfer. A high level on the I_{SYNC} pin will select a SYNC rising edge that is coincident with the initiation of a serial data transfer. See the **Summary of Operating Modes** and the **Serial Interface Description** sections for more information.

I_{SLAV}
Serial Interface Slave Mode Select Input (Pin 17)

This pin controls the direction of the serial interface SYNC and SCLK signals. A low level on the I_{SLAV} pin will configure the SYNC and SCLK pins as outputs, while a high level on the I_{SLAV} pin will configure the SYNC and SCLK pins as inputs. See the **Summary of Operating Modes** and the **Serial Interface Description** sections for more information.

I_{JUST}
Serial Interface Data Justification Select Input (Pin 16)

A low level on the I_{JUST} pin will cause the serial output data to be left justified relative to the SYNC signal. A high level on the I_{JUST} pin will select right justification of the serial output data. See the **Summary of Operating Modes** and the **Serial Interface Description** sections for more information.

I_{DOE}
Serial Interface Data Output Enable (Pin 15)

This pin controls the state of the SDO pin between 16–bit data word transfers. A high level on this pin will force the SDO pin to a low level between serial data words, while a low level on the I_{DOE} pin will force the SDO pin to a high–impedance state between data words. See the **Summary of Operating Modes** and the **Serial Interface Description** sections for more information.

POWER SUPPLY PINS

$V_{DD(A)}$ (Pin 4)

Positive analog power supply input. The voltage range for this pin is 4.5 to 5.5 V with respect to $V_{SS(A)}$. The absolute value of the difference between $V_{DD(A)}$ and $V_{DD(D)}$ must not exceed 0.5 V. For proper device operation, this pin should be decoupled to $V_{SS(A)}$ with a 1.0 μF or larger capacitor.

$V_{SS(A)}$ (Pin 5)

Negative analog power supply input. This pin should be connected to ground for normal device operation.

$V_{DD(D)}$ (Pin 8)

Positive digital power supply input. The voltage range for this pin is 4.5 to 5.5 V with respect to $V_{SS(D)}$. The absolute value of the difference between $V_{DD(A)}$ and $V_{DD(D)}$ must not exceed 0.5 V. For proper device operation, this pin should be decoupled to $V_{SS(D)}$ with a 1.0 μF or larger capacitor.

$V_{SS(D)}$ (Pin 7)

Negative digital power supply input. This pin should be connected to ground for normal device operation.

SUB (Pin 6)

Substrate connection. This pin should be connected to $V_{SS(A)}$ for normal device operation.

FUNCTIONAL DESCRIPTION

The MC145073 is a 16–bit stereo audio A/D converter intended for use in digital audio systems. The MC145073 uses a sigma–delta architecture consisting of a second order analog modulator followed by two stages of digital filtering for each channel. The analog modulator samples the input signal at a very high rate (128x the output data rate), performs a single bit quantization, and shapes the quantization noise towards out–of–band frequencies. The digital filters of the MC145073 reject most of the shaped quantization noise, and lower the serial data output rate. The digital filtering is implemented with a 5^{th} order, decimate–by–32 comb filter followed by a 121 tap, decimate–by–4, FIR filter on each channel. In addition to rejecting quantization noise, the FIR filter cancels the curvature in the response of the preceding comb filter. The comb and FIR filters also provide anti–alias filtering of out–of–band signals present at the input to the device. The analog inputs to the MC145073 can be fully differential (both inputs dynamic and 180 degrees out of phase), or single–ended (positive inputs dynamic while negative inputs are static at a level in the middle of the supply range). Analog input signals that exceed the differential analog input voltage range of 3.8 V p–p are clipped in order to prevent overflow of the digital filters. The MC145073 operates from a single 5 V power supply. For portable or other low power applications, a power–down mode is available.

The operation of the MC145073 can be tailored to specific applications by proper selection of the states of seven mode select pins. These mode pins control the divide ratio of the master clock, the FIR filter response, and the serial interface format. The master clock input can be divided by either 1, 2, or 3 to yield the input sampling rate. This means that the input clock frequency is either 128x, 256x, or 512x the serial output data rate.

NOTE

The oversampling ratio (OSR), which is the ratio of input sampling frequency to output data rate, is 128x in all three cases.

Two sets of FIR filter coefficients are stored in the on–board ROM of the MC145073. One set provides a transition band from 20 kHz to 25.8 kHz for operation at the 48 kHz output data rate. The other set of FIR filter coefficients provides a transition band from 20 kHz to 25 kHz for use with the 44.1 kHz output data rate.

Four mode select pins configure the serial interface. This yields sixteen possible serial interface operating modes. Included are modes that provide for interfacing directly to Motorola and TI general purpose DSPs, multiplexing of two MC145073s, as well as formats similar to the CS5326 interface.

SUMMARY OF DEVICE OPERATING MODES

The seven pins summarized in the tables below configure the MC145073 to operate in one of the modes specified. The modes can be chosen in any combination.

CSEL1	CSEL0	Master CLK Divider Select
0	0	Power–Down
0	1	Divide CLK by 1
1	0	Divide CLK by 2
1	1	Divide CLK by 3

FSEL	FIR Filter Transition Band Select
0	20 kHz – 25.8 kHz Transistion Band 6.144 MHz Input Rate, 48 kHz Output Data Rate.
1	20 kHz – 25 kHz Transistion Band 5.6448 MHz Input Rate, 44.1 kHz Output Data Rate

I_{SYNC}	Serial Interface SYNC Signal Format
0	SYNC rising edge is one SCLK cycle before the start of the serial output data transfer. (This is compatible with the DSP5600/56001 and TMS320 interface definitions.)
1	SYNC rising edge is coincident with the start of the serial output data transfer. (This is compatible with the CS5326 interface definition.)

I_{SLAV}	Serial Interface Master or Slave Select
0	MC145073 is a master, SYNC and SCLK are outputs.
1	MC145073 is a slave, SYNC and SCLK are inputs (re–clocked by the MC145073 internal clock, CLKI).

I_{JUST}	Serial Interface Data Justification Select
0	Serial output data is left justified relative to the SYNC signal.
1	Serial output data is right justified relative to the SYNC signal.

I_{DOE}	Serial Interface Data Output Enable
0	SDO goes to a high–impedance state between 16–bit output words.
1	SDO is forced low between 16–bit output words.

SERIAL INTERFACE DESCRIPTION

As summarized in the previous section, the format of the serial interface is controlled by four mode pins: I_{SYNC}, I_{SLAV}, I_{JUST}, and I_{DOE}. These control inputs can be configured in any combination, yielding $2^4 = 16$ unique modes. The following two subsections describe the format of the serial interface for these various modes. Timing information for the serial interface is provided in the **AC Electrical Specifications** section .

Compatibility with the DSP56000/1 and TMS320 general–purpose DSPs is accomplished by applying the appropriate logic level to the I_{SYNC} pin. The phase of the rising edge of the SYNC signal is different for the DSP56000 and TMS320 applications, while the falling edge of SYNC is not critical in such applications.

To interface to one or two MC145073s, the DSP56000/56001 should be configured as follows: network mode, four time slots per frame, 16 bits per slot, continuous clock, and control signals configured as either a master or slave. If interfacing to a TMS320 is desired, the serial interface should be configured in continuous mode without frame sync.

NOTE

The TMS320 interface must be initialized with frame sync enabled, and then switched to the no frame sync mode after initialization.

The I_{JUST} and I_{DOE} serial interface mode control inputs are provided to facilitate multiplexing of two MC145073s. The I_{JUST} input selects between left and right justification of the serial output data relative to the SYNC signal, while the I_{DOE} input provides a way to force the SDO pin to the high impedance state between the output data words. To multiplex the serial data outputs of two MC145073s onto the same SDO line, I_{DOE} must be forced low on both MC145073s, while the I_{JUST} pin is forced high on one MC145073 and low on the other. The MC145073s must be in the slave mode (I_{SLAV}=1) when multiplexing. It is not possible to operate with one MC145073 as a master tied to a second MC145073 operating as a slave due to the reclocking of the SYNC and SCLK inputs in the slave mode (see **Operation with the MC145073 as a Slave (I_{SLAV} = 1)** section).

NOTE

When multiplexing two MC145073 devices, all four analog channels are sampled at exactly the same phase.

In Figures 10 and 11, the internal clock signal CLKI is plotted instead of CLK. This is due to the fact that all internal clocks, as well as the serial interface, are slaved to this divided version of the master clock. Input signals to the serial interface are reclocked by CLKI to reduce the amount of noise injected into the analog section of the MC145073. Serial output data and high–impedance states of the SDO pin are clocked out relative to CLKI. This reclocking can cause a shift in phase of SDO relative to SCLK when operating in the slave mode. In cases where the MC145073 output is multiplexed with another device, the clock divide by 1 mode is recommended.

NOTE

If the clock divide by 2 or 3 mode is selected, it is impossible to know the exact phase of CLKI.

On initial power–up or recovery from a power–down condition, the first 68 serial output words of the MC145073 are indeterminate. This is because the digital filters and internal logic of the MC145073 must settle. This time is also used to charge the external REF filter capacitor.

Operation with the MC145073 as a Master (I_{SLAV} = 0)

When I_{SLAV} = 0, the SYNC and SCLK signals are defined as outputs, and the MC145073 is configured as master device. In this mode there are eight possible serial formats as illustrated in Figure 10. The phase of the SYNC output can precede the serial output data by one SCLK cycle (compatible with DSP56000/56001, TMS320, and I^2S interface format), or the SYNC signal can be coincident with the serial output data (similar to the CS5326 serial interface format). As shown in Figure 10, with each of these two SYNC formats there are four possible formats for the serial output data.

Serial output data is shifted out MSB first, with left channel data preceding the right channel data. All of the serial interface outputs, SYNC, SCLK, and SDO are initiated by a CLKI rising edge. There are 128 CLKI cycles, and 64 SCLK cycles per output data cycle. Multiplexing of two MC145073s is not feasible in the master mode since the exact phase of the output cannot be controlled.

NOTE

The serial data in one output cycle represents data that was simultaneously sampled on the two analog input channels.

It is possible to initiate the device in the slave mode described in the **Operation with the MC145073 as a Slave (I_{SLAV} = 1)** section, and then switch to master mode. Once set, the phase of SYNC should not change.

Operation with the MC145073 as a Slave (I_{SLAV} = 1)

When I_{SLAV} = 1 the SYNC and SCLK signals are defined as inputs, and the MC145073 is configured as a slave device. However, the slave mode of the MC145073 is not a true slave mode since the SYNC and SCLK inputs are reclocked by the internal sample clock, CLKI. These internal reclocked versions of SYNC and SCLK are shown in Figure 11, in addition to the external SYNC and SCLK signals.

Similar to the master mode of the previous section, there are two formats for the SYNC signal, and four SDO formats, yielding eight possible slave modes.

Multiplexing of two MC145073s in the slave mode is performed by forcing I_{DOE} low on both MC145073s, and forcing I_{JUST} high on one MC145073 and low on the other.

NOTE

When multiplexing two MC145073s, the master clock divide by 1 mode should be used (CSEL1,0 = 0,1) so that the exact phase of CLKI is determined.

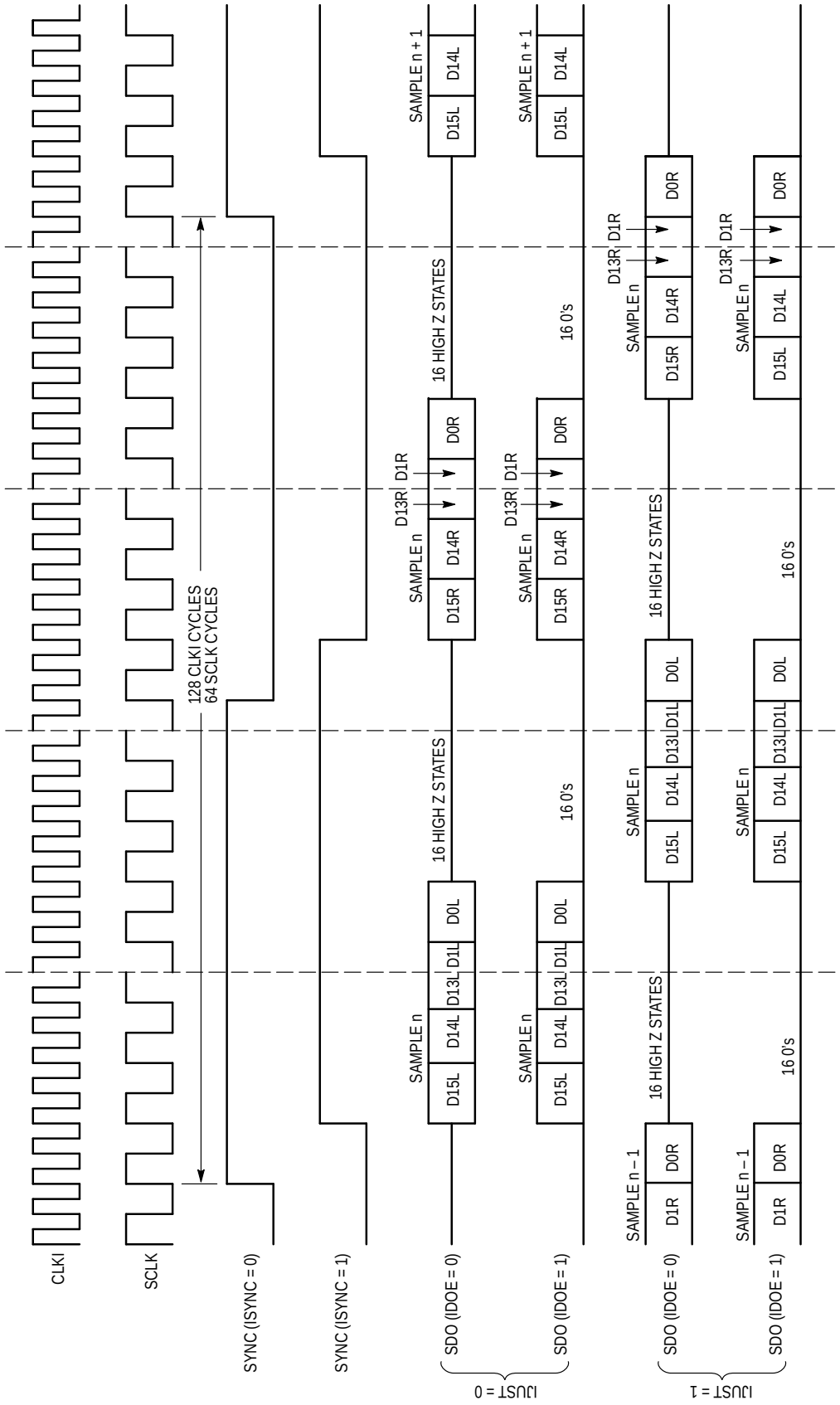


Figure 10. Serial Interface Operation with MC145073 Configured as Master (I_{SLAV} = 0)

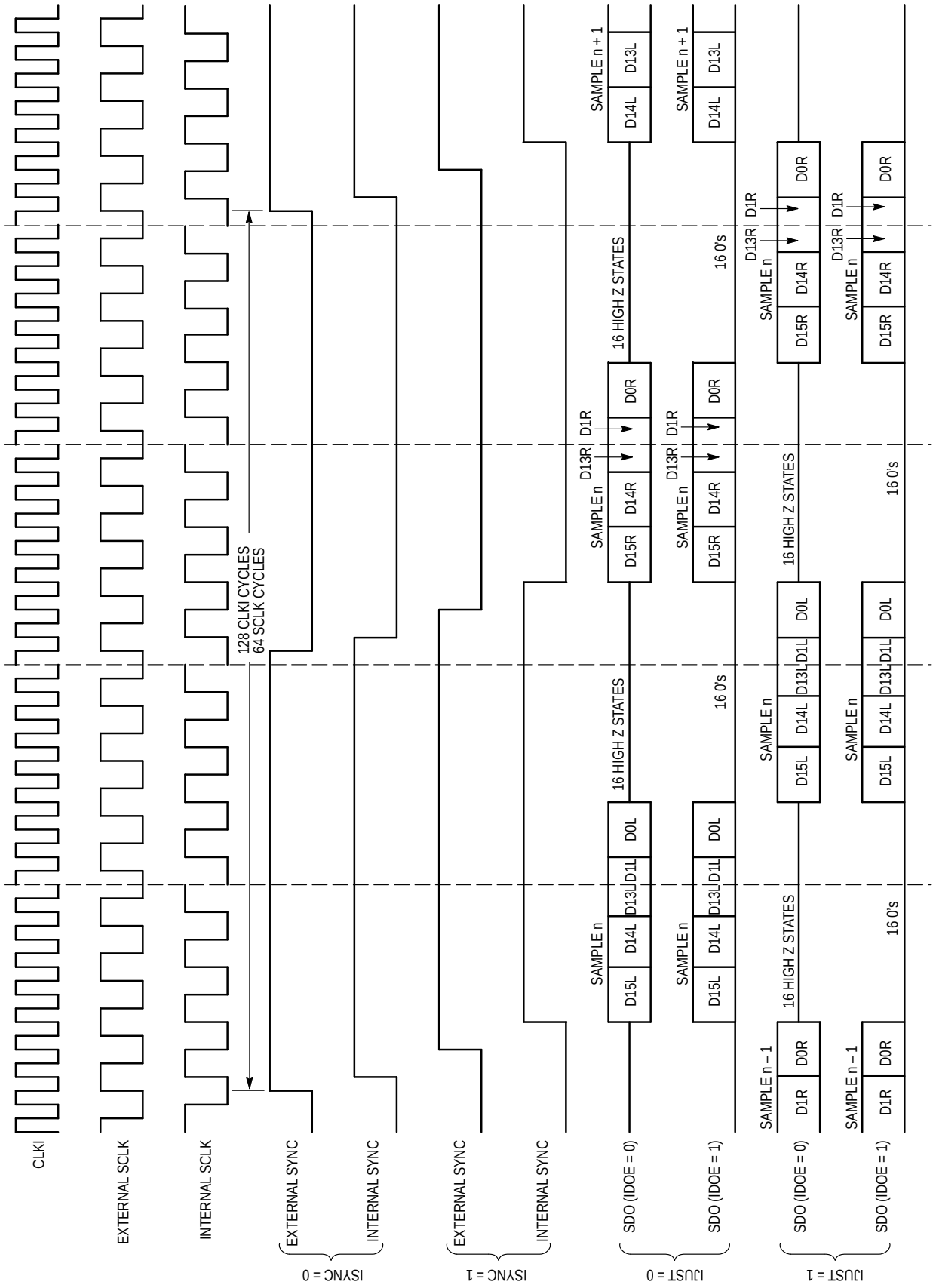
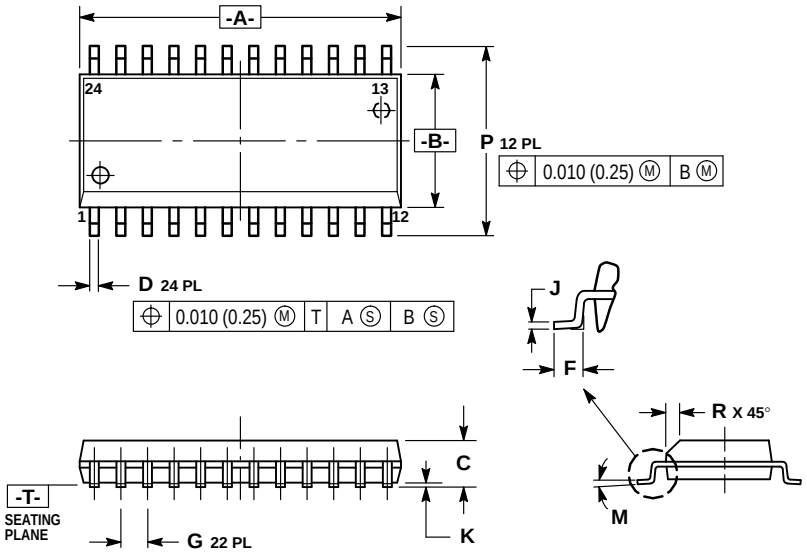


Figure 11. Serial Interface Operation with MC145073 Configured as Slave (I_{SLAV} = 1)

PACKAGE DIMENSIONS

DW SUFFIX
SOG PACKAGE
CASE 751E–04



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

How to reach us:

USA / EUROPE / Locations Not Listed: Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado 80217. 303–675–2140 or 1–800–441–2447

Mfax™: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609
– US & Canada ONLY 1–800–774–1848

INTERNET: http://motorola.com/sps

JAPAN: Nippon Motorola Ltd.: SPD, Strategic Planning Office, 4–32–1,
Nishi–Gotanda, Shinagawa–ku, Tokyo 141, Japan. 81–3–5487–8488

ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298