

## Dual PLLs for 46/49 MHz Cordless Telephones CMOS

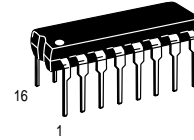
These devices are dual phase-locked loop (PLL) frequency synthesizers intended for use primarily in 46/49 MHz cordless phones with up to 10 channels. These parts contain two mask-programmable counter ROMs for receive and transmit loops with two independent phase detect circuits. A common reference oscillator and reference divider are shared by the receive and transmit circuits.

Frequency selection is accomplished via a 4-bit parallel input for the MC145166. The MC145167 utilizes a serial interface.

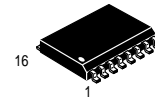
Other features include a lock detect circuit for the transmit loop, illegal code default, and a 5 kHz tone output.

- Synthesizes Up to Ten Channel Pairs
- Maximum Operating Frequency: 60 MHz @  $V_{in} = 200 \text{ mV p-p}$
- Operating Temperature Range:  $-40$  to  $+75^\circ\text{C}$
- Operating Voltage Range: 2.5 to 5.5 V
- On-Chip Oscillator Circuit Supports External Crystal
- Lock Detect Signal
- Operating Power Consumption: 3.0 mA @ 3.0 V
- Standby Mode for Power Savings: 1.5 mA @ 3.0 V
- Also See MC145162

### MC145166 MC145167



**P SUFFIX**  
PLASTIC DIP  
CASE 648



**DW SUFFIX**  
SOG PACKAGE  
CASE 751G

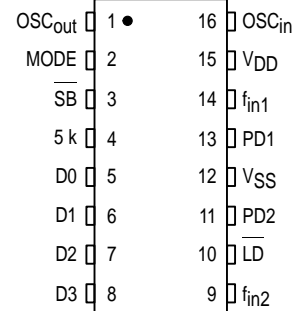
#### ORDERING INFORMATION

MC145166P Plastic DIP  
MC145166DW SOG Package

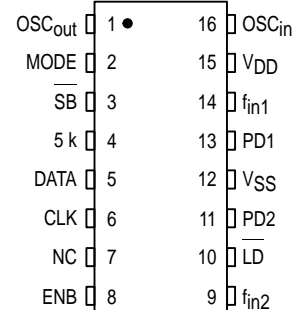
MC145167P Plastic DIP  
MC145167DW SOG Package

#### PIN ASSIGNMENTS

##### MC145166P MC145166DW



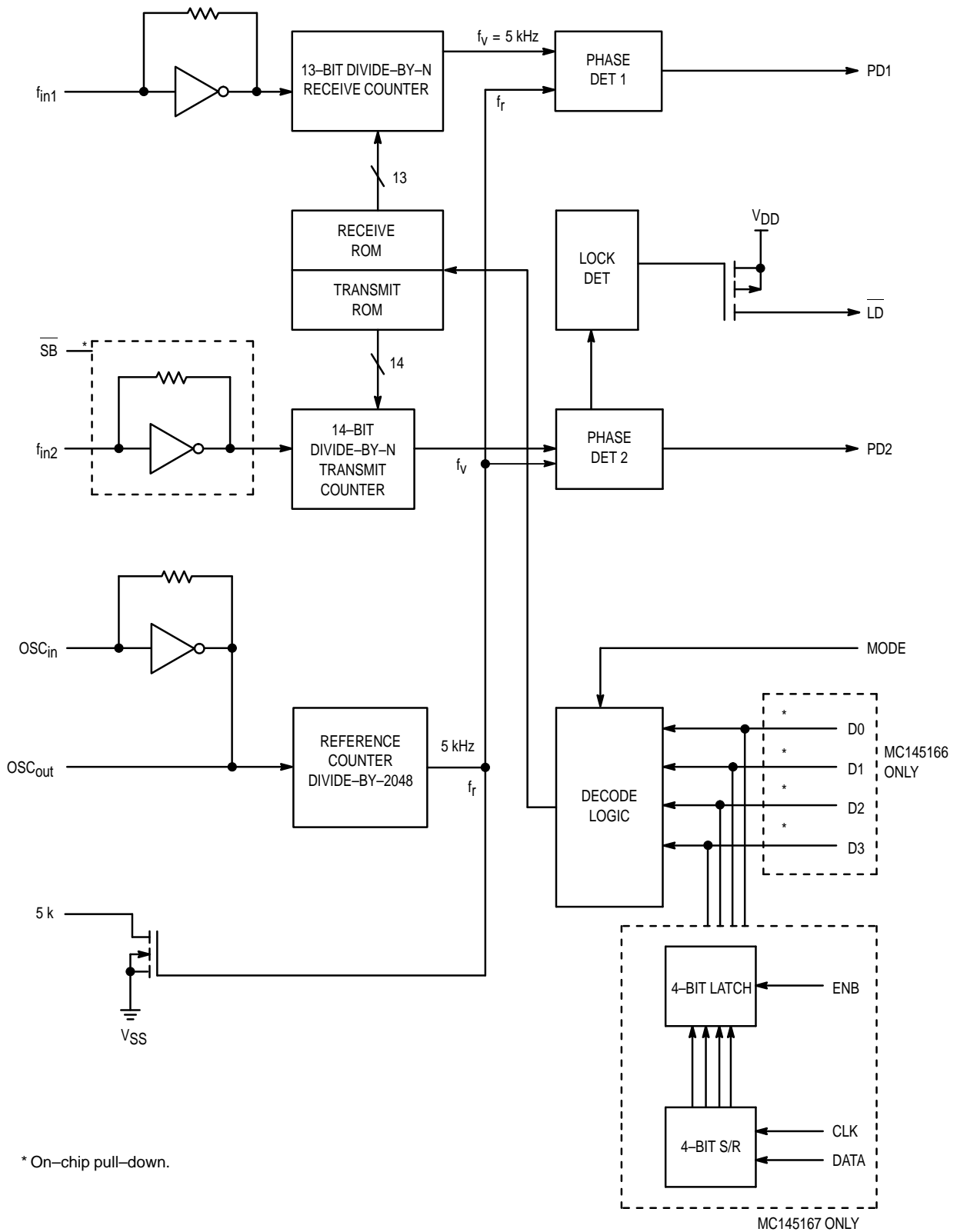
##### MC145167P MC145167DW



NC = NO CONNECTION



### BLOCK DIAGRAM



**MAXIMUM RATINGS\*** (Voltages Referenced to  $V_{SS}$ )

Symbol	Rating	Value	Unit
$V_{DD}$	DC Supply Voltage	- 0.5 to + 6.0	V
$V_{in}$	Input Voltage, All Inputs	- 0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	DC Current Drain Per Pin	10	mA
$I_{DD}, I_{SS}$	DC Current Drain $V_{DD}$ or $V_{SS}$ Pins	30	mA
$T_{stg}$	Storage Temperature Range	- 65 to + 150	°C

\* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to  $V_{SS}$ ,  $T_A = 25^\circ\text{C}$ )

Symbol	Characteristic	$V_{DD}$	Guaranteed Limit		Unit	
			Min	Max		
$V_{DD}$	Power Supply Voltage Range	—	2.5	5.5	V	
$V_{OL}$	Output Voltage ( $I_{out} = 0$ )	0 Level	2.5	—	0.05	V
			5.5	—	0.05	
$V_{OH}$	( $V_{in} = V_{DD}$ or 0 )	1 Level	2.5	2.45	—	
			5.5	5.45	—	
$V_{IL}$	Input Voltage ( $V_{out} = 0.5 \text{ V}$ or $V_{DD} - 0.5 \text{ V}$ )	0 Level	2.5	—	0.75	V
			5.5	—	1.65	
$V_{IH}$		1 Level	2.5	1.75	—	
			5.5	3.85	—	
$I_{OH}$	Output Current ( $V_{out} = 2.2 \text{ V}$ ) ( $V_{out} = 5.0 \text{ V}$ )	Source	2.5	- 0.18	—	mA
			5.5	- 0.55	—	
$I_{OL}$	( $V_{out} = 0.3 \text{ V}$ ) ( $V_{out} = 0.5 \text{ V}$ )	Sink	2.5	0.18	—	
			5.5	0.55	—	
$I_{IL}$	Input Current ( $V_{in} = 0$ )	OSC <sub>in</sub> , $f_{in1}$ , $f_{in2}$	2.5	—	- 30	$\mu\text{A}$
			5.5	—	- 66	
		DATA, $\overline{\text{SB}}$ , Mode	2.5	—	- 0.05	
			5.5	—	- 0.11	
$I_{IH}$	( $V_{in} = V_{DD} - 0.5$ )	OSC <sub>in</sub> , $f_{in1}$ , $f_{in2}$	2.5	—	30	$\mu\text{A}$
			5.5	—	66	
		DATA, $\overline{\text{SB}}$ , Mode	2.5	—	50	
			5.5	—	121	
$C_{in}$	Input Capacitance	—	—	14.0	pF	
$C_{out}$	Output Capacitance	—	—	8.0	pF	
$I_{DD}$	Standby Current, $\text{SB} = V_{SS}$ or Open	2.5	—	1.4	mA	
		5.5	—	3.6		
$I_{dd}$	Operating Current (200 mV p-p input at $f_{in1}$ and $f_{in2}$ , $\overline{\text{SB}} = V_{DD}$ )	2.5	—	2.8	mA	
		5.5	—	6.2		
$I_{OZ}$	Three-State Leakage Current ( $V_{out} = 0$ or $5.5 \text{ V}$ )	5.5	—	$\pm 1.0$	$\mu\text{A}$	

**SWITCHING CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$ )

Symbol	Characteristic	Figure No.	$V_{DD}$	Guaranteed Limit		Unit
				Min	Max	
$t_{TLH}$	Output Rise Time	1, 5	3.0 5.0	— —	200 100	ns
$t_{THL}$	Output Fall Time	1, 5	3.0 5.0	— —	200 100	ns
$t_r, t_f$	Input Rise and Fall Time, $OSC_{in}$	2	3.0 5.0	— —	5.0 4.0	$\mu\text{s}$
$f_{max}$	Input Frequency Input = Sine Wave 200 mV p-p	$OSC_{in}$ $f_{in1}$ $f_{in2}$	3.0 – 5.0 3.0 – 5.0 3.0 – 5.0	— — —	12 60 60	MHz
$t_{su}$	Setup Time (MC145167)	DATA to CLK	3.0 5.0	100 50	— —	ns
		ENB to CLK	3.0 5.0	200 100	— —	
$t_h$	Hold Time (MC145167), CLK to DATA	3	3.0 5.0	80 40	— —	ns
$t_{rec}$	Recovery Time (MC145167), ENB to CLK	3	3.0 5.0	80 40	— —	ns
$t_w$	Input Pulse Width (MC145167), CLK and ENB	4	3.0 5.0	80 60	— —	ns

## SWITCHING WAVEFORMS

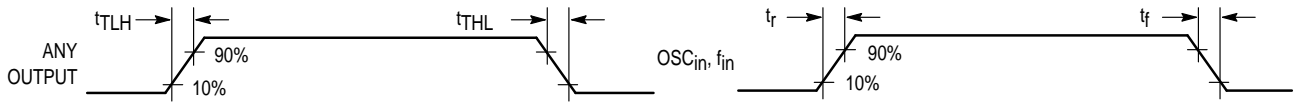


Figure 1.

Figure 2.

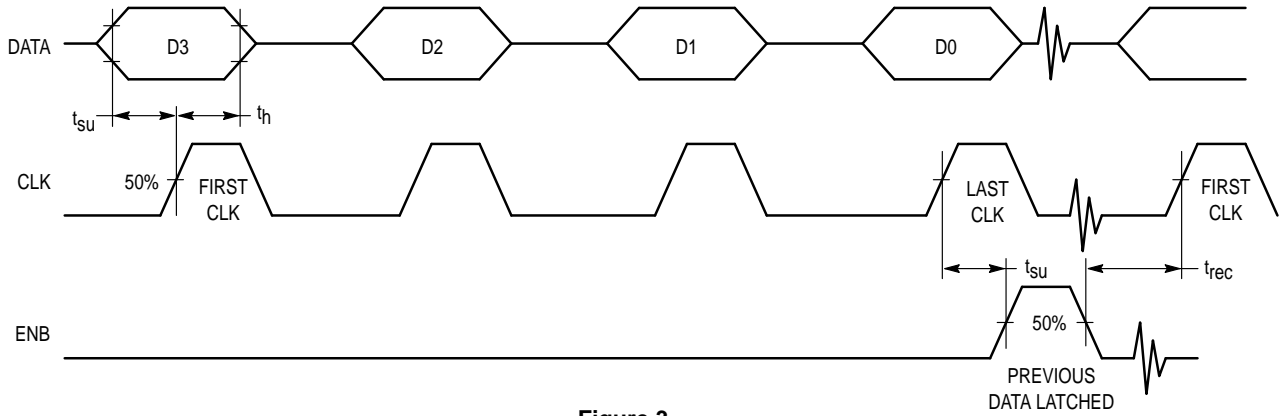


Figure 3.

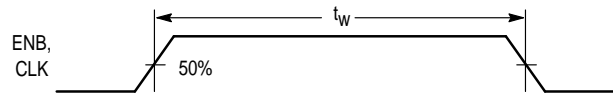


Figure 4.

## PIN DESCRIPTIONS

### INPUT PINS

#### OSC<sub>in</sub>/OSC<sub>out</sub>

##### Reference Oscillator Input/Output (Pins 1,16)

These pins form a reference oscillator when connected to an external parallel-resonant crystal. For a 46/49 MHz cordless phone application, a 10.24 MHz crystal is needed. OSC<sub>in</sub> may also serve as input for an externally generated reference signal. This signal is typically ac coupled to OSC<sub>in</sub>, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required for OSC<sub>out</sub>.

#### MODE

##### Mode Select (Pin 2)

Mode is for determining whether the part is to be used in the base or handset of a cordless phone. Internally, this pin is used in the decoding logic for selecting the ROM address. When high, the device is set in the base mode, and when low, it is set in the handset mode. This input has an internal pull-down device.

#### SB

##### Standby Input (Pin 3)

The standby pin is used to save power when not transmitting. When high, both the transmit and receive loops are in operation. When low, the transmit loop is disabled, thereby reducing power consumption. This input has an internal pull-down device.

#### D0 – D3

##### Data Inputs (MC145166 — Pins 5 – 8)

These inputs provide the BCD code for selecting the one of ten channels to be locked in both the transmit and receive loop. When address data other than 1 – 10 are input, the decoding logic defaults to channel 10. The frequency assignments with reference to Mode and D0 – D3 are shown in Table 1. These inputs have internal pull-down devices.

#### f<sub>in1</sub>, f<sub>in2</sub>

##### Frequency Inputs (Pins 14, 9)

f<sub>in1</sub> and f<sub>in2</sub> are inputs to the divide-by-N receive and transmit counters, respectively. These signals are typically derived from the loop VCO and are ac coupled. For larger amplitude signals (standard CMOS logic levels), dc coupling may be used. The minimum input level is 200 mV p-p.

#### CLK, DATA

##### Clock, Data (MC145167 — Pins 5, 6)

These pins provide the BCD input by using serial channel programming instead of parallel. Logical high represents a 1. Each low-to-high transition of the clock shifts one bit of data into the on-chip shift register.

#### ENB

##### Enable (MC145167 — Pin 8)

The enable pin controls the data transfer from the shift register to the 4-bit latch. A positive pulse latches the data.

### OUTPUT PINS

#### 5 k

##### 5 kHz Tone Signals (Pin 4)

The 5 kHz tone signals are N-channel, open-drain outputs derived from the reference oscillator.

#### LD

##### Lock Detect Signal (Pin 10)

The lock detect signal is associated with the transmit loop. The lock output goes high to indicate an out-of-lock condition. This is a P-channel open-drain output.

#### PD1, PD2

##### Phase Detector Outputs (Pins 13, 11)

These are three-state outputs of the transmit and receive phase detectors for use as loop error signals. Phase detector gain is  $V_{DD}/4\pi$  volts per radian.

- Frequency  $f_v > f_r$  or  $f_v$  leading: Output = Negative pulses
- Frequency  $f_v < f_r$  or  $f_v$  lagging: Output = Positive pulses
- Frequency  $f_v = f_r$  and phase coincidence: Output = High-impedance state

### POWER SUPPLY

#### V<sub>SS</sub>

##### Negative Power Supply (Pin 12)

This pin is the negative supply potential and is usually ground.

#### V<sub>DD</sub>

##### Positive Power Supply (Pin 15)

This pin is the positive supply potential and may range from +2.5 to +5.5 V with respect to V<sub>SS</sub>.

**Table 1. MC145166/67 Divide Ratios and VCO Frequencies**

Channels					Handset (Mode = 0)				Base (Mode = 1)			
					Transmit		Receive		Transmit		Receive	
D3	D2	D1	D0	CH#	f <sub>in2</sub> (MHz)	÷ N	f <sub>in1</sub> (MHz)	÷ N	f <sub>in2</sub> (MHz)	÷ N	f <sub>in1</sub> (MHz)	÷ N
0	0	0	1	1	49.670	9934	35.915	7183	46.610	9322	38.975	7795
0	0	1	0	2	49.845	9969	35.935	7187	46.630	9326	39.150	7830
0	0	1	1	3	49.860	9972	35.975	7195	46.670	9334	39.165	7833
0	1	0	0	4	49.770	9954	36.015	7203	46.710	9342	39.075	7815
0	1	0	1	5	49.875	9975	36.035	7207	46.730	9346	39.180	7836
0	1	1	0	6	49.830	9966	36.075	7215	46.770	9354	39.135	7827
0	1	1	1	7	49.890	9978	36.135	7227	46.830	9366	39.195	7839
1	0	0	0	8	49.930	9986	36.175	7235	46.870	9374	39.235	7847
1	0	0	1	9	49.990	9998	36.235	7247	46.930	9386	39.295	7859
1	0	1	0	10	49.970	9994	36.275	7255	46.970	9394	39.275	7855

NOTES:

1. Other input combinations will be defaulted to channel 10.
2. 0 = logic low, 1 = logic high.

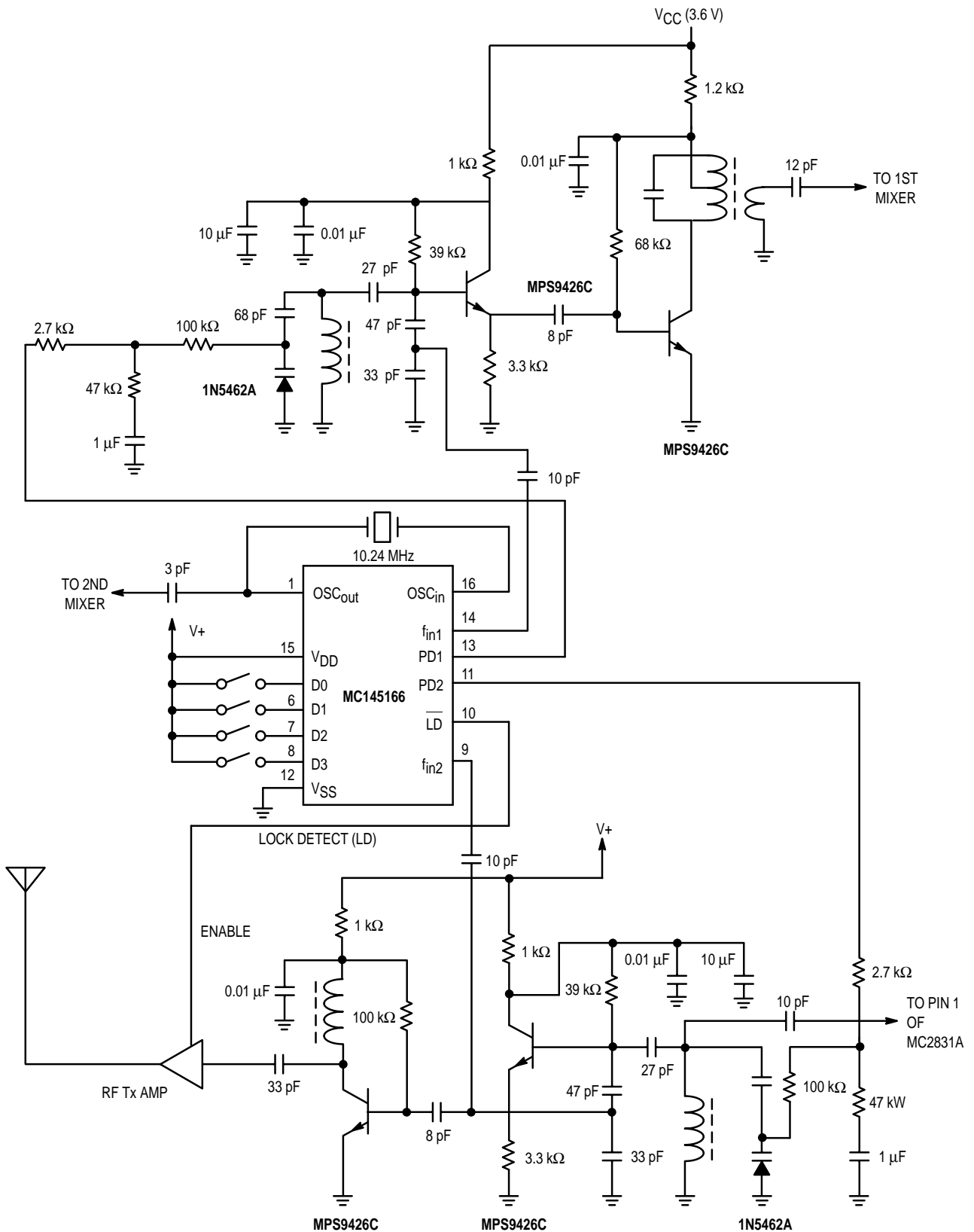


Figure 5. MC145166 Circuit Example



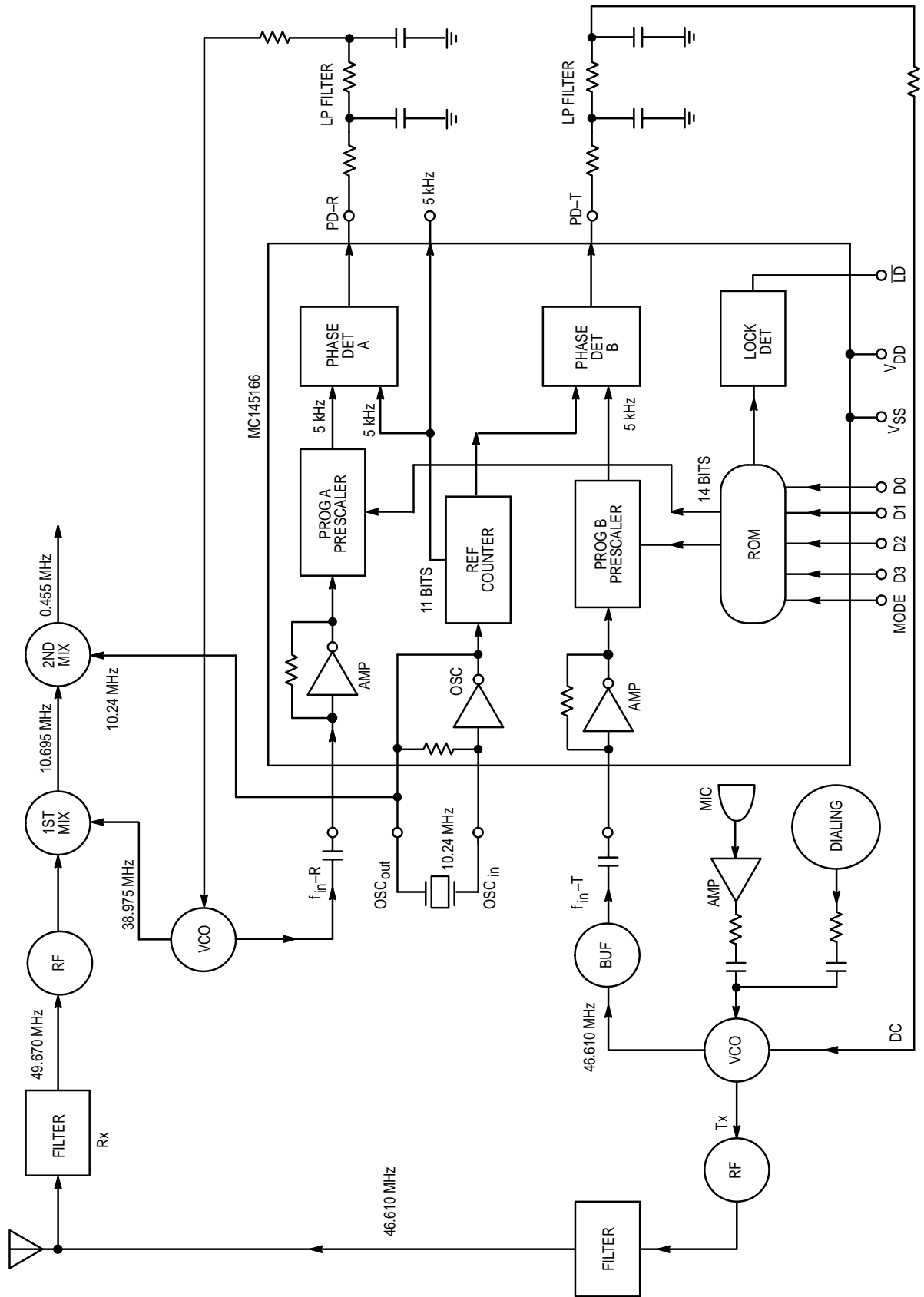
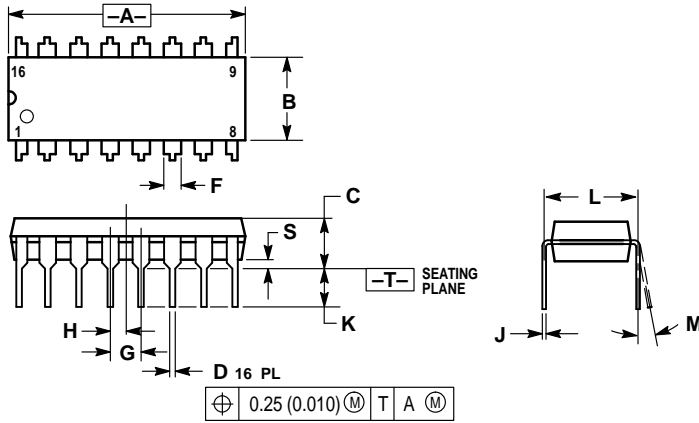


Figure 6. DPLL Application in 46/49 MHz Cordless Phone

## PACKAGE DIMENSIONS

### P SUFFIX PLASTIC DIP CASE 648-08

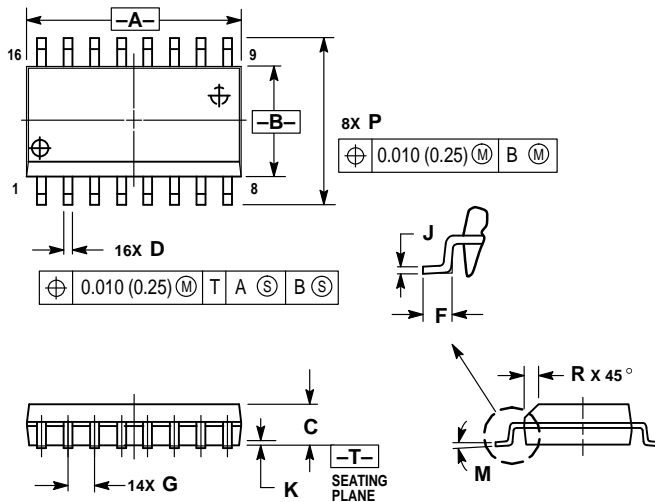


#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01


### DW SUFFIX SOG PACKAGE CASE 751G-02



#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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