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# MC44827/27B

## Low Power PLL Tuning Circuits for 3-Wire Bus

The MC44827/27B are tuning circuits for TV and VCR tuner applications. They contain on one chip all the functions required for PLL control of a VCO. The integrated circuits also contain a high frequency prescaler and thus can handle frequencies up to 1.3 GHz.

The MC44827 has programmable 512/1024 reference divider while the MC44827B has a fixed reference divider of 1024.

The MC44827/27B offer the same features as MC44817/17B but has improved sensitivity performance and reduced power dissipation. The low frequency preamplifier has been removed and the operational amplifier pull-up resistor has been increased to 60 kΩ.

The MC44827/27B are controlled via a 3-wire bus. The MC44827/27B have the same functions as the MC44828 which is I<sup>2</sup>C bus controlled. The MC44827/27B and the MC44828 can be exchanged to allow conversion between 3-wire bus and I<sup>2</sup>C bus control.

The MC44827/27B are manufactured on a single silicon chip using Motorola's high density bipolar process, MOSAIC™ (Motorola Oxide Self Aligned Implanted Circuits).

- Complete Single Chip System for MPU Control (3-Wire Bus). Data and Clock Inputs are I<sup>2</sup>C Bus Compatible
- Divide-by-8 Prescaler Accepts Frequencies up to 1.3 GHz
- 15 Bit Programmable Divider Accepts Input Frequencies up to 165 MHz
- 3-State Phase/Frequency Comparator
- Operational Amplifier for Direct Tuning Voltage Output (30 V)
- Four Integrated PNP Band Buffers can drive up to 40 mA (V<sub>CC1</sub> to 14.4 V)
- Output Options for the Reference Frequency and the Programmable Divider
- Bus Protocol for 18 or 19 Bit Transmission
- Extra 34-Bit Protocol for Test and Further Features
- High Sensitivity Preamplifier
- Lower Power Consumption, 200 mW Typical
- Improved Prescaler with Higher Margins for Sensitivity and Temperature Range
- Lock Detector with Push-Pull Output
- Space-Saving TSSOP Package
- ESD Protected to MIL-STD-883C, Method 3015.7 (1.5 kΩ, 100 pF)

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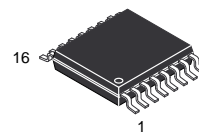
### ORDERING INFORMATION

| Device      | Operating Temperature Range    | Package  |
|-------------|--------------------------------|----------|
| MC44827DTB  | T <sub>A</sub> = -20° to +80°C | TSSOP-16 |
| MC44827BDTB |                                |          |

### LOW-POWER PLL TUNING CIRCUIT

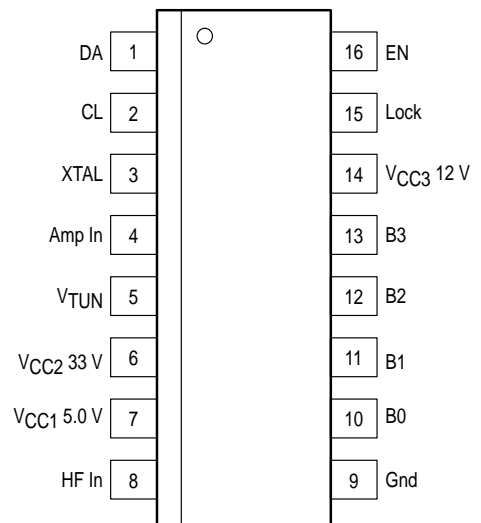
FOR 3-WIRE BUS WITH 1.3 GHz PRESCALER

SEMICONDUCTOR TECHNICAL DATA



DTB SUFFIX  
PLASTIC PACKAGE  
CASE 948F  
(TSSOP-16)

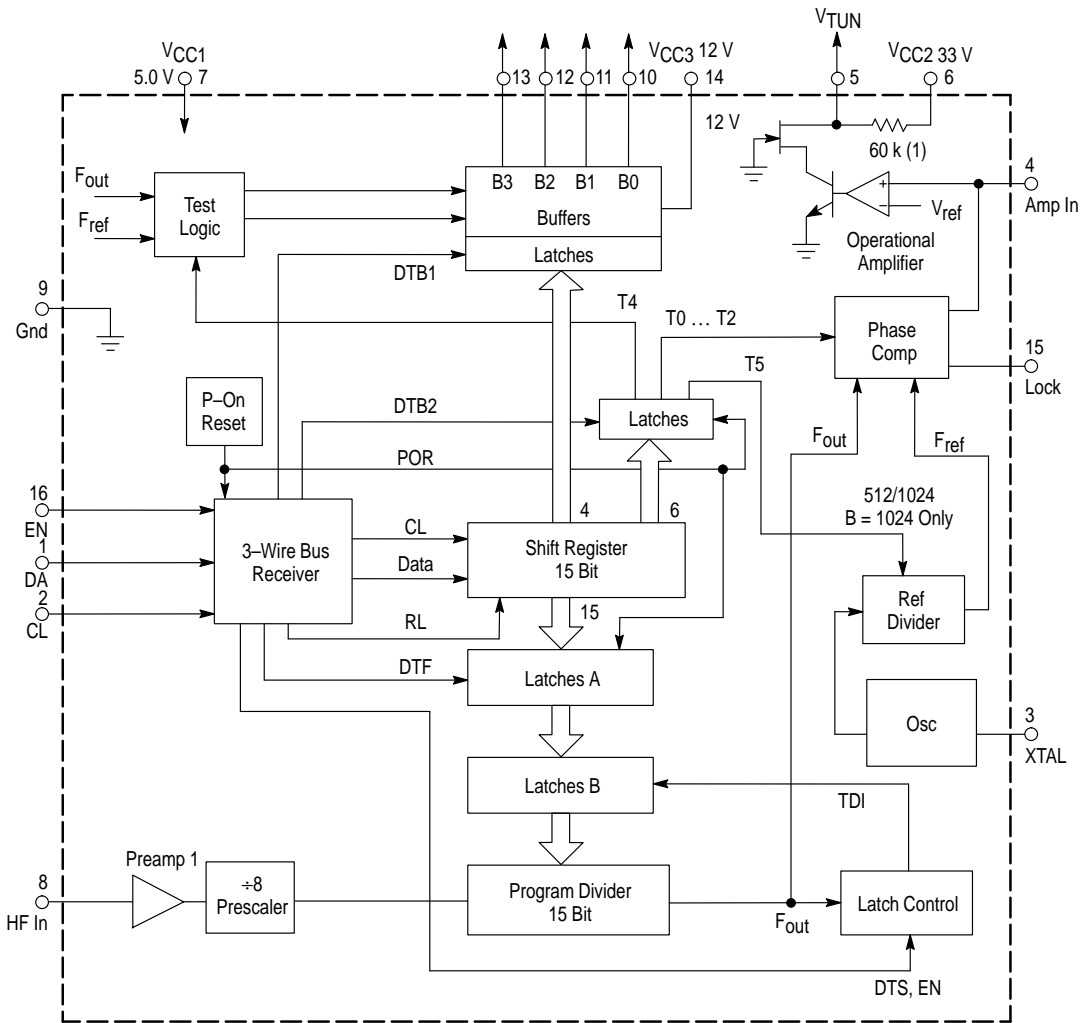
### PIN CONNECTIONS



(Top View)

# MC44827/27B

Figure 1. Representative Block Diagram



This device contains 3,204 active transistors.

**NOTE:** 1. This part may be used with an external pull-up resistor of 20 kΩ to remain compatible with MC44817/17B designed tuners. Pin 6 is left open. The internal pull-up can also be used with an external resistor in parallel.

## MAXIMUM RATINGS (T<sub>A</sub> = 25°C, unless otherwise noted.)

| Rating   | Pin   | Value            | Unit             |
|--|-------|------------------|------------------|
| Power Supply Voltage (V <sub>CC1</sub> )   | 7     | 6.0              | V                |
| Band Buffer "Off" Voltage  | 10-13 | 14.4             | V                |
| Band Buffer "On" Current   | 10-13 | 50               | mA               |
| Band Buffer Pin Shorted to Ground or V <sub>CC3</sub> (Short Circuit Duration) (Note 1)  | 10-13 | Continuous       | -                |
| Operational Amplifier Power Supply Voltage (V <sub>CC2</sub> )                           | 6     | 40               | V                |
| Operational Amplifier Pin Shorted to Ground or V <sub>CC2</sub> (Short Circuit Duration) | 5     | Continuous       | -                |
| Power Supply Voltage (V <sub>CC3</sub> )   | 14    | 14.4             | V                |
| Storage Temperature  | -     | -65 to +150      | °C               |
| Operating Temperature Range  | -     | -20 to +80       | °C               |
| Band Buffer Operation (Note 2) at 50 mA each Buffer All Buffers "On" Simultaneously      | 10-13 | 10               | s                |
| Operational Amplifier Output Voltage   | 5     | V <sub>CC2</sub> | V                |
| RF Input Level (80 MHz to 1.3 GHz)   | 8     | 1.5              | V <sub>rms</sub> |

**NOTES:** 1. At V<sub>CC3</sub> = V<sub>CC1</sub> to 14.4 V and T<sub>A</sub> = -20° to +80°C one buffer "On" only.  
 2. At V<sub>CC3</sub> = V<sub>CC1</sub> to 14.4 V and T<sub>A</sub> = -20° to +80°C.  
 3. ESD data available upon request.

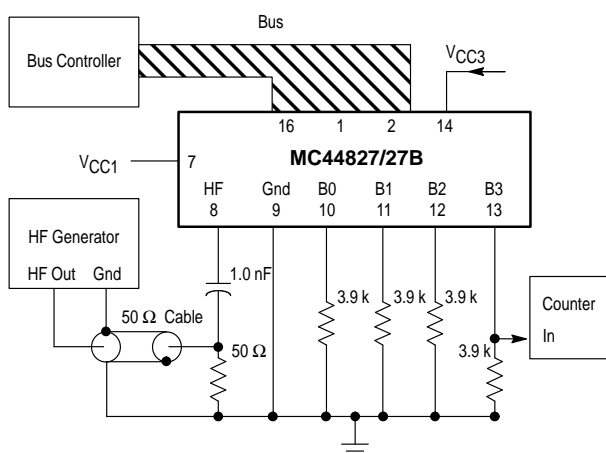
## MC44827/27B

**ELECTRICAL CHARACTERISTICS** (Parameter Type: A–100% Tested, B–100% Correlation Tested, C–Characterized on Samples, D–Design Parameter.  $V_{CC1} = 5.0\text{ V}$ ;  $V_{CC2} = 33\text{ V}$ ;  $V_{CC3} = 12\text{ V}$ ;  $T_A = 25^\circ\text{C}$ , unless otherwise noted.)

| Characteristic  | Pin      | Min       | Typ  | Max  | Unit          | Type |
|---|----------|-----------|------|------|---------------|------|
| $V_{CC1}$ Supply Voltage Range  | 7        | 4.5       | 5.0  | 5.5  | V             | A    |
| $V_{CC2}$ Supply Voltage Range  | 6        | 25        | 32   | 37   | V             | A    |
| $V_{CC3}$ Supply Voltage Range  | 14       | $V_{CC1}$ | 12   | 14.4 | V             | A    |
| $V_{CC1}$ Supply Current ( $V_{CC1} = 5.0\text{ V}$ ; $V_{CC3} = 12\text{ V}$ ) One Buffer "On" | 7        | –         | 23   | 30   | mA            | A    |
| $V_{CC2}$ Supply Current (Output Open) $V_{TUN} = 15\text{ V}$                                  | 6        | –         | 0.3  | 1.0  | mA            | A    |
| $V_{CC3}$ Supply Current<br>All Buffers "Off"   | 14       | –         | 0.15 | 0.3  | mA            | A    |
| One Buffer "On" when Open   |          | –         | 6.5  | 8.0  |               |      |
| One Buffer "On" at 40 mA  |          | –         | 46.5 | 50   |               |      |
| Band Buffer Leakage Current when "Off" at 12 V  | 10–13    | –         | 0.01 | 1.0  | $\mu\text{A}$ | A    |
| Band Buffer Saturation Voltage when "On" at 30 mA   | 10–13    | –         | 0.15 | 0.3  | V             | B    |
| Band Buffer Saturation Voltage when "On" at 40 mA   | 10–13    | –         | 0.2  | 0.5  | V             | A    |
| Data/Clock/Enable Current at 0 V  | 1, 2, 16 | –10       | –    | 0    | $\mu\text{A}$ | A    |
| Data/Clock/Enable Current at 5.0 V  | 1, 2, 16 | 0         | –    | 1.0  | $\mu\text{A}$ | A    |
| Data/Clock/Enable Input Voltage Low   | 1, 2, 16 | –         | –    | 1.5  | V             | A    |
| Data/Clock/Enable Input Voltage High  | 1, 2, 16 | 3.0       | –    | –    | V             | A    |
| Clock Frequency Range   | 2        | –         | –    | 100  | kHz           | D    |
| Oscillator Frequency Range  | 3        | 3.15      | 3.2  | 4.05 | MHz           | D    |
| Operational Amplifier Internal Reference Voltage  | –        | 1.8       | 2.75 | 3.5  | V             | A    |
| Operational Amplifier Input Current   | 4        | –15       | 0    | 15   | nA            | A    |
| DC Open Loop Gain   | –        | 100       | 250  | –    | –             | B    |
| Gain Bandwidth Product ( $CL = 1.0\text{ nF}$ )   | –        | 0.3       | –    | –    | MHz           | C    |
| $V_{out}$ Low, Sinking $50\text{ }\mu\text{A}$ (Note 1)   | 5        | –         | 80   | 200  | mV            | A    |
| $V_{out}$ High, Sourcing $3.0\text{ }\mu\text{A}$ , $V_{CC2} - V_{out}$                         | 5        | –         | 0.2  | 0.5  | V             | B    |
| Phase Comparator 3–State Current  | 4        | –15       | 0    | 15   | nA            | A    |
| Charge Pump High Current of Phase Comparator  | 4        | 30        | 50   | 85   | $\mu\text{A}$ | A    |
| Charge Pump Low Current of Phase Comparator   | 4        | 10        | 15   | 30   | $\mu\text{A}$ | A    |

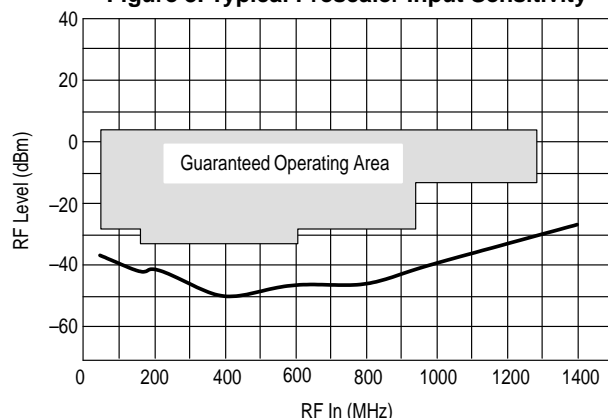
**NOTE:** 1. Using the internal  $60\text{ k}\Omega$  pull-up resistor only.

**Figure 2. HF (Prescaler Input) Sensitivity Test Circuit**



**NOTES:** 1. Device is in test mode. B2, B3 are "On" and B0, B1 are "Off".  
2. Sensitivity is level of HF generator on  $50\text{ }\Omega$  load.

**Figure 3. Typical Prescaler Input Sensitivity**

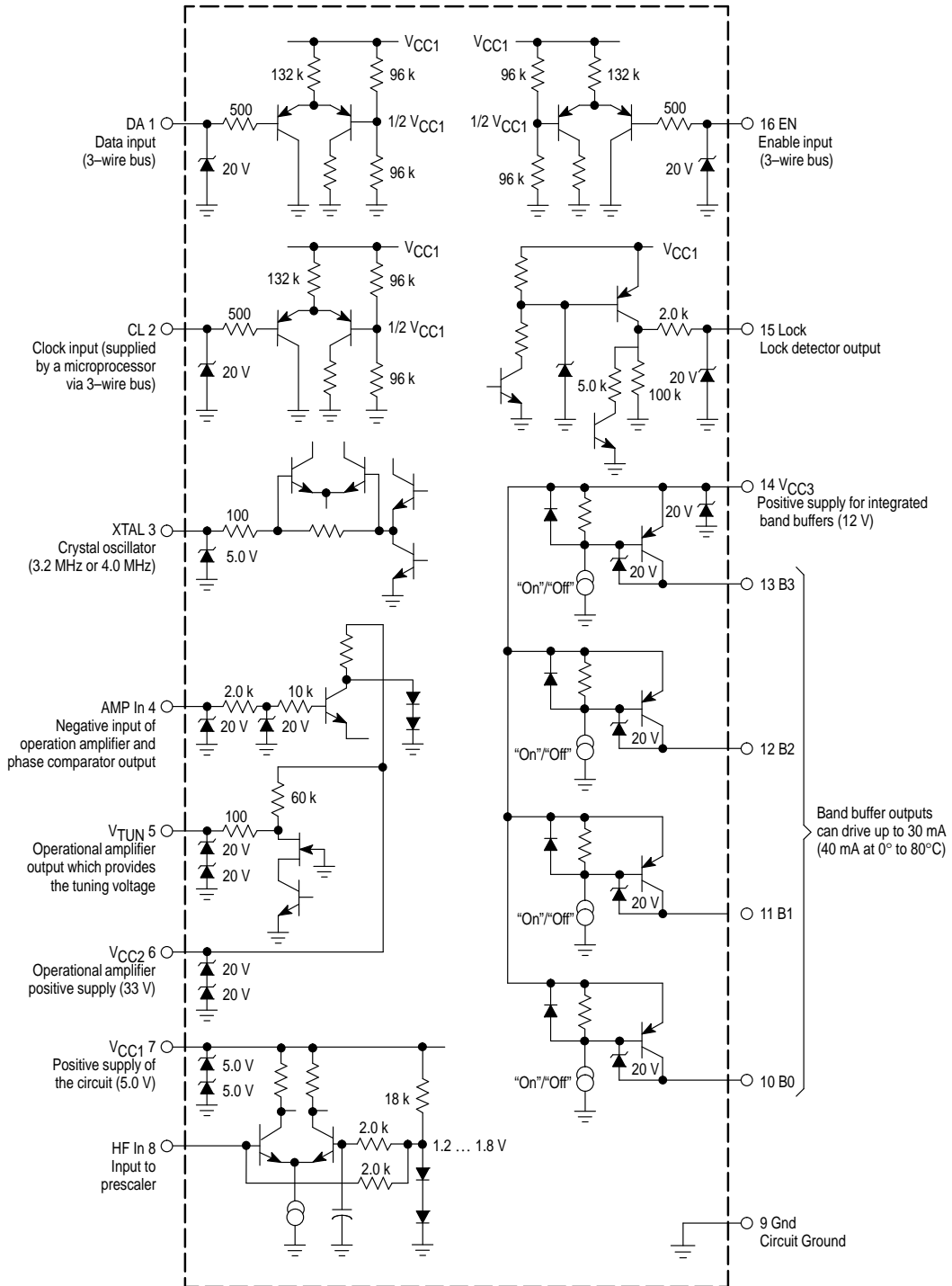


# MC44827/27B

HF INPUT SENSITIVITY AND OVERLOAD CHARACTERISTICS ( $V_{CC1} = 5.0\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .) (See Figure 2.)

| Frequency Range | Pin | Min | Typ | Max | Unit  | Type |
|-----------------|-----|-----|-----|-----|-------|------|
| DC Bias         | 8   | —   | 1.6 | —   | V     | A    |
| 80–150 MHz      | 8   | 10  | —   | 315 | mVrms | C    |
| 150–600 MHz     | 8   | 5.0 | —   | 315 | mVrms | C    |
| 600–950 MHz     | 8   | 10  | —   | 315 | mVrms | C    |
| 950–1300 MHz    | 8   | 50  | —   | 315 | mVrms | C    |

Figure 4. Pin Circuit Schematic



# MC44827/27B

## PIN FUNCTION DESCRIPTION

| Pin         | Symbol                           | Description  |
|-------------|----------------------------------|--|
| 1           | DA                               | 3-wire bus data input  |
| 2           | CL                               | 3-wire bus clock input   |
| 3           | XTAL                             | Crystal oscillator (3.2 MHz or 4 MHz)                            |
| 4           | Amp In                           | Negative operational amplifier input and phase comparator output |
| 5           | V <sub>TUN</sub>                 | Operational amplifier output which provides the tuning voltage   |
| 6           | V <sub>CC2</sub>                 | Operational amplifier positive supply (33 V)                     |
| 7           | V <sub>CC1</sub>                 | Positive supply of the circuit (5 V)                             |
| 8           | HF In                            | Asymmetrical HF input  |
| 9           | Gnd                              | Ground   |
| 10,11,12,13 | B <sub>0</sub> to B <sub>3</sub> | PNP Band buffer outputs  |
| 14          | V <sub>CC3</sub>                 | Positive supply for integrated band buffers (12 V)               |
| 15          | Lock                             | Lock detector output   |
| 16          | EN                               | 3-wire bus enable input  |

### Data Format and Bus Receiver

The circuit is controlled by a 3-wire bus via Data (DA), Clock (CL), and Enable (EN) inputs. The Data and Clock inputs may be shared with other inputs on the I<sup>2</sup>C-Bus while the Enable is a separate signal. The circuit is compatible with 18 and 19 bit data transmission and also has a mode for 34 bit transmission for test and additional features.

The 3-wire bus receiver receives data for the internal shift register after the positive going edge of the EN-signal. The data is transmitted to the band buffers on the negative going edge of the clock pulse 4 (signal DTB1).

### 18 and 19 Bit Data Transmission

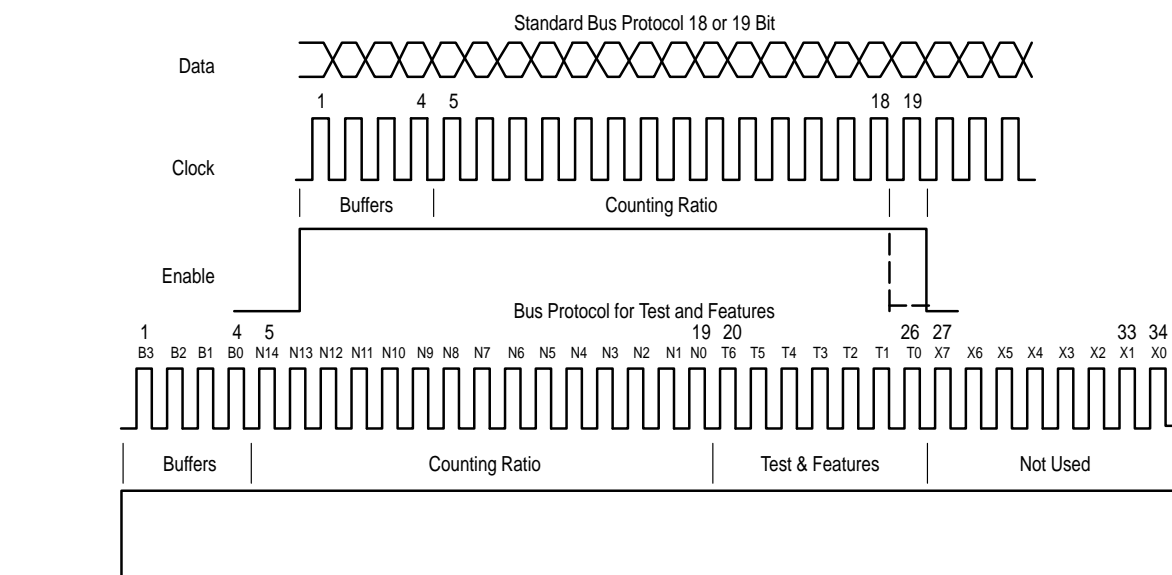
The programmable divider may receive a division ratio coded by a 14 bit (18 bit transmission) or 15 bit (19 bit transmission). The data is transmitted to the programmable divider (latches A) on the negative going edge of clock pulse 19 or on the negative edge of the EN-signal if EN goes down after the 18th clock pulse (signal DTF). If the programmable divider receives a 14 bit byte, its MSB (bit N14) is internally

reset. The reset pulse is generated only if EN goes negative after the 18th clock pulse (signal RL).

### 34 Bit Data Transmission (For Test and Additional Features)

In the test mode, the programmable divider receives a 15 bit byte and the data is transferred to latches A on the negative edge of clock pulse 19 (signal DTF). The information for test is received on clock pulses 20 to 26 and transmitted to the latches on the negative edge of pulse 34 (signal DTB2). These latches have a power-on reset. The power-on reset sets the programmable divider to a counting ratio of 256 or higher and resets the corresponding latches to the test bits T0 to T6 (signal POR). The bus receiver is not disturbed if the data format is wrong. Unused bits are ignored. If for example the Enable signal goes low after clock pulse 9, bits one to four are accepted as valid buffer information and the other bits are ignored. If more than 34 bits are received, bit 35 and the following are ignored.

Figure 5. Bus Timing Diagram



# MC44827/27B

## Definition of Permissible Bus Protocols

- Bus Protocol for 18 Bit  
 B3 B2 B1 B0 N13 N12 N11 N10 N9 N8 N7 N6 N5 N4 N3  
 N2 N1 N0  
 Max Counting Ratio 16363  
 N14 is Reset Internally
- Bus Protocol for 19 Bit  
 B3 B2 B1 B0 N14 N13 N12 N11 N10 N9 N8 N7 N6 N5 N4  
 N3 N2 N1 N0  
 Max Counting Ratio 32767  
 B0 to B3: Control of Band Buffers  
 N0 to N14: Programmable Divider Counting Ratio  
  
 N14 = MSB; N0 = LSB  
 Minimum Counting Ratio Always 17  
 B3 = First Shifted Bit  
 N0 = Last Shifted Bit
- Bus Protocol for Test and Further Features (34 Bit)  
 B3 B2 B1 B0 N14...N0 Y6 T5 T4 Y3 T2 T1 T0 X7  
 X6...X1 X0  
 T0 to T2: Control the Phase Comparator (Note 1)  
 T4: Switches Test Signals to the Buffer Outputs  
 T5: Division Ratio of the Reference Divider  
 B Version T5 = "X"  
 - X0 to X7: Are Random  
 - Y3 and Y6: Are Not Used  
  
 B3 = First Shifted Bit  
 X0 = Last Shifted Bit

## Definition of the Bits for Test and Features

### Bit T0: Defines the Charge Pump Current of the Phase Comparator

|        |                                 |
|--------|---------------------------------|
| T0 = 0 | Pump Current 50 $\mu$ A Typical |
| = 1    | Pump Current 15 $\mu$ A Typical |

### Bits T1 and T2: Define the Digital Function of the Phase Comparator

| T2 | T1 | State | Output Function of Phase Comparator   |
|----|----|-------|---------------------------------------|
| 0  | 0  | 1     | Normal Operation                      |
| 0  | 1  | 2     | High Impedance (3-State)              |
| 1  | 0  | 3     | Upper Source "On", Lower Source "Off" |
| 1  | 1  | 4     | Lower Source "On", Upper Source "Off" |

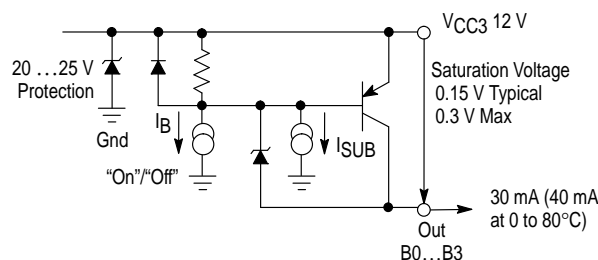
**NOTE:** 1. The phase comparator pulls high if the input frequency is too high and it pulls low when the input frequency is too low. (Inversion by Operational Amplifier) The phase comparator generates a fixed duration offset pulse for each comparison pulse. This guarantees operation in the linear region. The offset pulse is a positive current pulse (upper source).

### Bit T4: Switches the Internal Frequencies $F_{ref}$ and $FBY2$ to the Buffer Outputs (B2, B3)

|        |   |
|--------|---|
| T4 = 0 | Normal Operation  |
| = 1    | $F_{ref}$ Switched to Buffer Output B2<br>$FBY2$ Switched to Buffer Output B3 |

**NOTE:** Bits B2 and B3 have to be one in this case.  $F_{ref}$  is the reference frequency.  $FBY2$  is the output frequency of the programmable divider, divided by two.

Figure 6. Equivalent Circuit of the Integrated Band Buffers



**NOTES:**  $I_B + I_{SUB} = 5.5$  mA Typical  
 $I_B$  = Base Current  
 $I_{SUB}$  = Substrate Current of PNP

### Bit T5: Defines the Division Ratio of the Reference Divider

|        |                     |
|--------|---------------------|
| T5 = 0 | Division Ratio 512  |
| = 1    | Division Ratio 1024 |

**NOTE:** The division ratio of the reference divider can only be programmed in the 34 bit bus protocol. In the standard bus protocol the division ratio is 512. (The power-up reset POR sets the division ratio to 512). On "B-version", T5 = "X". Division ratio 1024 is fixed.

## OPERATING DESCRIPTION

### Introduction

A representative block diagram and typical system application are shown in Figures 1 and 8. A discussion of the features and function of each of the internal blocks is given.

### The Programmable Divider

The programmable divider is a presettable down counter. When it has counted to zero it takes its required division ratio out of the latches B. Latches B are loaded from latches A by means of signal TDI which is synchronous to the programmable divider output signal.

Since latches A receive the data asynchronously with the programmable divider; this double latch scheme is needed to assure correct data transfer to the counter.

The division ratio definition is given by:  
 $N = 16384 \times N14 + 8132 \times N13 + \dots + 4 \times N2 + 2 \times N1 + N0$   
 Maximum Ratio 32767  
 (16363 in case of 18 bit bus protocol)  
 Minimum Ratio 17

N0 ... N14 are the different bits for frequency information. At power-on the whole bus receiver is reset and the programmable divider is set to a counting ratio of  $N = 256$  or higher.

### The Prescaler

The divide by 8 prescaler has a preamplifier which guarantees high input sensitivity.

### The Phase Comparator

The phase comparator is both phase and frequency sensitive and has very low output leakage current in the high impedance state.

### Lock Detector

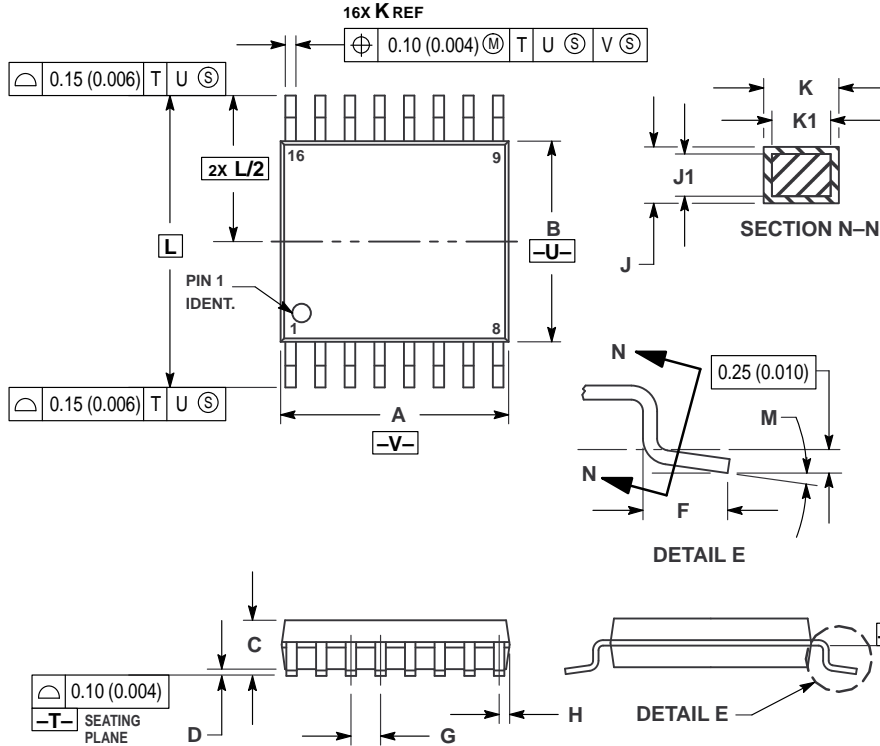
The lock-detector output is low in lock. The output goes immediately high when an unlock condition is detected. The output goes low again when the loop is in lock during a complete period of the reference frequency.



# MC44827/27B

## OUTLINE DIMENSIONS

DTB SUFFIX  
PLASTIC PACKAGE  
CASE 948F-01  
(TSSOP-16)  
ISSUE 0



NOTES:

- 1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION: MILLIMETER.
- 3 DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- 4 DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- 5 DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- 6 TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- 7 DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS        |      | INCHES    |       |
|-----|--------------------|------|-----------|-------|
|     | MIN                | MAX  | MIN       | MAX   |
| A   | 4.90               | 5.10 | 0.193     | 0.200 |
| B   | 4.30               | 4.50 | 0.169     | 0.177 |
| C   | —                  | 1.20 | —         | 0.047 |
| D   | 0.05               | 0.15 | 0.002     | 0.006 |
| F   | 0.50               | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC 0.026 BSC |      |           |       |
| H   | 0.18               | 0.28 | 0.007     | 0.011 |
| J   | 0.09               | 0.20 | 0.004     | 0.008 |
| J1  | 0.09               | 0.16 | 0.004     | 0.006 |
| K   | 0.19               | 0.30 | 0.007     | 0.012 |
| K1  | 0.19               | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC           |      | 0.252 BSC |       |
| M   | 0°                 | 8°   | 0°        | 8°    |

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