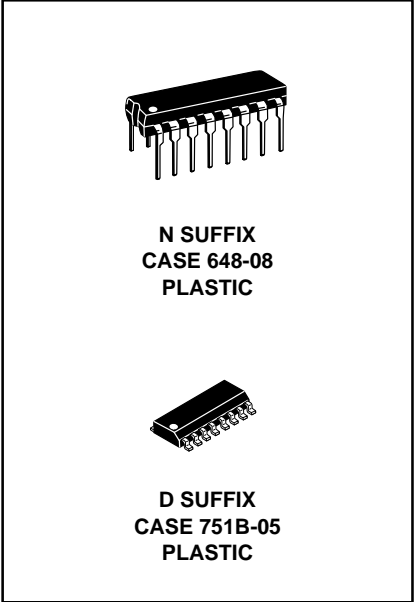




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14-STAGE BINARY RIPPLE COUNTER

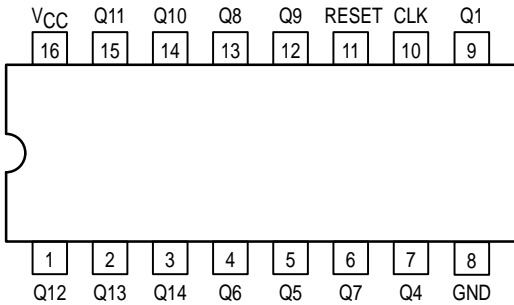


14-Stage Binary Ripple Counter

The MC74AC4020 consists of 14 master-slave flip-flops with 12 stages brought out to pins. The output of each flip-flop feeds the next and the frequency at each output is half that of the preceding one. The state of the counter advances on the negative-going edge of the Clock input. Reset is asynchronous and active-high.

State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and may have to be gated with the Clock of the MC74AC4020 for some designs.

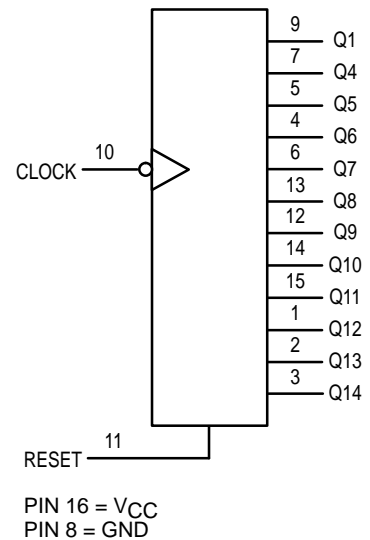
- 140 MHz Typ. Clock
- Outputs Source/Sink 24 mA
- Operating Voltage Range: 2.0 to 6.0 V
- High Noise Immunity



FUNCTION TABLE

| Clock | Reset | Output State |
|-------|-------|-----------------------|
| | L | No Change |
| | L | Advance to next state |
| X | H | All Outputs are low |

LOGIC DIAGRAM



MC74AC4020

MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|-----------|--|------------------------|-------------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | -0.5 to +7.0 | V |
| V_{in} | DC Input Voltage (Referenced to GND) | -0.5 to $V_{CC} + 0.5$ | V |
| V_{out} | DC Output Voltage (Referenced to GND) | -0.5 to $V_{CC} + 0.5$ | V |
| I_{in} | DC Input Current, per Pin | ± 20 | mA |
| I_{out} | DC Output Current, per Pin | ± 50 | mA |
| I_{CC} | DC V_{CC} or GND Current per Output Pin | ± 50 | mA |
| P_D | Power Dissipation in Still Air Plastic** SOIC Package** | 750 500 | mW |
| T_{stg} | Storage Temperature | -65 to +150 | $^{\circ}C$ |
| T_L | Lead Temperature, 1 mm from Case for 10 seconds (Plastic DIP or SOIC Package) | 260 | $^{\circ}C$ |

* Maximum Ratings are those values beyond which damage to the device may occur.

** Derating: Plastic DIP: - 10mW/ $^{\circ}C$ from 65 $^{\circ}C$ to 125 $^{\circ}C$
SOIC Package: -7.0 mW/ $^{\circ}C$ from 65 $^{\circ}C$ to 125 $^{\circ}C$

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|------------------|---|-----|----------|-------------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | 2.0 | 6.0 | V |
| V_{in}/V_{out} | Input Voltage, Output Voltage (Ref. to GND) | 0 | V_{CC} | |
| T_A | Operating Temperature, All Package Types | -40 | +85 | $^{\circ}C$ |
| t_r/t_f | Input Rise/Fall Time (Figure 1) | | | ns/V |
| | $V_{CC} = 3.0 V$ | 0 | 150 | |
| | $V_{CC} = 4.5 V$ | 0 | 40 | |
| | $V_{CC} = 5.5 V$ | 0 | 25 | |

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DC CHARACTERISTICS (unless otherwise specified)

| Symbol | Parameter | Value | Unit | |
|-----------------|----------------------------------|-------|------|---|
| I _{CC} | Maximum Quiescent Supply Voltage | 80 | μA | V _{in} = V _{CC} or GND V _{CC} = 5.5 V, T _A = Worst Case |
| I _{CC} | Maximum Quiescent Supply Current | 8.0 | μA | V _{in} = V _{CC} or GND V _{CC} = 5.5 V, T _A = 25°C |

DC CHARACTERISTICS

| Symbol | Parameter | V _{CC} (V) | 74AC | | Unit | Conditions |
|------------------|-----------------------------------|------------------------|------------------------|-------------------|------|--|
| | | | T _A = +25°C | | | |
| | | | Typ | Guaranteed Limits | | |
| V _{IH} | Minimum High Level Input Voltage | 3.0 | | 2.1 | 2.1 | V V _{OUT} = 0.1 V or V _{CC} - 0.1 V |
| | | 4.5 | | 3.15 | 3.15 | |
| | | 5.5 | | 3.85 | 3.85 | |
| V _{IL} | Maximum Low Level Input Voltage | 3.0 | | 0.9 | 0.9 | V V _{OUT} = 0.1 V or V _{CC} - 0.1 V |
| | | 4.5 | | 1.35 | 1.35 | |
| | | 5.5 | | 1.65 | 1.65 | |
| V _{OH} | Minimum High Level Output Voltage | 3.0 | 2.99 | 2.9 | 2.9 | V I _{OUT} = -50 μA |
| | | 4.5 | 4.49 | 4.4 | 4.4 | |
| | | 5.5 | 5.49 | 5.4 | 5.4 | |
| | | 3.0 | | 2.56 | 2.46 | V *V _{IN} = V _{IL} or V _{IH} -12 mA I _{OH} -24 mA -24 mA |
| | | 4.5 | | 3.86 | 3.76 | |
| | | 5.5 | | 4.86 | 4.76 | |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 | 0.002 | 0.1 | 0.1 | V I _{OUT} = 50 μA |
| | | 4.5 | 0.001 | 0.1 | 0.1 | |
| | | 5.5 | 0.001 | 0.1 | 0.1 | |
| | | 3.0 | | 0.36 | 0.44 | V *V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA |
| | | 4.5 | | 0.36 | 0.44 | |
| | | 5.5 | | 0.36 | 0.44 | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | μA V _I = V _{CC} , GND |
| I _{OLD} | Minimum Dynamic Output Current** | 5.5 | | | 75 | mA V _{OLD} = 1.65 V Max |
| I _{OHD} | | 5.5 | | | -75 | mA V _{OHD} = 3.85 V Min |

* All outputs loaded; thresholds on input associated with output under test.

** Maximum test duration 2.0 ms, one output loaded at a time.

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

| Symbol | Parameter | V _{CC} * (V) | 74AC | | | 74AC | | Unit | Fig. No. |
|------------------------------|--|-----------------------|--|--------------|------------|--|------------|------|----------|
| | | | T _A = +25°C C _L = 50 pF | | | T _A = -40°C to +85°C C _L = 50 pF | | | |
| | | | Min | Typ | Max | Min | Max | | |
| f _{max} | Maximum Clock Frequency | 3.3 5.0 | 110 130 | 0 140 | | 100 120 | | MHz | |
| t _{PLH} | Propagation Delay CP to Q1 | 3.3 5.0 | 2.0 2.0 | | 11 8.0 | 2.0 2.0 | 14 10 | ns | |
| t _{PHL} | Propagation Delay CP to Q1 | 3.3 5.0 | 2.0 2.0 | | 11 8.0 | 2.0 2.0 | 14 10 | ns | |
| t _{PLH} | Propagation Delay CP to Q4 | 3.3 5.0 | 2.0 2.0 | | 18 13 | 2.0 2.0 | 21 16 | ns | |
| t _{PHL} | Propagation Delay CP to Q4 | 3.3 5.0 | 2.0 2.0 | | 18 13 | 2.0 2.0 | 21 16 | ns | |
| t _{PHL} | Propagation Delay Reset to any Q | 3.3 5.0 | 3.0 3.0 | | 12 10 | 3.0 3.0 | 15 12 | ns | |
| t _{PHL} | Propagation Delay O _n to Q _n +1 | 3.3 5.0 | 0 0 | | 5.5 3.5 | 0 0 | 6.5 4.5 | ns | |
| t _{PHL} | Propagation Delay O _n to Q _n +1 | 3.3 5.0 | 0 0 | | 5.5 3.5 | 0 0 | 6.5 4.5 | ns | |
| t _{rec} MR to CP | Recovery Time | 3.3 5.0 | 0 0 | -2.5 -1.5 | | 0 0 | | ns | |
| t _w CP | Minimum Pulse Width Clock Pin | 3.3 5.0 | 4.0 3.0 | 3.5 2.5 | | 4.5 3.5 | | ns | |
| t _w MR | Minimum Pulse Width Master Reset | 3.3 5.0 | 4.0 3.0 | 3.5 2.5 | | 4.5 3.5 | | ns | |

* Voltage Range 3.3 V is 3.3 V ±0.3 V.
Voltage Range 5.0 V is 5.0 V ±0.5 V.

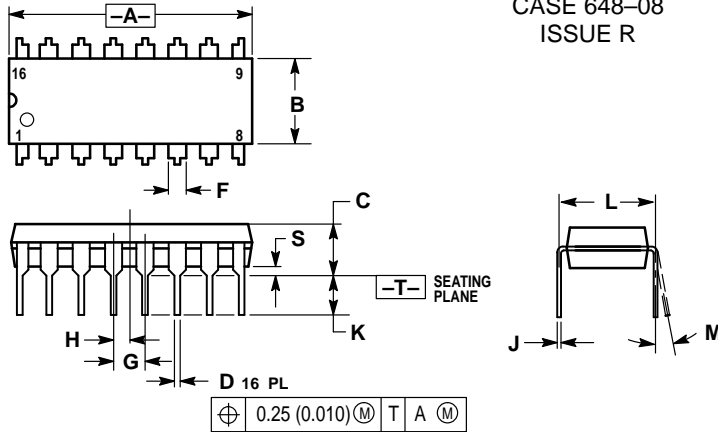
CAPACITANCE

| Symbol | Parameter | Value Typ | Unit | Test Conditions |
|-----------------|-------------------------------|--------------|------|-------------------------|
| C _{IN} | Input Capacitance | 4.5 | pF | V _{CC} = 5.0 V |
| CPD | Power Dissipation Capacitance | 50 | pF | V _{CC} = 5.0 V |

MC74AC4020

OUTLINE DIMENSIONS

N SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R

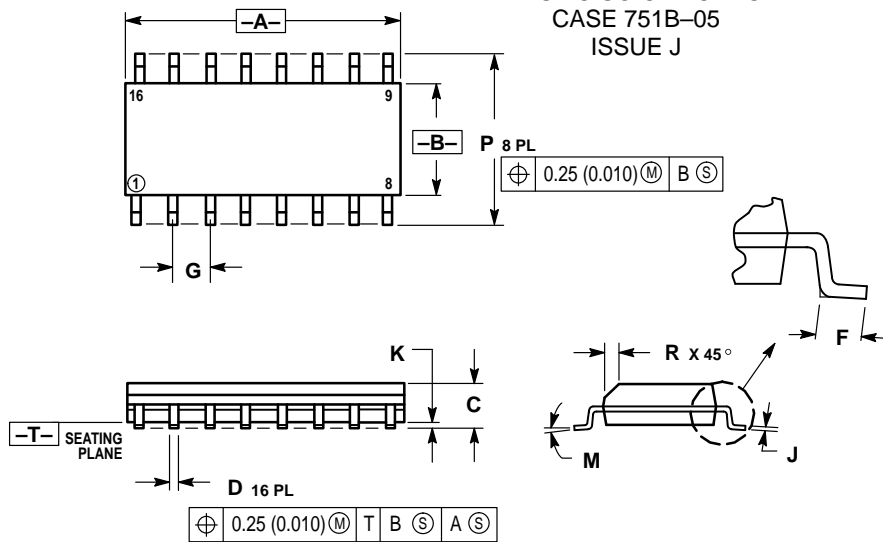


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.740 | 0.770 | 18.80 | 19.55 |
| B | 0.250 | 0.270 | 6.35 | 6.85 |
| C | 0.145 | 0.175 | 3.69 | 4.44 |
| D | 0.015 | 0.021 | 0.39 | 0.53 |
| F | 0.040 | 0.70 | 1.02 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.050 BSC | | 1.27 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.130 | 2.80 | 3.30 |
| L | 0.295 | 0.305 | 7.50 | 7.74 |
| M | 0° | 10° | 0° | 10° |
| S | 0.020 | 0.040 | 0.51 | 1.01 |


D SUFFIX PLASTIC SOIC PACKAGE CASE 751B-05 ISSUE J



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

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