MC54/74HCT14A

Hex Schmitt-Trigger Inverter with LSTTL Compatible Inputs

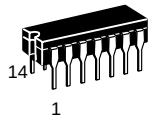
High–Performance Silicon–Gate CMOS

The MC54/74HCT14A may be used as a level converter for interfacing TTL or NMOS outputs to high–speed CMOS inputs.

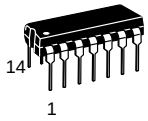
The HCT14A is identical in pinout to the LS14.

The HCT14A is useful to “square up” slow input rise and fall times. Due to the hysteresis voltage of the Schmitt trigger, the HCT14A finds applications in noisy environments.

- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS–Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 72 FETs or 18 Equivalent Gates



J SUFFIX
CERAMIC PACKAGE
CASE 632–08



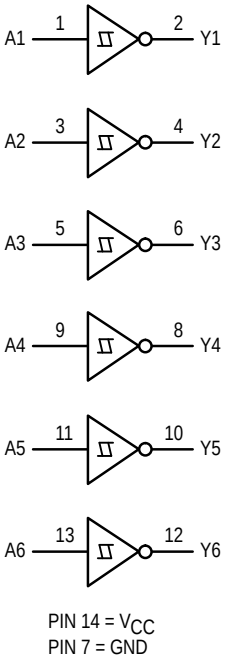
N SUFFIX
PLASTIC PACKAGE
CASE 646–06

D SUFFIX
SOIC PACKAGE
CASE 751A–03

ORDERING INFORMATION

MC54HCTXXAJ	Ceramic
MC74HCTXXAN	Plastic
MC74HCTXXAD	SOIC

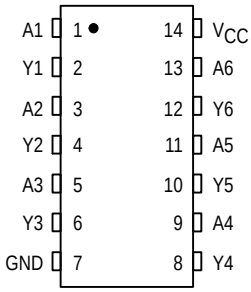
LOGIC DIAGRAM



$Y = \overline{A}$

PIN 14 = V_{CC}
PIN 7 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Input A	Output Y
L	H
H	L

MOTOROLA

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 1.5 to V_{CC} + 1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	 260 300	°C °C

* Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
Ceramic DIP: – 10 mW/°C from 100° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	*	ns

* No Limit when V_{in} ≈ 50% V_{CC}, I_{CC} > 1 mA.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} Volts	Temperature Limit						Unit
				– 55 to 25°C		≤ 85°C		≤ 125°C		
				Min	Max	Min	Max	Min	Max	
V_{T+} max	Maximum Positive–Going Input Threshold Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	4.5 5.5		1.9 2.1		1.9 2.1		1.9 2.1	V
V_{T+} min	Minimum Positive–Going Input Threshold Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	1.2 1.4		1.2 1.4		1.2 1.4		V
$V_{T–}$ max	Maximum Positive–Going Input Threshold Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	4.5 5.5		1.2 1.4		1.2 1.4		1.2 1.4	
$V_{T–}$ min	Minimum Positive–Going Input Threshold Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	0.5 0.6		0.5 0.6		0.5 0.6		
V_H max	Maximum Hysteresis Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	4.5 5.5		1.4 1.5		1.4 1.5		1.4 1.5	
V_H min	Minimum Hysteresis Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	0.4 0.4		0.4 0.4		0.4 0 4		
V_{OH}	Minimum High–Level Output Voltage	V_{in} < VT–min $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	4.4 5.4		4.4 5.4		4.4 5.4		V
		V_{in} < VT–min $\|I_{out}\|$ ≤ 4.0 mA	4.5	3.98		3.84		3.7		

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

(continued)

DC CHARACTERISTICS (Voltages Referenced to GND) **– continued**

Symbol	Parameter	Test Conditions	V_{CC} Volts	Temperature Limit: – 55 to 25°C Min	– 55 to 25°C Max	≤ 85°C Min	≤ 85°C Max	≤ 125°C Min	≤ 125°C Max	Unit
V_{OL}	Maximum Low–Level Output Voltage	V_{in} < VT–min $\|I_{out}\| \leq 20$ μA	4.5 5.5		0.1 0.1		0.1 0.1		0.1 0.1	V
		V_{in} < VT–min $\|I_{out}\| \leq 4.0$ mA	4.5		0.26		0.33		0.4	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	5.5		± 0.1		± 1.0		± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per package)	$V_{in} = V_{CC}$ or GND I_{out} = 0 μA	5.5		1.0		10		40	μA
					≥ – 55°C		25°C to 125°C			
ΔI_{CC}	Additional Quiescent Supply Current	V_{in} = 2.4 V, Any One Input $V_{in} = V_{CC}$ or GND, Other Inputs I_{out} = 0 μA	5.5		2.9		2.4			mA

AC CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	Test Conditions		Guaranteed Limit: – 55 to 25°C Min	– 55 to 25°C Max	≤ 85°C Min	≤ 85°C Max	≤ 125°C Min	≤ 125°C Max	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A to Output Y (L to H)	V_{CC} = 5.0 V ± 10% C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns	Fig. 1 & 2		32		40		48	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time. Any Output	V_{CC} = 5.0 V ± 10% C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns	Fig. 1 & 2		15		19		22	ns

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Inverter)*	32	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

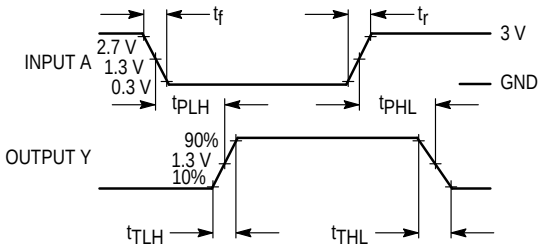
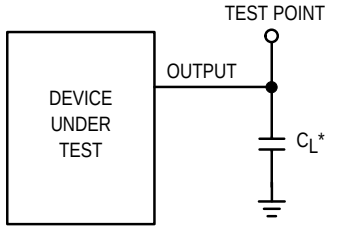


Figure 1. Switching Waveforms

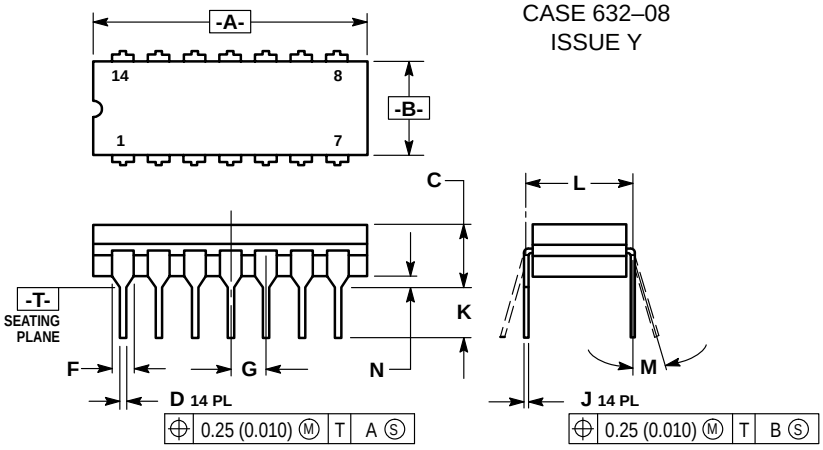


* Includes all probe and jig capacitance

Figure 2. Test Circuit

OUTLINE DIMENSIONS

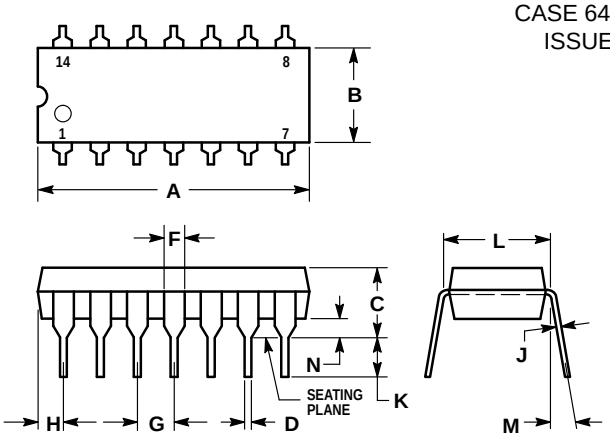
J SUFFIX
CERAMIC DIP PACKAGE
CASE 632–08
ISSUE Y



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMESNION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.94
B	0.245	0.280	6.23	7.11
C	0.155	0.200	3.94	5.08
D	0.015	0.020	0.39	0.50
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

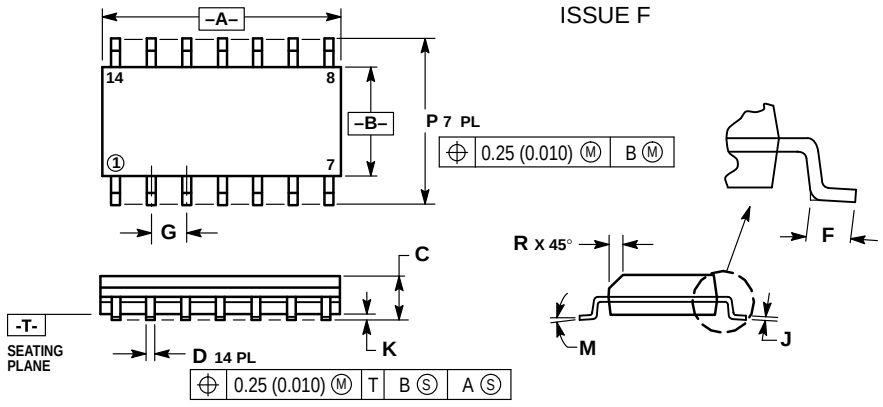
N SUFFIX
PLASTIC DIP PACKAGE
CASE 646–06
ISSUE L



NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751A–03
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

How to reach us:
USA/EUROPE: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447

MFAX: RMFAX0@email.sps.mot.com –TOUCHTONE (602) 244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, Toshikatsu Otsuki,
6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–3521–8315

HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298

MOTOROLA

◊ CODELINE

MC54/74HCT14A/D