MOTOROLA

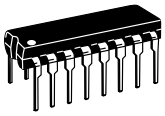
MC74AC160
MC74ACT160
MC74AC162
MC74ACT162

Synchronous Presettable BCD Decade Counter

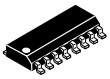
SYNCHRONOUS PRESETTABLE BCD DECADE COUNTER

The MC74AC160/74ACT160 and MC74AC162/74ACT162 are high-speed synchronous decade counters operating in the BCD (8421) sequence. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The MC74AC160/74ACT160 has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The MC74AC162/74ACT162 has a Synchronous Reset input that overrides counting and parallel loading and allows all outputs to be simultaneously reset on the rising edge of the clock.

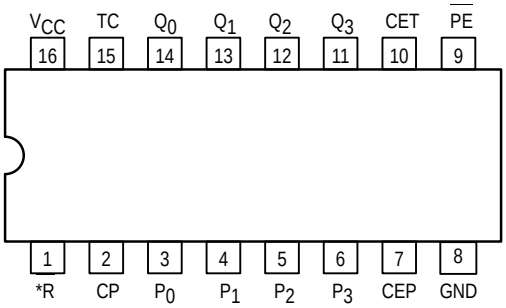
- Synchronous Counting and Loading
- High-Speed Synchronous Expansion
- Typical Count Rate of 120 MHz
- Outputs Source/Sink 24 mA
- ′ACT160 and ′ACT162 Have TTL Compatible Inputs



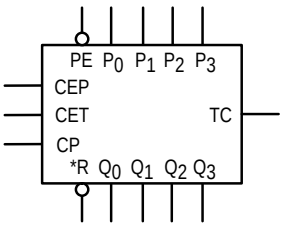
N SUFFIX
CASE 648-08
PLASTIC



D SUFFIX
CASE 751B-05
PLASTIC



LOGIC SYMBOL



*$\overline{MR}$ for ′160
*SR for ′162

PIN NAMES

CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
$\overline{CP}$	Clock Pulse Input
$\overline{MR}$	(′160) Asynchronous Master Reset Input
SR	(′162) Synchronous Reset Input
P_0–P_3	Parallel Data Inputs
PE	Parallel Enable Input
Q_0–Q_3	Flip-Flop Outputs
TC	Terminal Count Output

FUNCTIONAL DESCRIPTION

The MC74AC160/74ACT160 and MC74AC162/74ACT162 count modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the ′160) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset (′160), synchronous reset (′162), parallel load, count-up and hold. Five control inputs — Master Reset (MR, ′160), Synchronous Reset (SR,′162), Parallel Enable (PE), Count Enable Parallel (CEP) and Count Enable Trickle (CET) — determine the mode of operation, as shown in the Mode Select Table. A LOW signal on MR overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on SR overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on PE overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With PE and MR (′160) or SR (′162) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The MC74AC160/74ACT160 and MC74AC162/74ACT162 use D-type edge-triggered flip-flops and changing the SR, PE, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and counter is in state 9. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. Please refer to the MC74AC568 data sheet. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers. In the MC74AC160/74AC162 decade counters, the TC output is fully decoded and can only be HIGH in state 9. If a decade counter is preset to an illegal state, or assumes an illegal state when power is applied, it will return to the normal sequence within two counts, as shown in the State Diagram.

Logic Equations: Count Enable = CEP• CET• PE

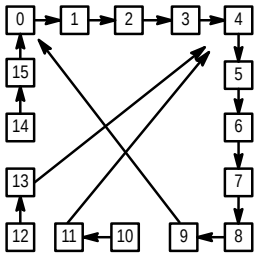
$TC = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet CET$

MODE SELECT TABLE

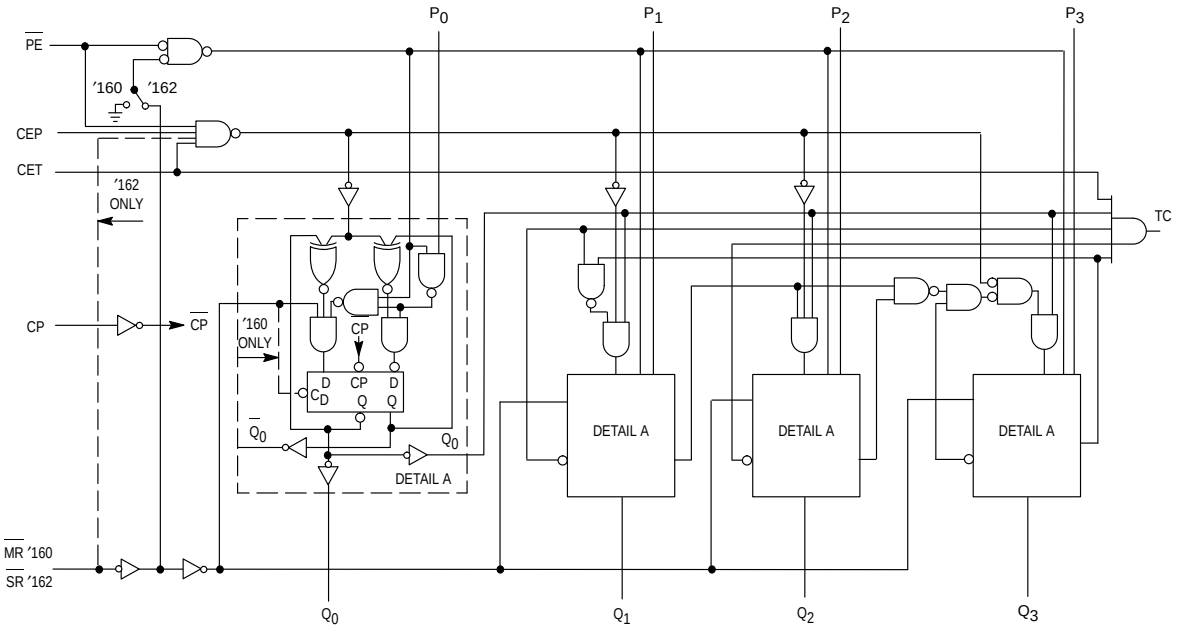
*$\overline{SR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge (⌐)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

*For ′162 only
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

STATE DIAGRAM



LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	–0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	–0.5 to V_{CC} +0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	–0.5 to V_{CC} +0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Sink/Source Current, per Pin	±50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	±50	mA
T_{stg}	Storage Temperature	–65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	′AC	2.0	5.0	6.0	V
		′ACT	4.5	5.0	5.5	
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Ref. to GND)		0		V_{CC}	V
t_r, t_f	Input Rise and Fall Time (Note 1) ′AC Devices except Schmitt Inputs	V_{CC} @ 3.0 V		150		ns/V
		V_{CC} @ 4.5 V		40		
		V_{CC} @ 5.5 V		25		
t_r, t_f	Input Rise and Fall Time (Note 2) ′ACT Devices except Schmitt Inputs	V_{CC} @ 4.5 V		10		ns/V
		V_{CC} @ 5.5 V		8.0		
T_J	Junction Temperature (PDIP)				140	°C
T_A	Operating Ambient Temperature Range		–40	25	85	°C
I_{OH}	Output Current — High				–24	mA
I_{OL}	Output Current — Low				24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C	74AC T_A = –40°C to +85°C		Unit	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V_{OUT} = 0.1 V or V_{CC} – 0.1 V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V_{OUT} = 0.1 V or V_{CC} – 0.1 V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = –50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} –12 mA
		4.5		3.86	3.76		I_{OH} –24 mA
		5.5		4.86	4.76		I_{OH} –24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.44		I_{OL} 24 mA
		5.5		0.36	0.44		I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V_I = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V_{OLD} = 1.65 V Max
I_{OHD}		5.5			–75	mA	V_{OHD} = 3.85 V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V_{IN} = V_{CC} or GND

* All outputs loaded; thresholds on input associated with output under test.
† Maximum test duration 2.0 ms, one output loaded at a time.
Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

MC74AC160

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC160 T_A = +25°C C_L = 50 pF		74AC160 T_A = –40°C to +85°C C_L = 50 pF		Unit	Fig. No.
			Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	3.3 5.0	65 110	— —	60 95	— —	MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n (PE Input HIGH)	3.3 5.0	2.0 1.5	12.0 9.0	1.5 1.0	14.0 10.5	ns	3-6
t_{PHL}	Propagation Delay CP to Q_n (PE Input HIGH)	3.3 5.0	2.0 1.5	12.0 9.0	1.5 1.5	14.0 10.5	ns	3-6
t_{PLH}	Propagation Delay CP to Q_n (PE Input LOW)	3.3 5.0	2.0 1.5	12.0 9.0	1.5 1.0	14.0 10.5	ns	3-6
t_{PHL}	Propagation Delay CP to Q_n (PE Input LOW)	3.3 5.0	2.0 1.5	12.0 9.0	1.5 1.5	14.0 10.5	ns	3-6
t_{PLH}	Propagation Delay CP to TC	3.3 5.0	3.0 2.0	15.0 11.0	2.5 1.5	17.5 12.5	ns	3-6
t_{PHL}	Propagation Delay CP to TC	3.3 5.0	3.5 2.0	14.5 11.0	2.5 2.0	16.5 12.5	ns	3-6
t_{PLH}	Propagation Delay CET to TC	3.3 5.0	2.0 1.5	10.5 7.5	1.5 1.0	12.5 9.0	ns	3-6
t_{PHL}	Propagation Delay CET to TC	3.3 5.0	2.5 2.0	11.5 9.0	2.0 1.5	13.5 10.5	ns	3-6
t_{PHL}	Propagation Delay MR to Q_n (′AC160)	3.3 5.0	2.0 1.5	12.0 9.5	1.5 1.0	13.5 10.0	ns	3-6
t_{PHL}	Propagation Delay MR to TC	3.3 5.0	3.5 2.5	15.0 12.0	3.0 2.0	17.0 13.5	ns	3-6

* Voltage Range 3.3 V is 3.3 V ±0.3 V.
Voltage Range 5.0 V is 5.0 V ±0.5 V.

MC74AC162

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC162 T_A = +25°C C_L = 50 pF			74AC162 T_A = –40°C to +85°C C_L = 50 pF		Unit	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Count Frequency	3.3 5.0	80 125			60 100		MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n (PE Input HIGH)	3.3 5.0	2.0 2.0		12.0 9.0	1.5 1.5	13.5 10.5	ns	3-6
t_{PHL}	Propagation Delay CP to Q_n (PE Input HIGH)	3.3 5.0	2.0 2.0		12.0 9.0	1.5 1.5	13.5 10.5	ns	3-6
t_{PLH}	Propagation Delay CP to Q_n (PE Input LOW)	3.3 5.0	2.0 2.0		12.0 9.0	1.5 1.5	13.5 10.5	ns	3-6
t_{PHL}	Propagation Delay CP to Q_n (PE Input LOW)	3.3 5.0	2.0 2.0		12.0 9.0	1.5 1.5	13.5 10.5	ns	3-6
t_{PLH}	Propagation Delay CP to TC	3.3 5.0	2.0 2.0		15.0 11.0	1.5 1.5	17.0 13.0	ns	3-6
t_{PHL}	Propagation Delay CP to TC	3.3 5.0	2.0 2.0		14.0 11.0	1.5 1.5	16.0 13.0	ns	3-6
t_{PLH}	Propagation Delay CET to TC	3.3 5.0	2.0 2.0		10.0 7.0	1.5 1.5	11.5 8.5	ns	3-6
t_{PHL}	Propagation Delay CET to TC	3.3 5.0	2.0 2.0		11.0 8.0	1.5 1.5	12.5 9.5	ns	3-6

*Voltage Range 3.3 V is 3.0 V ±0.3 V.
Voltage Range 5.0 V is 5.0 V ±0.5 V.

MC74AC160
AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC160 T_A = +25°C C_L = 50 pF Guaranteed	74AC160 T_A = –40°C to +85°C C_L = 50 pF Maximum	Unit	Fig. No.
t_s	Setup Time, HIGH or LOW P_n to CP	3.3 5.0	13.5 8.5	16.0 10.5	ns	3-9
t_h	Hold Time, HIGH or LOW P_n to CP	3.3 5.0	–1.0 0	– 0.5 0	ns	3-9
t_s	Setup Time, HIGH or LOW PE or SR to CP	3.3 5.0	11.5 7.5	14.0 8.5	ns	3-9
t_h	Hold Time, HIGH or LOW PE or SR to CP	3.3 5.0	0 0.5	0 1.0	ns	3-9
t_s	Setup Time, HIGH or LOW CEP or CET to CP	3.3 5.0	6.0 4.5	7.0 5.0	ns	3-9
t_h	Hold Time, HIGH or LOW CEP or CET to CP	3.3 5.0	0 0	0 0.5	ns	3-9
t_w	Clock Pulse Width (Load) HIGH or LOW	3.3 5.0	4.0 3.0	5.0 3.5	ns	3-6
t_w	Clock Pulse Width (Count) HIGH or LOW	3.3 5.0	7.0 4.5	7.5 5.5	ns	3-6
t_w	$\overline{MR}$ Pulse Width, LOW (′AC160)	3.3 5.0	5.5 4.5	7.5 6.0	ns	3-6
t_{rec}	Recovery Time MR to CP (′AC160)	3.3 5.0	– 0.5 0	0 0.5	ns	3-9

* Voltage Range 3.3 V is 3.3 V ±0.3 V.
Voltage Range 5.0 V is 5.0 V ±0.5 V.

MC74AC162

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC162 T_A = +25°C C_L = 50 pF		74AC162 T_A = –40°C to +85°C C_L = 50 pF	Unit	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW P_n to CP	3.3 5.0		8.0 5.0	9.0 6.0	ns	3-9
t_h	Hold Time, HIGH or LOW P_n to CP	3.3 5.0		0.5 0.5	1.0 1.0	ns	3-9
t_s	Setup Time, HIGH or LOW PE to CP	3.3 3.3		10.0 6.0	11.0 7.0	ns	3-9
t_h	Hold Time, HIGH or LOW PE to CP	3.3 5.0		0.5 0.5	1.0 1.0	ns	3-9
t_s	Setup Time, HIGH or LOW CEP or CET to CP	3.3 5.0		6.0 4.0	7.0 5.0	ns	3-9
t_h	Hold Time, HIGH or LOW CEP or CET to CP	3.3 5.0		0.5 0.5	1.0 1.0	ns	3-9
t_s	Setup Time, HIGH or LOW SR to CP	3.3 5.0		8.0 6.0	9.0 7.0	ns	3-9
t_h	Hold Time, HIGH or LOW SR to CP	3.3 5.0		0.5 0.5	1.0 1.0	ns	3-9
t_w	Clock Pulse Width (Load) HIGH or LOW	3.3 5.0		5.5 4.5	6.0 5.0	ns	3-6
t_w	Clock Pulse Width (Count) HIGH or LOW	3.3 5.0		5.0 4.0	5.5 4.5	ns	3-6

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
Voltage Range 5.0 V is 5.0 V ±0.5 V.

DC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	74ACT T_A = +25°C	74ACT T_A = –40°C to +85°C		Unit	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1 V or V_{CC} – 0.1 V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1 V or V_{CC} – 0.1 V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I_{OUT} = –50 μA
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} –24 mA I_{OH} –24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V_I = V_{CC}, GND
ΔI_{CCT}	Additional Max. I_{CC}/Input	5.5	0.6		1.5	mA	V_I = V_{CC} – 2.1 V
I_{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V_{OLD} = 1.65 V Max
I_{OHD}		5.5			–75	mA	V_{OHD} = 3.85 V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V_{IN} = V_{CC} or GND

* All outputs loaded; thresholds on input associated with output under test.
† Maximum test duration 2.0 ms, one output loaded at a time.

MC74ACT160
AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT160 T_A = +25°C C_L = 50 pF			74ACT160 T_A = −40°C to +85°C C_L = 50 pF		Unit	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Count Frequency	5.0	120			100		MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n (PE Input HIGH)	5.0	2.0	6.0	10.0	2.0	11.0	ns	3-6
t_{PHL}	Propagation Delay CP to Q_n (PE Input HIGH)	5.0	2.0	6.0	10.0	2.0	11.0	ns	3-6
t_{PLH}	Propagation Delay CP to Q_n (PE Input LOW)	5.0	2.0	6.0	10.0	2.0	11.0	ns	3-6
t_{PHL}	Propagation Delay CP to Q_n (PE Input LOW)	5.0	2.0	6.0	10.0	2.0	11.0	ns	3-6
t_{PLH}	Propagation Delay CP to TC	5.0	2.0	8.0	12.0	2.0	14.0	ns	3-6
t_{PHL}	Propagation Delay CP to TC	5.0	2.0	8.0	12.0	2.0	14.0	ns	3-6
t_{PLH}	Propagation Delay CET to TC	5.0	2.0	6.0	8.5	2.0	9.5	ns	3-6
t_{PHL}	Propagation Delay CET to TC	5.0	2.0	7.0	9.5	2.0	11.0	ns	3-6
t_{PHL}	Propagation Delay MR to Q_n (′AC160)	5.0	1.5	6.0	9.5	1.5	11.0	ns	3-6
t_{PHL}	Propagation Delay MR to TC	5.0	2.5	—	13.0	2.5	14.0	ns	3-6

* Voltage Range 5.0 V is 5.0 V ±0.5 V.

MC74ACT162
AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT162 T_A = +25°C C_L = 50 pF			74ACT162 T_A = −40°C to +85°C C_L = 50 pF		Unit	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Count Frequency	5.0	120			100		MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n (PE Input HIGH)	5.0	2.0	6.0	10.0	2.0	11.5	ns	3-6
t_{PHL}	Propagation Delay CP to Q_n (PE Input HIGH)	5.0	2.0	6.0	10.0	2.0	11.0	ns	3-6
t_{PLH}	Propagation Delay CP to Q_n (PE Input LOW)	5.0	2.0	6.0	10.0	2.0	11.5	ns	3-6
t_{PHL}	Propagation Delay CP to Q_n (PE Input LOW)	5.0	2.0	6.0	10.0	2.0	11.0	ns	3-6
t_{PLH}	Propagation Delay CP to TC	5.0	2.0	8.0	13.0	2.0	14.5	ns	3-6
t_{PHL}	Propagation Delay CP to TC	5.0	2.0	8.0	13.0	2.0	14.5	ns	3-6
t_{PLH}	Propagation Delay CET to TC	5.0	2.0	6.0	9.0	2.0	10.5	ns	3-6
t_{PHL}	Propagation Delay CET to TC	5.0	2.0	6.0	9.0	2.0	10.5	ns	3-6

* Voltage Range 5.0 V is 5.0 V ±0.5 V. 3

MC74ACT160
AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT160 T_A = +25°C C_L = 50 pF		74ACT160 T_A = –40°C to +85°C C_L = 50 pF	Unit	Fig. No.
			Typ	Guaranteed Maximum			
t_s	Setup Time, HIGH or LOW P_n to CP	5.0	4.0	6.5	8.0	ns	3-9
t_h	Hold Time, HIGH or LOW P_n to CP	5.0	–4.0	–0.5	0	ns	3-9
t_s	Setup Time, HIGH or LOW PE or MR to CP	5.0	4.0	8.5	10.5	ns	3-9
t_h	Hold Time, HIGH or LOW PE or MR to CP	5.0	–4.0	0	0	ns	3-9
t_s	Setup Time, HIGH or LOW CEP or CET to CP	5.0	3.0	6.0	7.0	ns	3-9
t_h	Hold Time, HIGH or LOW CEP or CET to CP	5.0	–3.0	0	0	ns	3-9
t_w	Clock Pulse Width (Load) HIGH or LOW	5.0	3.0	4.0	4.0	ns	3-6
t_w	Clock Pulse Width (Count) HIGH or LOW	5.0	3.0	4.0	4.0	ns	3-6
t_w	$\overline{MR}$ Pulse Width, LOW (′ACT160)	5.0	2.0	4.0	6.0	ns	3-6
t_{rec}	Recovery Time MR to CP (′ACT160)	5.0	–1.0	0	0	ns	3-9

* Voltage Range 5.0 V is 5.0 V ±0.5 V.

MC74ACT162
AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT162 T_A = +25°C C_L = 50 pF		74ACT162 T_A = –40°C to +85°C C_L = 50 pF	Unit	Fig. No.
			Typ	Guaranteed Maximum			
t_s	Setup Time, HIGH or LOW P_n to CP	5.0	4.0	7.0	10.0	ns	3-9
t_h	Hold Time, HIGH or LOW P_n to CP	5.0	–3.0	–1.0	0	ns	3-9
t_s	Setup Time, HIGH or LOW PE to CP	5.0	4.0	7.0	10.0	ns	3-9
t_h	Hold Time, HIGH or LOW PE to CP	5.0	–3.0	–1.0	0	ns	3-9
t_s	Setup Time, HIGH or LOW SR to CP	5.0	5.0	10	11.5	ns	3-9
t_h	Hold Time, HIGH or LOW SR to CP	5.0	–5.0	0	0	ns	3-9
t_s	Setup Time, HIGH or LOW CET to CP	5.0	3.0	6.0	7.0	ns	3-9
t_h	Hold Time, HIGH or LOW CET to CP	5.0	–3.0	0	0	ns	3-9
t_w	Clock Pulse Width (Load) HIGH or LOW	5.0	2.0	4.5	5.0	ns	3-6
t_w	Clock Pulse Width (Count) HIGH or LOW	5.0	2.0	4.0	4.5	ns	3-6

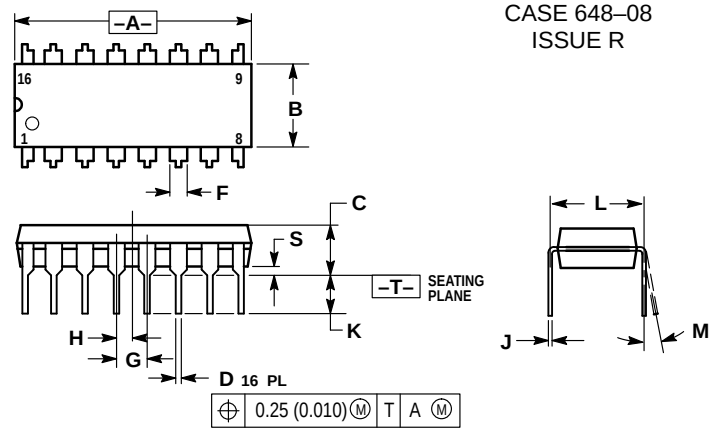
* Voltage Range 5.0 V is 5.0 V ±0.5 V.

CAPACITANCE

Symbol	Parameter	Value Typ	Unit	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	45	pF	V_{CC} = 5.0 V

OUTLINE DIMENSIONS

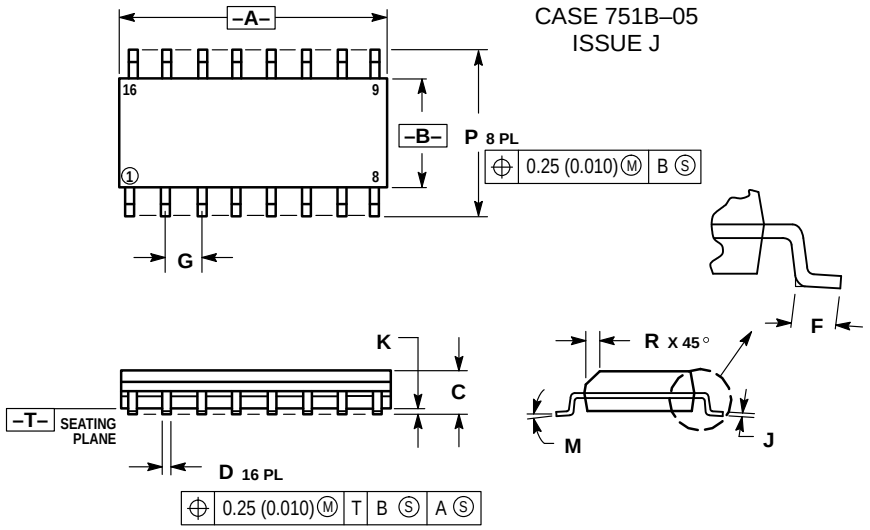
N SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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