

# Advance Information

## Clock Driver

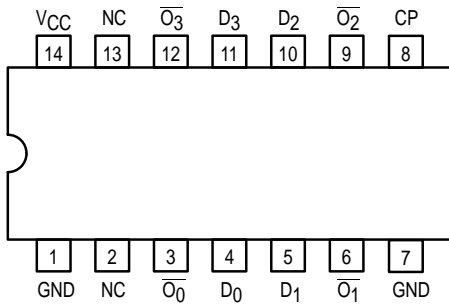
### Quad D-Type Flip-Flop

### With Matched Propagation Delays

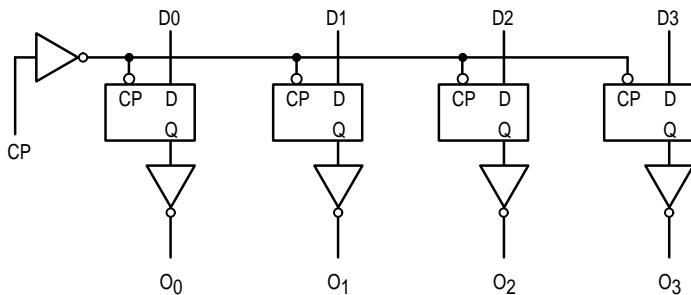
The MC74F1803 is a high-speed, low-power, quad D-type flip-flop featuring separate D-type inputs and inverting outputs with closely matched propagation delays. With a buffered clock (CP) input that is common to all flip-flops, the MC74F1803 is useful in high-frequency systems as a clock driver, providing multiple outputs that are synchronous. Because of the matched propagation delays, the duty cycles of the output waveforms in a clock driver application are symmetrical within 2.0 nanoseconds.

- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- Matched Outputs for Synchronous Clock Driver Applications
- Outputs Guaranteed for Simultaneous Switching

Pinout: 14-Lead Plastic (Top View)



LOGIC DIAGRAM



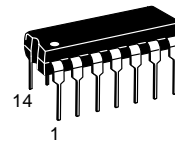
VCC = Pin 14; GND = Pins 1,7; NC = Pins 2, 13

NOTE: This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays

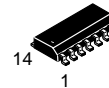
This document contains information on a new product. Specifications and information herein are subject to change without notice.

## MC74F1803

### CLOCK DRIVER QUAD D-TYPE FLIP-FLOP WITH MATCHED PROPAGATION DELAYS

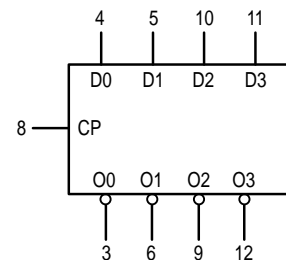


N SUFFIX  
PLASTIC  
CASE 646-06



D SUFFIX  
SOIC  
CASE 751A-03

LOGIC SYMBOL



VCC = PIN 14  
GND = PINS 1 AND 7  
NC = PINS 2 AND 13



# MC74F1803

## FUNCTIONAL DESCRIPTION

The MC74F1803 consists of four positive edge-triggered flip-flops with individual D-type inputs and inverting outputs. The buffered clock is common to all flip-flops and the following specifications allow for outputs switching simultaneously. The four flip-flops store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. The maximum frequency of the clock input is 70 megahertz and the LOW-to-HIGH and HIGH-to-LOW

propagation delays of the  $\overline{O_n}$  output vary by at most, 2.0 nanoseconds. Therefore, the device is ideal for use as a divide-by-two driver for high-frequency clock signals that require symmetrical duty cycles. In addition, the output-to-output skew is a maximum of 2.0 nanoseconds. Finally, the  $I_{OH}$  specification at 2.5 volts is guaranteed to be at least -20 milli-amps. If their inputs are identical, multiple outputs can be tied together and the  $I_{OH}$  is commensurately increased.

## GUARANTEED OPERATION RANGES

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	4.5	5.0	5.5	V
$T_A$	Operating Ambient Temperature Range	0	25	70	°C
$I_{OH}$	Output Current — High	—	—	-20	mA
$I_{OL}$	Output Current — Low	—	—	24	mA

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions 1,2
			Min	Typ	Max		
$V_{IH}$	Input HIGH Voltage		2.0	—	—	V	Guaranteed Input HIGH Voltage
$V_{IL}$	Input LOW Voltage		—	—	0.8	V	Guaranteed Input LOW Voltage
$V_{IK}$	Input Clamp Diode Voltage		—	—	-1.2	V	$V_{CC} = \text{MIN}$ , $I_{IN} = -18 \text{ mA}$
$V_{OH}$	Output HIGH Voltage $A_n$ Outputs	74	2.5	—	—	V	$I_{OH} = -20 \text{ mA}$ , $V_{CC} = 4.5 \text{ V}$
$V_{OL}$	Output LOW Voltage $A_n$ Outputs	74	—	0.35	0.5	V	$I_{OL} = 24 \text{ mA}$ , $V_{CC} = \text{MIN}$
$I_{IH}$	Input HIGH Current		—	—	20	$\mu\text{A}$	$V_{CC} = \text{MAX}$ , $V_{IN} = 2.7 \text{ V}$
			—	—	100	$\mu\text{A}$	$V_{CC} = \text{MAX}$ , $V_{IN} = 7.0 \text{ V}$
$I_{IL}$	Input LOW Current		—	—	-0.6	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 0.5 \text{ V}$
$I_{OS}$	Output Short Circuit Current <sup>3</sup>		-60	—	-150	mA	$V_{CC} = \text{MAX}$ , $V_{OUT} = 0 \text{ V}$
$I_{CC}$	Power Supply Current		—	—	70	mA	$V_{CC} = \text{MAX}$

<sup>1</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

<sup>2</sup> Normal test conditions for this device are all four outputs switching simultaneously. Two outputs of the MC74F1803 can be tied together and the  $I_{OH}$  doubles.

<sup>3</sup> Not more than one output should be shorted at a time, nor for more than 1 second.

## AC OPERATING REQUIREMENTS ( $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ ; $V_{CC} = +5.0 \text{ V} \pm 10\%$ ; $R_L = 500 \Omega$ )

Symbol	Parameter	$C_L = 50 \text{ pF}$		Unit
		Min	Max	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW: $D_n$ to CP	3.0 3.0	— —	ns
$t_f$	$t_p + t_s$ <sup>1</sup>	—	9.0	ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW: $D_n$ to CP	2.0 2.0	— —	ns
$t_w(H)$ $t_w(L)$	Cp Pulse Width HIGH or LOW	7.0 6.0	— —	ns

<sup>1</sup> The combination of the setup time ( $t_s$ ) requirement and maximum propagation delay ( $t_p$ ) are guaranteed to be within this limit for all conditions.

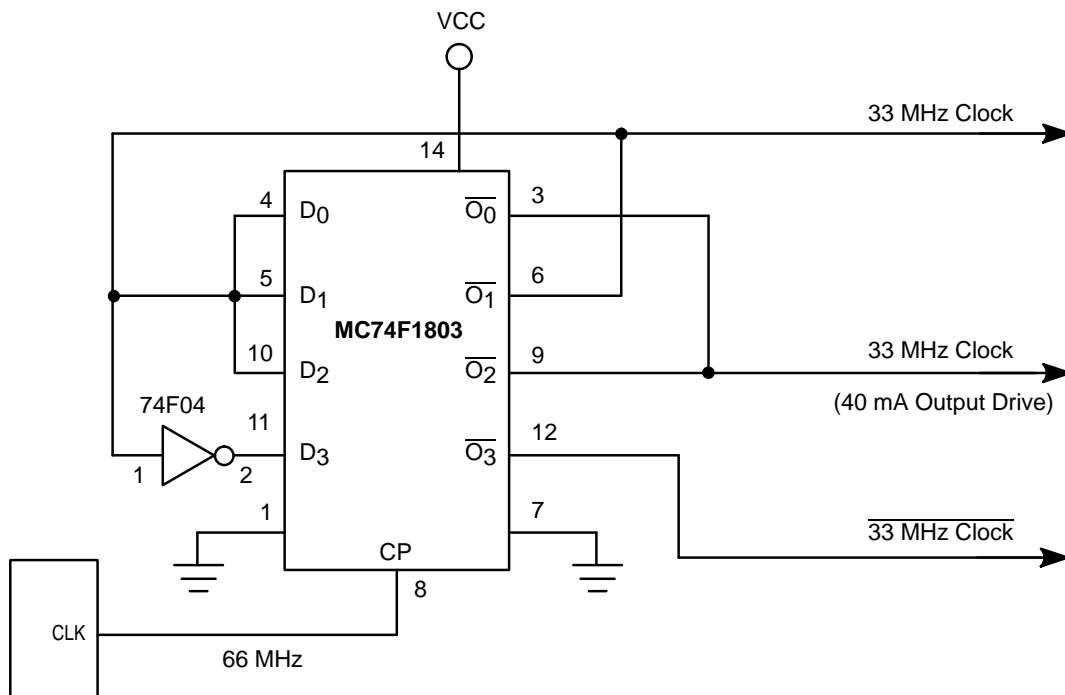
# MC74F1803

## AC ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 0°C to +70°C: V<sub>CC</sub> = +5.0 V ±10%: R<sub>L</sub> = 500 Ω) <sup>1</sup>

Symbol	Parameter	C <sub>L</sub> = 50 pF		Unit
		Min	Max	
f <sub>max</sub>	Maximum Clock Frequency	70	–	MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to $\overline{O}_n$	3.0	7.5	ns
t <sub>Pv</sub>	Propagation Delay CP to $\overline{O}_n$ Variation	–	3.0	ns
t <sub>ps</sub> $\overline{O}_0, \overline{O}_1, \overline{O}_2, \overline{O}_3$	Propagation Delay Skew  t <sub>PLH</sub> Actual – t <sub>PHL</sub> Actual  for $\overline{O}_0, \overline{O}_1, \overline{O}_2, \overline{O}_3$	–	2.0	ns
t <sub>os</sub>	Output to Output Skew <sup>2</sup>  t <sub>p</sub> $\overline{O}_n$ – t <sub>p</sub> $\overline{O}_m$	–	2.0	ns
t <sub>rise</sub> , t <sub>fall</sub> $\overline{O}_1$	Rise/Fall Time for $\overline{O}_1$ (0.8 to 2.0 V)	–	3.0	ns
t <sub>rise</sub> , t <sub>fall</sub> $\overline{O}_0, \overline{O}_2, \overline{O}_3$	Rise/Fall Time for $\overline{O}_1, \overline{O}_2, \overline{O}_3$ (0.8 to 2.0 V)	–	3.5	ns

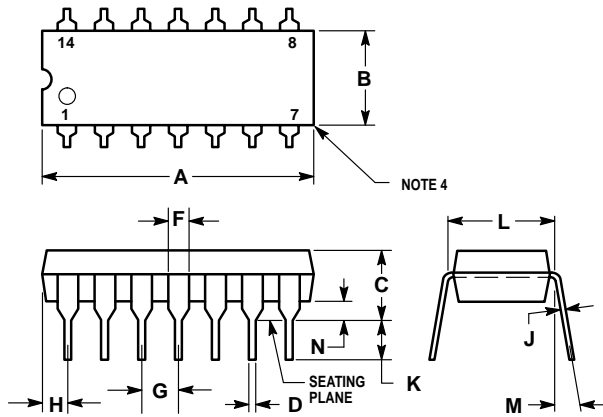
- <sup>1</sup> The test conditions used are all four outputs switching simultaneously. The AC characteristics described above are also guaranteed when two outputs are tied together.
- <sup>2</sup> Where t<sub>p</sub>  $\overline{O}_n$  and t<sub>p</sub>  $\overline{O}_m$  are the actual propagation delays (any combination of high or low) for two separate outputs from a given high transition of CP.
- <sup>3</sup> For a given set of conditions (i.e., capacitive load, temperature, V<sub>CC</sub>, and number of outputs switching simultaneously) the variation from device to device is guaranteed to be less than or equal to the maximum.

### TYPICAL MC74F1803 APPLICATION



OUTLINE DIMENSIONS

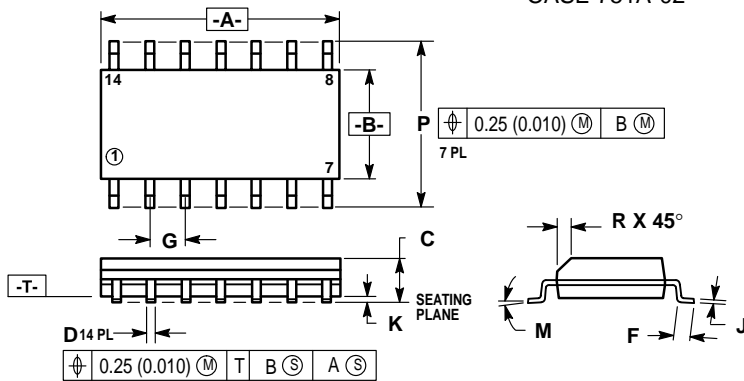
**N SUFFIX**  
PLASTIC PACKAGE  
CASE 646-06



- NOTES:
- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
  - DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
  - DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
  - ROUNDED CORNERS OPTIONAL.
  - 646-05 OBSOLETE, NEW STANDARD 646-06.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	0.62 BSC		0.300 BSC	
M	0.30	1.01	0.015	0.039
N				

**D SUFFIX**  
SOIC PACKAGE  
CASE 751A-02



- NOTES:
- DIMENSIONS "A" AND "B" ARE DATUMS AND "T" IS A DATUM SURFACE.
  - DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  - CONTROLLING DIMENSION: MILLIMETER.
  - DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  - MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  - 751A-01 IS OBSOLETE, NEW STANDARD 751A-02.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0	7	0	7
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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