MC74HC299

8-Bit Bidirectional Universal Shift Register with Parallel I/O

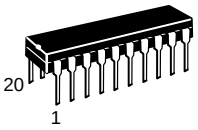
High–Performance Silicon–Gate CMOS

The MC74HC299 is identical in pinout to the LS299. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC299 features a multiplexed parallel input/output data port to achieve full 8–bit handling in a 20 pin package. Due to the large output drive capability and the 3–state feature, this device is ideally suited for interface with bus lines in a bus–oriented system.

Two Mode–Select inputs and two Output Enable inputs are used to choose the mode of operation as listed in the Function Table. Synchronous parallel loading is accomplished by taking both Mode–Select lines, S_1 and S_2, high. This places the outputs in the high–impedance state, which permits data applied to the data port to be clocked into the register. Reading out of the register can be accomplished when the outputs are enabled. The active–low asynchronous Reset overrides all other inputs.

- Output Drive Capability: 15 LSTTL Loads for Q_A through Q_H
  10 LSTTL Loads for Q_A' and Q_H'
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 398 FETs or 99.5 Equivalent Gates



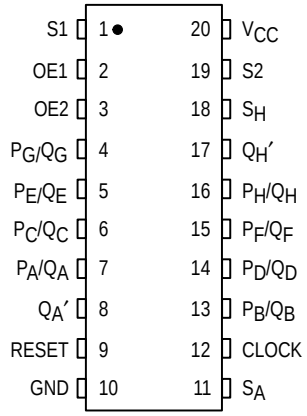
N SUFFIX
PLASTIC PACKAGE
CASE 738–03

DW SUFFIX
SOIC PACKAGE
CASE 751D–04

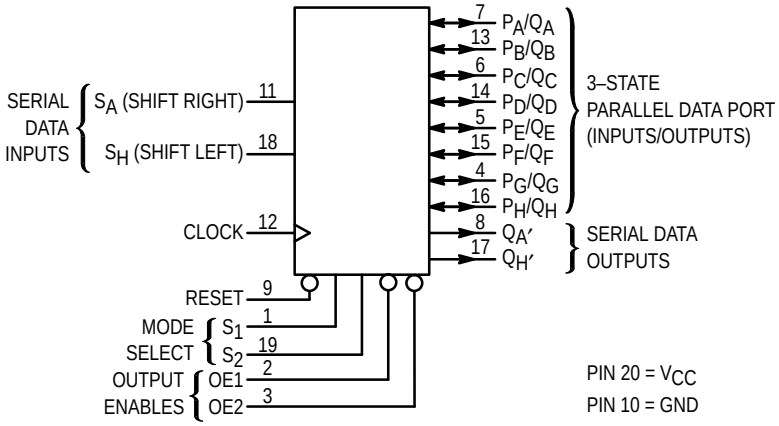
ORDERING INFORMATION

MC74HCXXXN	Plastic
MC74HCXXXDW	SOIC

PIN ASSIGNMENT



LOGIC DIAGRAM



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 1.5 to V_{CC} + 1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air Plastic DIP†	750	mW
	SOIC Package†	500	
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time V_{CC} = 2.0 V	0	1000	ns
	(Figure 1) V_{CC} = 4.5 V	0	500	
	V_{CC} = 6.0 V	0	400	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit – 55 to 25°C	Guaranteed Limit ≤ 85°C	Guaranteed Limit ≤ 125°C	Unit
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\| \le 20$ μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\| \le 20$ μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 20$ μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 6.0$ mA (P/Q)	4.5	3.98	3.84	3.70	
		$\|I_{out}\| \le 7.8$ mA (P/Q)	6.0	5.48	5.34	5.20	
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 4.0$ mA (Q′)	4.5	3.98	3.84	3.70	
		$\|I_{out}\| \le 5.2$ mA (Q′)	6.0	5.48	5.34	5.20	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 20$ μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 6.0$ mA (P/Q)	4.5	0.26	0.33	0.40	
		$\|I_{out}\| \le 7.8$ mA (P/Q)	6.0	0.26	0.33	0.40	
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 4.0$ mA (Q′)	4.5	0.26	0.33	0.40	
		$\|I_{out}\| \le 5.2$ mA (Q′)	6.0	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three–State Leakage Current (Q_A thru Q_H)	Output in High–Impedance State V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	6.0	± 0.5	± 5.0	± 10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 5)	2.0 4.5 6.0	5.0 25 29	4.0 20 24	3.4 17 20	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q_A' or Q_H' (Figures 1 and 5)	2.0 4.5 6.0	170 34 29	215 43 37	255 51 43	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q_A thru Q_H (Figures 1 and 5)	2.0 4.5 6.0	160 32 27	200 40 34	240 48 41	ns
t_{PHL}	Maximum Propagation Delay, Reset to Q_A or Q_H (Figures 2 and 5)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t_{PHL}	Maximum Propagation Delay, Reset to Q_A' thru Q_H' (Figures 2 and 5)	2.0 4.5 6.0	190 38 32	240 48 41	285 57 48	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, OE1, OE2, S1, or S2 to Q_A thru Q_H (Figures 3 and 6)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, OE1, OE2, S1, or S2 to Q_A thru Q_H (Figures 3 and 6)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Q_A thru Q_H (Figures 1 and 5)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Q_A' or Q_H' (Figures 1 and 5)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High–Impedance State), Q_A thru Q_H	—	15	15	15	pF

NOTES:
1. For propagation delays with loads other than 50 pF, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).
2. Information on typical parametric values can be found in Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Package)*, Outputs Enabled	240	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{su}	Minimum Setup Time, Mode Select S1 or S2 to Clock (Figure 4)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_{su}	Minimum Setup Time, Data Inputs S_A, S_H, P_A thru P_H to Clock (Figure 4)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_h	Minimum Hold Time, Clock to Mode Select S1 or S2 (Figure 4)	2.0 4.5 6.0	120 24 20	150 30 26	180 36 31	ns
t_h	Minimum Hold Time, Clock to Data Inputs, S_A, S_H, P_A thru P_H (Figure 4)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0 4.5 6.0	50 10 9	65 13 11	75 15 13	ns
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_f, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

FUNCTION TABLE

Inputs									Response									
		Mode Select		Output Enables			Serial Inputs											
Mode	Reset	S_2	S_1	OE1†	OE2†	Clock	D_A	D_H	P_A/Q_A	P_B/Q_B	P_C/Q_C	P_D/Q_D	P_E/Q_E	P_F/Q_F	P_G/Q_G	P_H/Q_H	Q_A'	Q_H'
Reset	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	X	X	X	Q_A through Q_H = Z								L	L
Shift Right	H	L	H	H	X	↗	D	X	Shift Right: Q_A through Q_H = Z; $D_A \rightarrow F_A$; $F_A \rightarrow F_B$; etc.								D	Q_G
	H	L	H	X	H	↗	D	X	Shift Right: Q_A through Q_H = Z; $D_A \rightarrow F_A$; $F_A \rightarrow F_B$; etc.								D	Q_G
	H	L	H	L	L	↗	D	X	Shift Right: $D_A \rightarrow F_A = Q_A$; $F_A \rightarrow F_B = Q_B$; etc.								D	Q_G
Shift Left	H	H	L	H	X	↗	X	D	Shift Left: Q_A through Q_H = Z; $D_H \rightarrow F_H$; $F_H \rightarrow F_G$; etc.								Q_B	D
	H	H	L	X	H	↗	X	D	Shift Left: Q_A through Q_H = Z; $D_H \rightarrow F_H$; $F_H \rightarrow F_G$; etc.								Q_B	D
	H	H	L	L	L	↗	X	D	Shift Left: $D_H \rightarrow F_H = Q_H$; $F_H \rightarrow F_G = Q_G$; etc.								Q_B	D
Parallel Load	H	H	H	X	X	↗	X	X	Parallel Load: $P_N \rightarrow F_N$								P_A	P_H
Hold	H	L	L	H	X	X	X	X	Hold: Q_A through Q_H = Z; $F_N = F_N$								P_A	P_H
	H	L	L	X	H	X	X	X	Hold: Q_A through Q_H = Z; $F_N = F_N$								P_A	P_H
	H	L	L	L	L	X	X	X	Hold: $Q_N = Q_N$								P_A	P_H

Z = high impedance
D = data on serial input
F = flip–flop (see Logic Diagram)
†When one or both output controls are high the eight input/output terminals are disabled to the high impedance state, however, sequential operation or clearing of the register is not affected.

PIN DESCRIPTIONS

DATA INPUTS

S_A (Pin 11)

Serial data input (Shift Right). Data on this input is shifted into the shift register on the rising edge of Clock when S2 is low and S1 is high (shift right mode).

S_H (Pin 18)

Serial data input (Shift Left). Data on this input is shifted into the shift register on the rising edge of Clock when S2 is high and S1 is low (shift left mode).

P_A through P_H (Pins 7, 13, 6, 14, 5, 15, 4, 16)

Parallel data port inputs. Data on these pins can be parallel loaded into the shift register on the rising edge of Clock when both S1 and S2 are high. For any other combination of S1 and S2, these pins serve as the outputs of the shift register.

CONTROL INPUTS

Clock (Pin 12)

Clock input. A low–to–high transition on this pin shifts the data at each stage to the next stage (shift right or left mode) or loads the data at the parallel data inputs into the shift register (parallel load mode).

OE1, OE2 (Pins 2, 3)

Active–low output enables. When both OE1 and OE2 are low, the Outputs Q_A through Q_H are enabled. When one or both output enables are high, the outputs are forced to the high–impedance state; however, sequential operation or clearing of the register is not affected.

Reset (Pin 9)

Active–low reset. A low on this pin resets all stages of the register to a low level. The reset operation is asynchronous.

S1, S2 (Pins 1, 19)

Mode select inputs. The levels present at these pins determine the shift register's mode of operation:

S1 = S2 = Low. Hold.
S1 = Low, S2 High. Shift left.
S1 = High, S2 Low. Shift right.
S1 = S2 = High. Parallel load.

OUTPUTS

Q_A', Q_H' (Pins 8, 17)

Serial data outputs. These are the outputs of the first and last stages of the shift register, respectively. These outputs are not 3–state outputs and have standard drive capabilities.

Q_A through Q_H (Pins 7, 13, 6, 14, 5, 15, 4, 16)

Parallel data port outputs. Shifted data is present at these pins when OE1 and OE2 are low. For all other combinations of OE1 and OE2 these outputs are in the high–impedance state.

SWITCHING WAVEFORMS

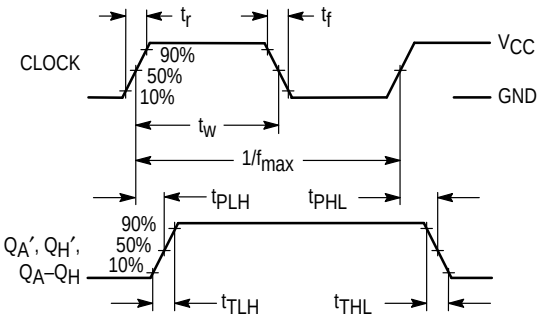


Figure 1.

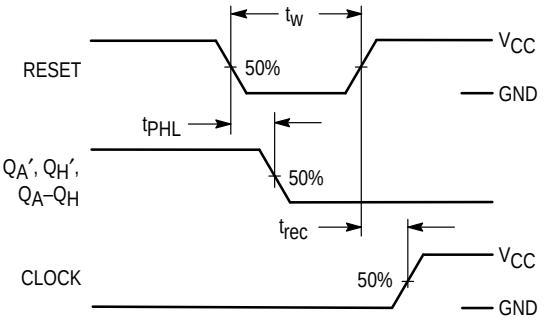


Figure 2.

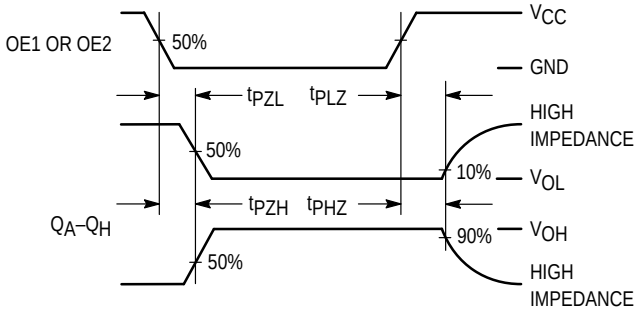


Figure 3a.

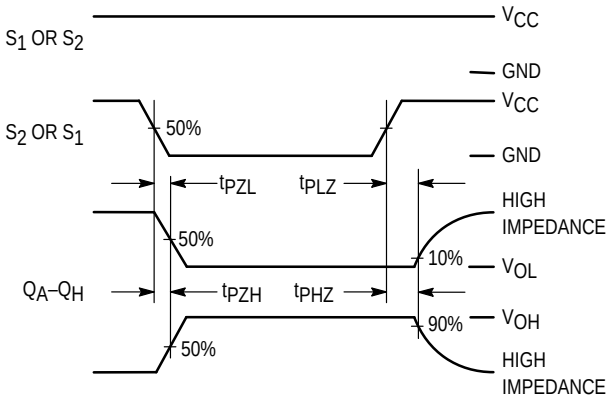


Figure 3b.

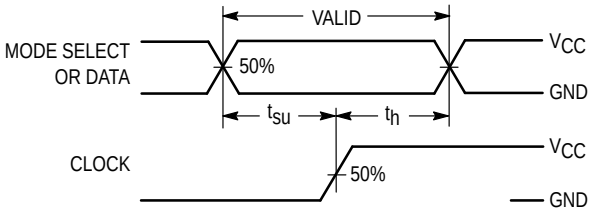
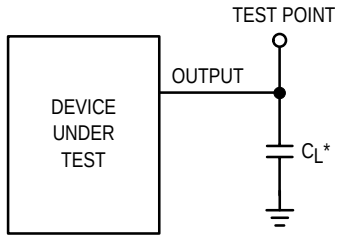
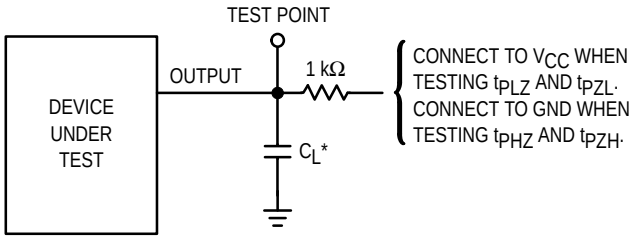


Figure 4.



* Includes all probe and jig capacitance

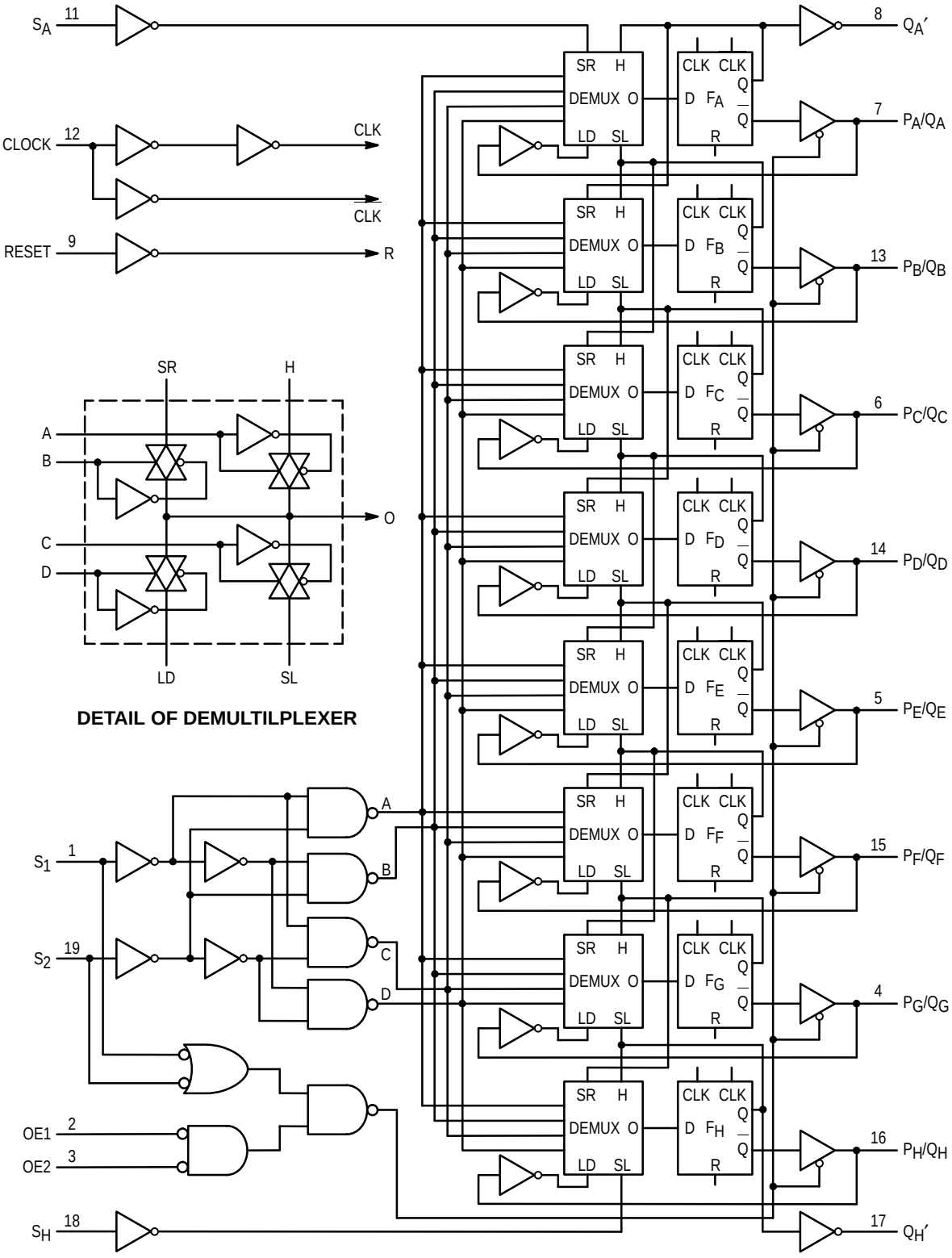
Figure 5. Test Circuit



* Includes all probe and jig capacitance

Figure 6. Test Circuit

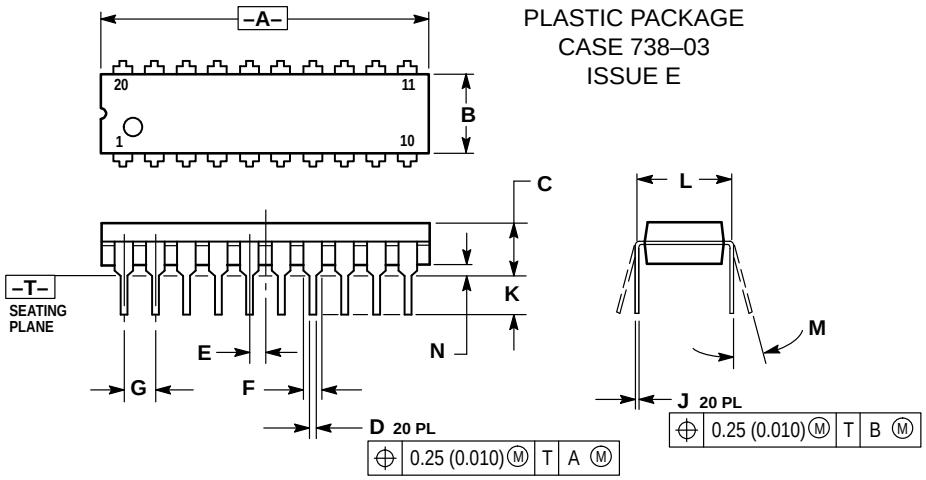
EXPANDED LOGIC DIAGRAM



DETAIL OF DEMULTILPLEXER

OUTLINE DIMENSIONS

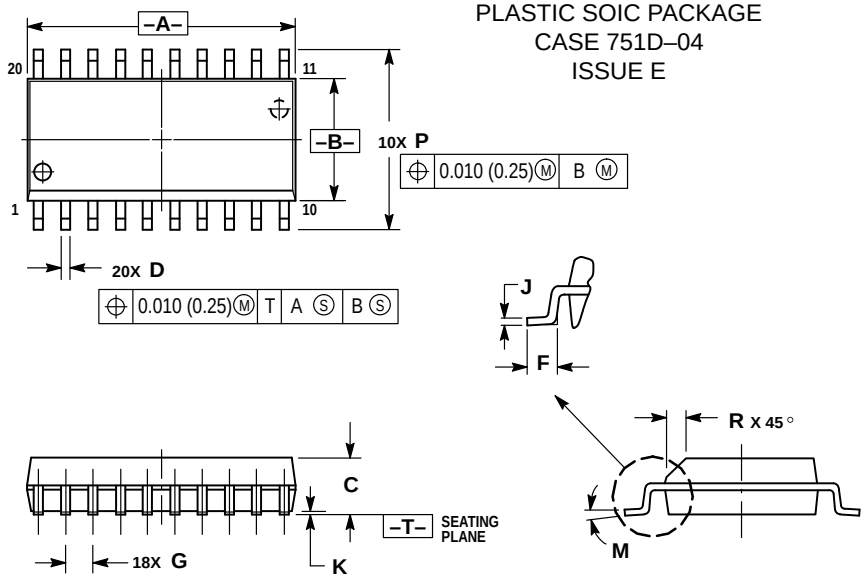
N SUFFIX
PLASTIC PACKAGE
CASE 738–03
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D–04
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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