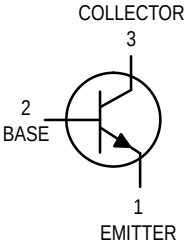
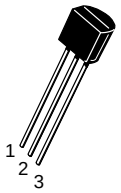
# High Voltage Transistor

## NPN Silicon

**BF844**




**CASE 29–04, STYLE 1**
**TO–92 (TO–226AA)**

### MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Collector–Emitter Voltage | $V_{CEO}$ | 400 | Vdc |
| Collector–Base Voltage | $V_{CBO}$ | 450 | Vdc |
| Emitter–Base Voltage | $V_{EBO}$ | 6.0 | Vdc |
| Collector Current — Continuous | $I_C$ | 300 | mAdc |
| Total Device Dissipation @ $T_A$ = 25°C<br>Derate above 25°C | $P_D$ | 625<br>5.0 | mW<br>mW/°C |
| Total Device Dissipation @ $T_C$ = 25°C<br>Derate above 25°C | $P_D$ | 1.5<br>12 | Watt<br>mW/°C |
| Operating and Storage Junction Temperature Range | $T_J$, $T_{stg}$ | –55 to +150 | °C |

### THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Thermal Resistance, Junction to Ambient | $R_{\theta JA}$ | 200 | °C/W |
| Thermal Resistance, Junction to Case | $R_{\theta JC}$ | 83.3 | °C/W |

### ELECTRICAL CHARACTERISTICS ($T_A$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | |
| Collector–Emitter Breakdown Voltage(1)<br>($I_C$ = 1.0 mAdc, $I_B$ = 0) | $V_{(BR)CEO}$ | 400 | — | Vdc |
| Collector–Emitter Breakdown Voltage<br>($I_C$ = 100 μAdc, $V_{BE}$ = 0) | $V_{(BR)CES}$ | 450 | — | Vdc |
| Collector–Base Breakdown Voltage<br>($I_C$ = 100 μAdc, $I_E$ = 0) | $V_{(BR)CBO}$ | 450 | — | Vdc |
| Emitter–Base Breakdown Voltage<br>($I_E$ = 10 μAdc, $I_C$ = 0) | $V_{(BR)EBO}$ | 6.0 | — | Vdc |
| Collector Cutoff Current<br>($V_{CB}$ = 400 Vdc, $I_E$ = 0) | $I_{CBO}$ | — | 0.1 | μAdc |
| Collector Cutoff Current<br>($V_{CE}$ = 400 Vdc, $V_{BE}$ = 0) | $I_{CES}$ | — | 500 | nAdc |
| Emitter Cutoff Current<br>($V_{EB}$ = 4.0 Vdc, $I_C$ = 0) | $I_{EBO}$ | — | 0.1 | μAdc |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted) (Continued)

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| **ON CHARACTERISTICS** | | | | |
| DC Current Gain(1)<br>($I_C$ = 1.0 mAdc, $V_{CE}$ = 10 Vdc)<br>($I_C$ = 10 mAdc, $V_{CE}$ = 10 Vdc)<br>($I_C$ = 50 mAdc, $V_{CE}$ = 10 Vdc)<br>($I_C$ = 100 mAdc, $V_{CE}$ = 10 Vdc) | $h_{FE}$ | <br>40<br>50<br>45<br>20 | <br>—<br>200<br>—<br>— | — |
| Collector–Emitter Saturation Voltage(1)<br>($I_C$ = 1.0 mAdc, $I_B$ = 0.1 mAdc)<br>($I_C$ = 10 mAdc, $I_B$ = 1.0 mAdc)<br>($I_C$ = 50 mAdc, $I_B$ = 5.0 mAdc) | $V_{CE(sat)}$ | <br>—<br>—<br>— | <br>0.4<br>0.5<br>0.75 | Vdc |
| Base–Emitter Saturation Voltage<br>($I_C$ = 10 mAdc, $I_B$ = 1.0 mAdc) | $V_{BE(sat)}$ | — | 0.75 | Vdc |
| **DYNAMIC CHARACTERISTICS** | | | | |
| High Frequency Current Gain<br>($I_C$ = 10 mAdc, $V_{CE}$ = 10 Vdc, f = 20 MHz) | $\|h_{fe}\|$ | 1.0 | — | |
| Collector–Base Capacitance<br>($V_{CB}$ = 20 Vdc, $I_E$ = 0, f = 1.0 MHz) | $C_{ob}$ | — | 6.0 | pF |
| Emitter–Base Capacitance<br>($V_{EB}$ = 0.5 Vdc, $I_C$ = 0, f = 1.0 MHz) | $C_{ib}$ | — | 110 | pF |
| Turn–On Time<br>($V_{CC}$ = 150 Vdc, $V_{BE(off)}$ = 4.0 V, $I_C$ = 30 mAdc, $I_{B1}$ = 3.0 mAdc) | $t_{on}$ | — | 0.6 | μs |
| Turn–Off Time<br>($V_{CC}$ = 150 Vdc, $I_C$ = 30 mAdc, $I_{B1}$ = $I_{B2}$ = 3.0 mAdc) | $t_{off}$ | — | 10 | μs |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

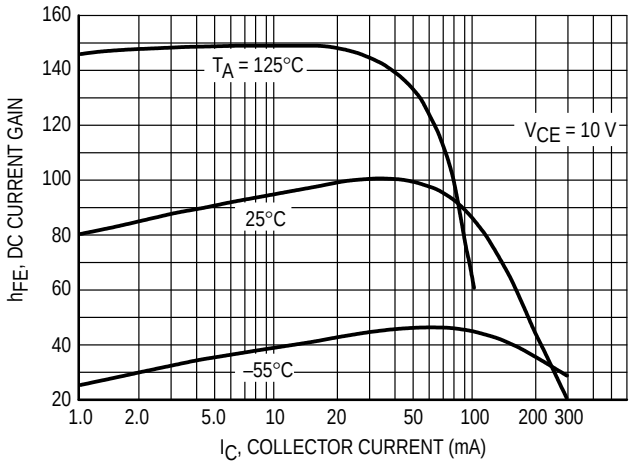



**Figure 1. DC Current Gain**

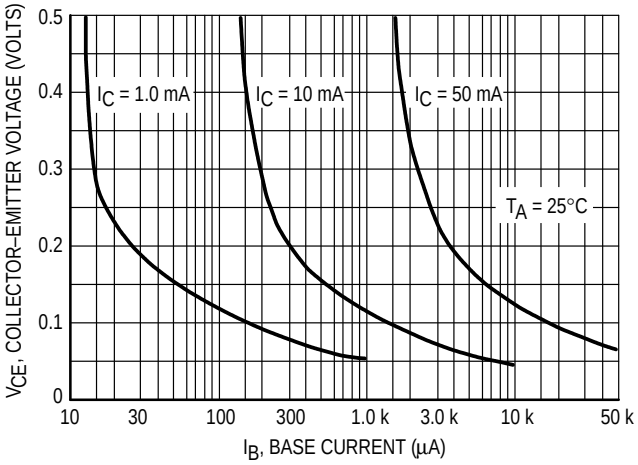



**Figure 2. Collector Saturation Region**

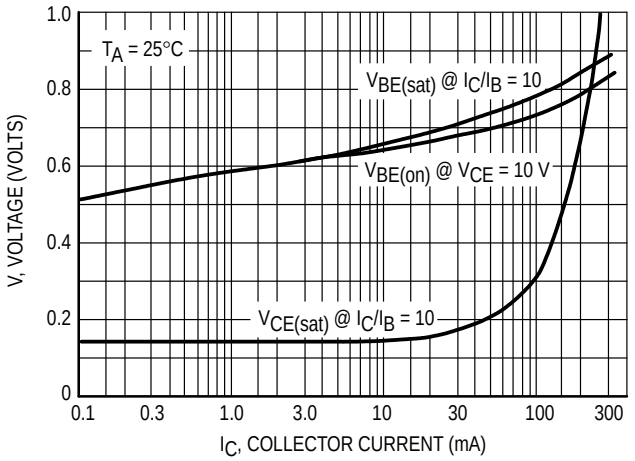



**Figure 3. On Voltages**

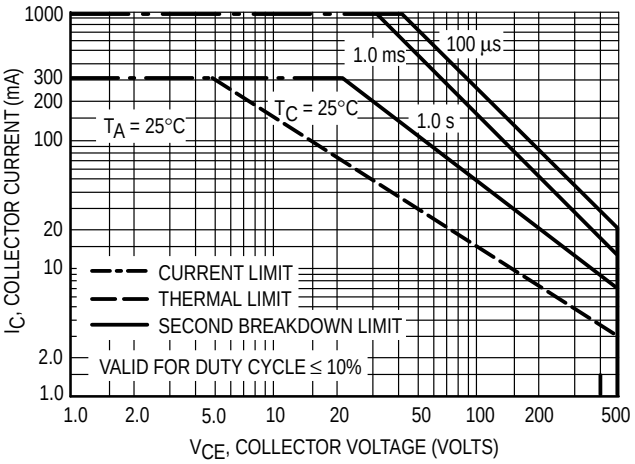



**Figure 4. Active Region Safe Operating Area**

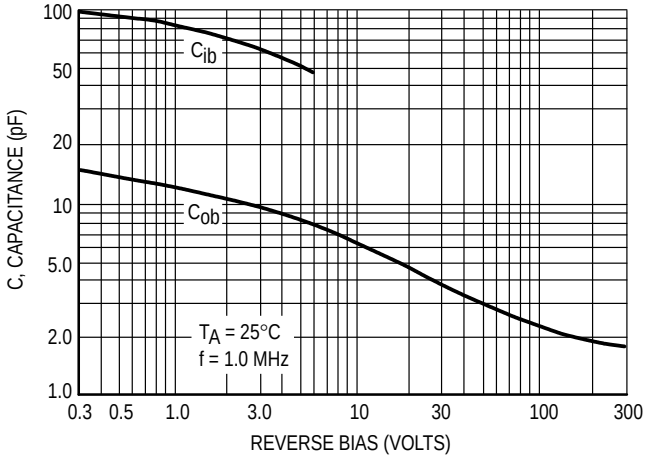



**Figure 5. Capacitance**

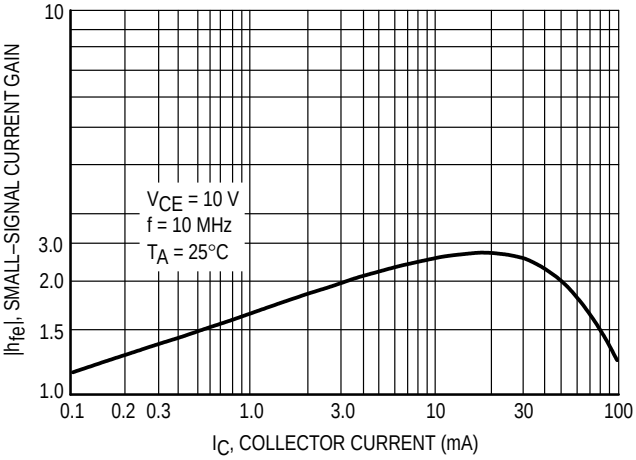



**Figure 6. High Frequency Current Gain**

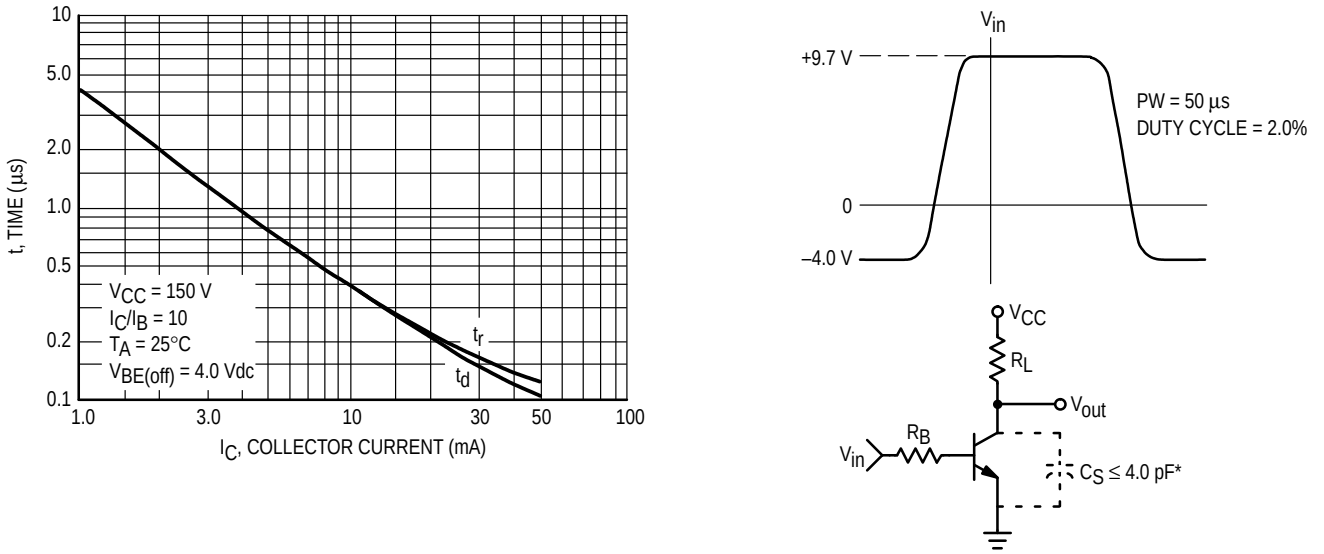



**Figure 7. Turn–On Switching Times and Test Circuit**

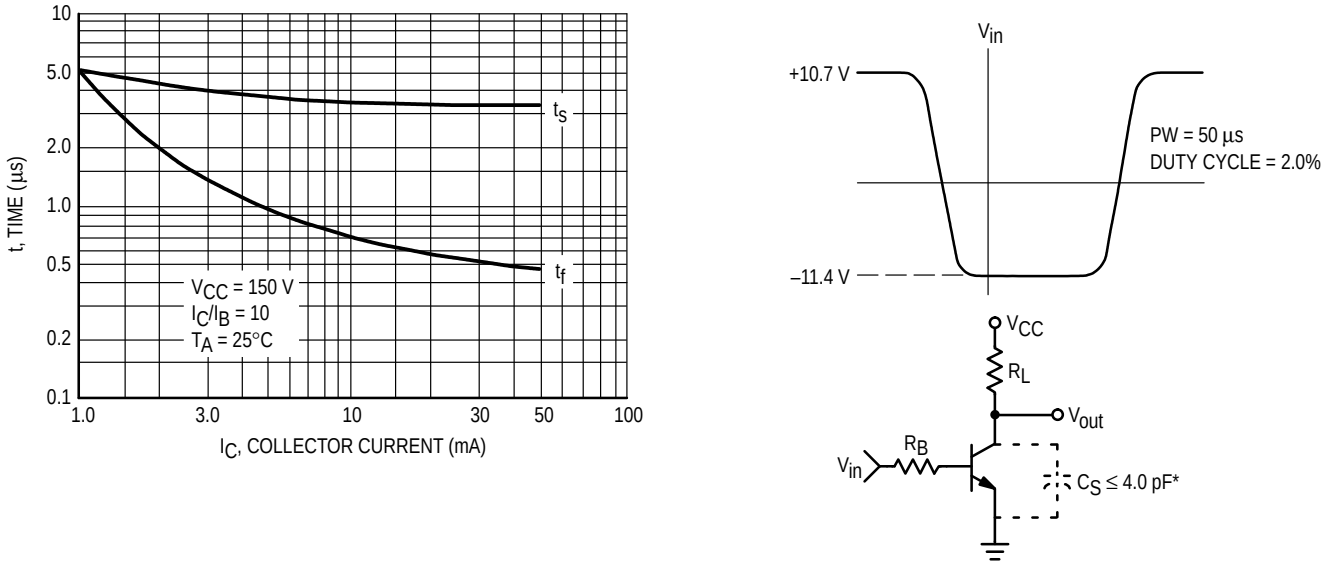
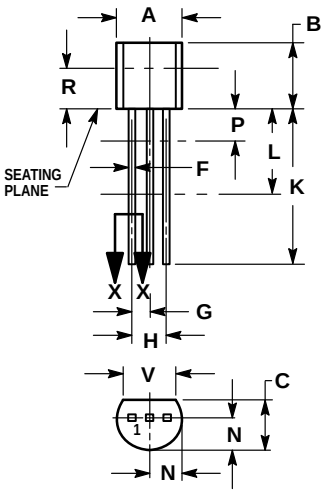
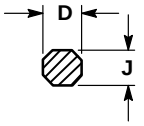



**Figure 8. Turn–Off Switching Times and Test Circuit**

* Total Shunt Capacitance or Test Jig and Connectors.

## PACKAGE DIMENSIONS




SECTION X–X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN P AND L. DIMENSION D AND J APPLY BETWEEN L AND K MINIMUM. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.175 | 0.205 | 4.45 | 5.20 |
| B | 0.170 | 0.210 | 4.32 | 5.33 |
| C | 0.125 | 0.165 | 3.18 | 4.19 |
| D | 0.016 | 0.022 | 0.41 | 0.55 |
| F | 0.016 | 0.019 | 0.41 | 0.48 |
| G | 0.045 | 0.055 | 1.15 | 1.39 |
| H | 0.095 | 0.105 | 2.42 | 2.66 |
| J | 0.015 | 0.020 | 0.39 | 0.50 |
| K | 0.500 | — | 12.70 | — |
| L | 0.250 | — | 6.35 | — |
| N | 0.080 | 0.105 | 2.04 | 2.66 |
| P | — | 0.100 | — | 2.54 |
| R | 0.115 | — | 2.93 | — |
| V | 0.135 | — | 3.43 | — |

**CASE 029–04**
**(TO–226AA)**
**ISSUE AD**

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

**How to reach us:**
**USA / EUROPE / Locations Not Listed**: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447 or 602–303–5454

**MFAX**: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609
**INTERNET**: http://Design–NET.com

**JAPAN**: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center,
3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–81–3521–8315

**ASIA / PACIFIC**: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298