Designer's™ Data Sheet
SWITCHMODE™
NPN Bipolar Power Transistor For Switching Power Supply Applications

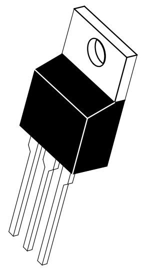
The BUL146/BUL146F have an applications specific state–of–the–art die designed for use in fluorescent electric lamp ballasts to 130 Watts and in Switchmode Power supplies for all types of electronic equipment. These high voltage/high speed transistors offer the following:

- Improved Efficiency Due to Low Base Drive Requirements:
  — High and Flat DC Current Gain
  — Fast Switching
  — No Coil Required in Base Circuit for Turn–Off (No Current Tail)
- Full Characterization at 125°C
- Parametric Distributions are Tight and Consistent Lot–to–Lot
- Two Package Choices: Standard TO–220 or Isolated TO–220
- BUL146F, Isolated Case 221D, is UL Recognized to 3500 V_{RMS}: File #E69369

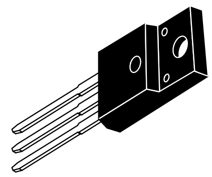
BUL146*
BUL146F*

*Motorola Preferred Device

**POWER TRANSISTOR
6.0 AMPERES
700 VOLTS
40 and 100 WATTS**



**BUL146
CASE 221A–06
TO–220AB**



**BUL146F
CASE 221D–02
ISOLATED TO–220 TYPE
UL RECOGNIZED**

MAXIMUM RATINGS

Rating	Symbol	BUL146	BUL146F	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	400		Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	700		Vdc
Emitter–Base Voltage	V_{EBO}	9.0		Vdc
Collector Current — Continuous — Peak(1)	I_C I_{CM}	6.0 15		Adc
Base Current — Continuous — Peak(1)	I_B I_{BM}	4.0 8.0		Adc
RMS Isolated Voltage(2) Test No. 1 Per Fig. 22a (for 1 sec, R.H. < 30%, Test No. 2 Per Fig. 22b T_C = 25°C) Test No. 3 Per Fig. 22c	V_{ISOL}	— — —	4500 3500 1500	V
Total Device Dissipation (T_C = 25°C) Derate above 25°C	P_D	100 0.8	40 0.32	Watts W/°C
Operating and Storage Temperature	T_J, T_{stg}	– 65 to 150		°C

THERMAL CHARACTERISTICS

Rating	Symbol	BUL44	BUL44F	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.25 62.5	3.125 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	260		°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)	$V_{CEO(sus)}$	400	—	—	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)	I_{CEO}	—	—	100	µAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0) (T_C = 125°C) (V_{CE} = 500 V, V_{EB} = 0) (T_C = 125°C)	I_{CES}	— — —	— — —	100 500 100	µAdc
Emitter Cutoff Current (V_{EB} = 9.0 Vdc, I_C = 0)	I_{EBO}	—	—	100	µAdc

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.
(2) Proper strike and creepage distance must be provided.

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
Base–Emitter Saturation Voltage (I_C = 1.3 Adc, I_B = 0.13 Adc) (I_C = 3.0 Adc, I_B = 0.6 Adc)	$V_{BE(sat)}$	— —	0.82 0.93	1.1 1.25	Vdc
Collector–Emitter Saturation Voltage (I_C = 1.3 Adc, I_B = 0.13 Adc) (T_C = 125°C) (I_C = 3.0 Adc, I_B = 0.6 Adc) (T_C = 125°C)	$V_{CE(sat)}$	— — — —	0.22 0.20 0.30 0.30	0.5 0.5 0.7 0.7	Vdc
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 5.0 Vdc) (T_C = 125°C) (I_C = 1.3 Adc, V_{CE} = 1.0 Vdc) (T_C = 125°C) (I_C = 3.0 Adc, V_{CE} = 1.0 Vdc) (T_C = 125°C) (I_C = 10 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	14 — 12 12 8.0 7.0 10	— 30 20 20 13 12 20	34 — — — — — —	—
DYNAMIC CHARACTERISTICS					
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	—	14	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{OB}	—	95	150	pF
Input Capacitance (V_{EB} = 8.0 V)	C_{IB}	—	1000	1500	pF
Dynamic Saturation Voltage: Determined 1.0 µs and 3.0 µs respectively after rising I_{B1} reaches 90% of final I_{B1} (see Figure 18); (I_C = 1.3 Adc, I_{B1} = 300 mAdc, V_{CC} = 300 V) 1.0 µs (T_C = 125°C)	$V_{CE(dsat)}$	— —	2.5 6.5	— —	V
(I_C = 1.3 Adc, I_{B1} = 300 mAdc, V_{CC} = 300 V) 3.0 µs (T_C = 125°C)		— —	0.6 2.5	— —	
(I_C = 3.0 Adc, I_{B1} = 0.6 Adc, V_{CC} = 300 V) 1.0 µs (T_C = 125°C)		— —	3.0 7.0	— —	
(I_C = 3.0 Adc, I_{B1} = 0.6 Adc, V_{CC} = 300 V) 3.0 µs (T_C = 125°C)		— —	0.75 1.4	— —	
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 µs)					
Turn–On Time (I_C = 1.3 Adc, I_{B1} = 0.13 Adc, I_{B2} = 0.65 Adc, V_{CC} = 300 V) (T_C = 125°C)	t_{on}	— —	100 90	200 —	ns
Turn–Off Time (T_C = 125°C)	t_{off}	— —	1.35 1.90	2.5 —	µs
Turn–On Time (I_C = 3.0 Adc, I_{B1} = 0.6 Adc, I_{B1} = 1.5 Adc, V_{CC} = 300 V) (T_C = 125°C)	t_{on}	— —	90 100	150 —	ns
Turn–Off Time (T_C = 125°C)	t_{off}	— —	1.7 2.1	2.5 —	µs
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 µH)					
Fall Time (I_C = 1.3 Adc, I_{B1} = 0.13 Adc, I_{B2} = 0.65 Adc) (T_C = 125°C)	t_{fi}	— —	115 120	200 —	ns
Storage Time (T_C = 125°C)	t_{si}	— —	1.35 1.75	2.5 —	µs
Crossover Time (T_C = 125°C)	t_c	— —	200 210	350 —	ns
Fall Time (I_C = 3.0 Adc, I_{B1} = 0.6 Adc, I_{B2} = 1.5 Adc) (T_C = 125°C)	t_{fi}	— —	85 100	150 —	ns
Storage Time (T_C = 125°C)	t_{si}	— —	1.75 2.25	2.5 —	µs
Crossover Time (T_C = 125°C)	t_c	— —	175 200	300 —	ns
Fall Time (I_C = 3.0 Adc, I_{B1} = 0.6 Adc, I_{B2} = 0.6 Adc) (T_C = 125°C)	t_{fi}	80 —	— 210	180 —	ns
Storage Time (T_C = 125°C)	t_{si}	2.6 —	— 4.5	3.8 —	µs
Crossover Time (T_C = 125°C)	t_c	— —	230 400	350 —	ns

TYPICAL STATIC CHARACTERISTICS

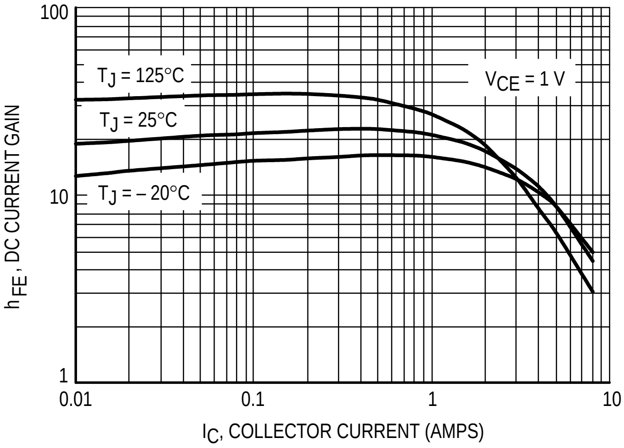


Figure 1. DC Current Gain @ 1 Volt

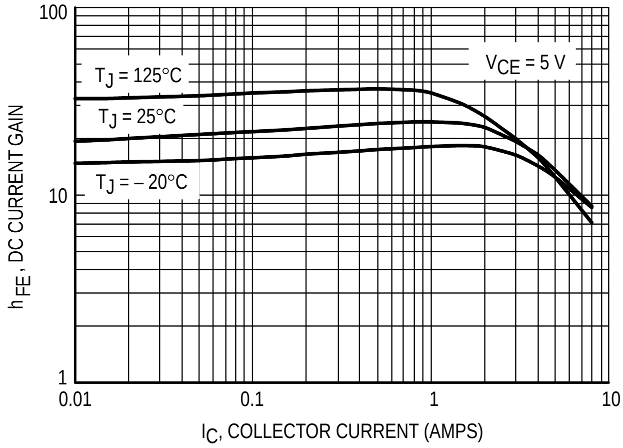


Figure 2. DC Current Gain @ 5 Volts

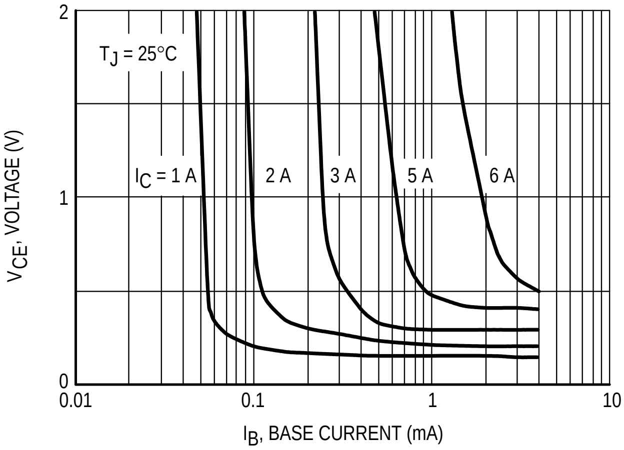


Figure 3. Collector Saturation Region

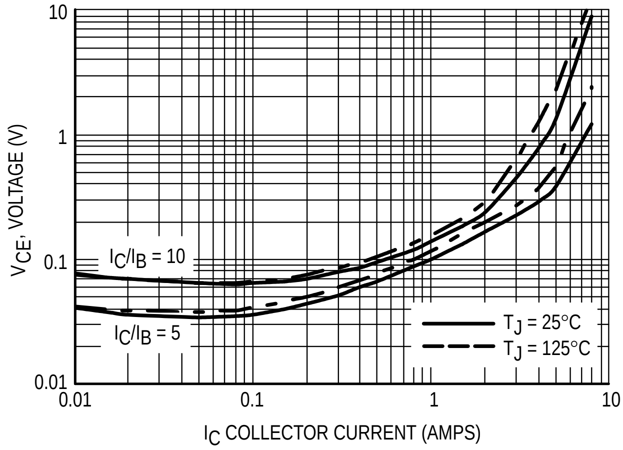


Figure 4. Collector–Emitter Saturation Voltage

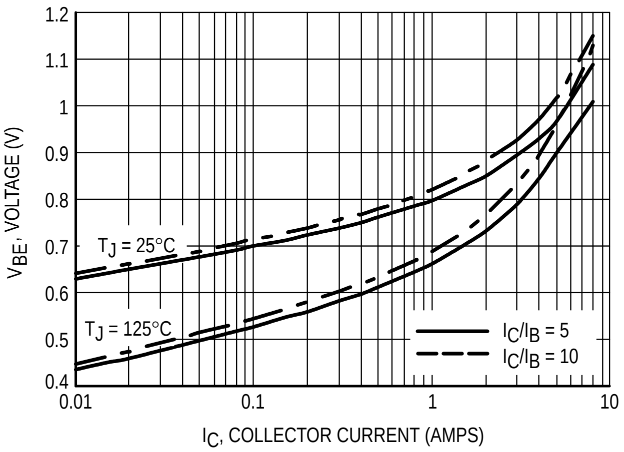


Figure 5. Base–Emitter Saturation Region

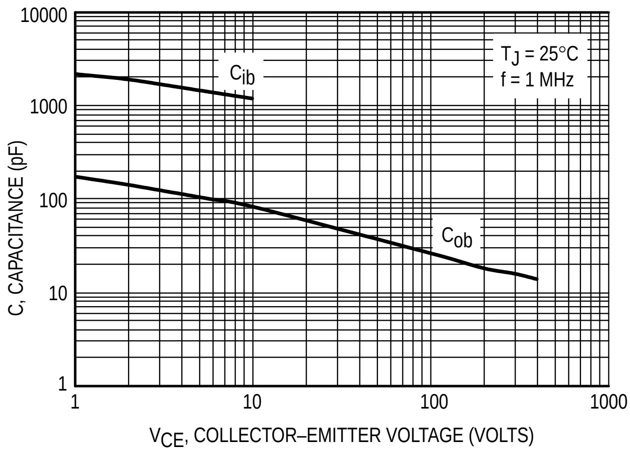


Figure 6. Capacitance

TYPICAL SWITCHING CHARACTERISTICS
(I_{B2} = I_C/2 for all switching)

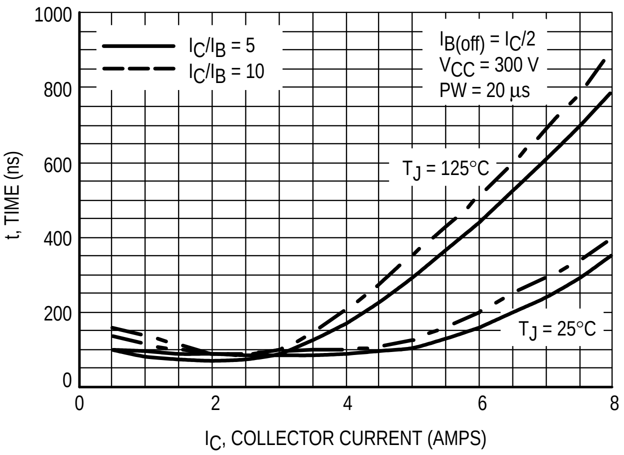


Figure 7. Resistive Switching, t_{on}

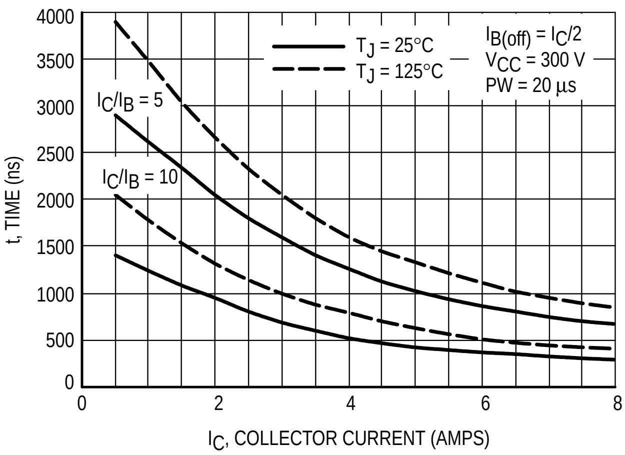


Figure 8. Resistive Switching, t_{off}

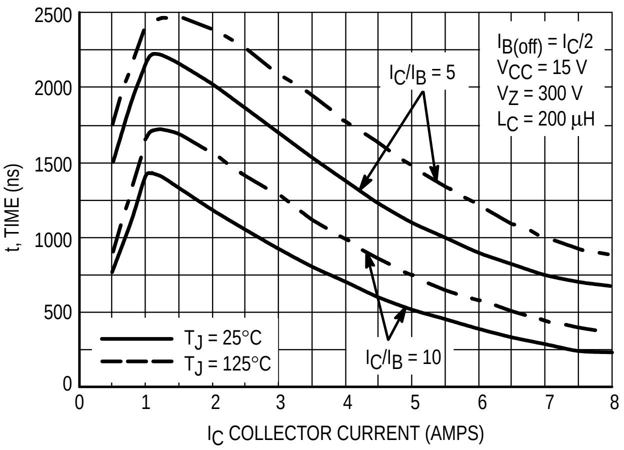


Figure 9. Inductive Storage Time, t_{si}

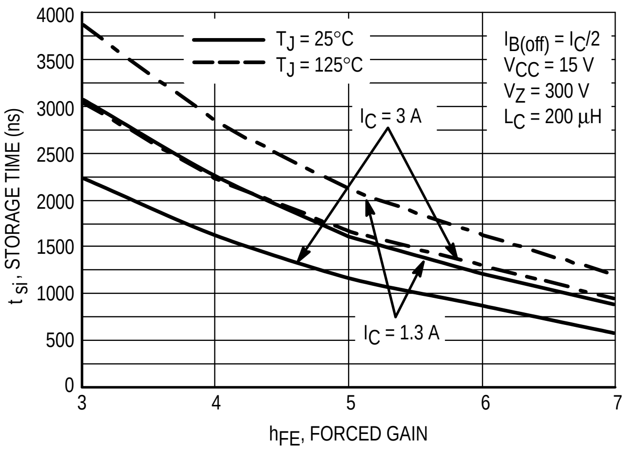


Figure 10. Inductive Storage Time, $t_{si}(h_{FE})$

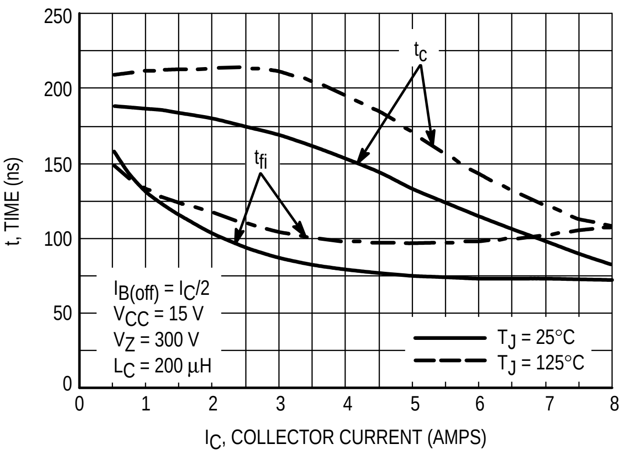


Figure 11. Inductive Switching, t_c and t_{fi}
I_C/I_B = 5

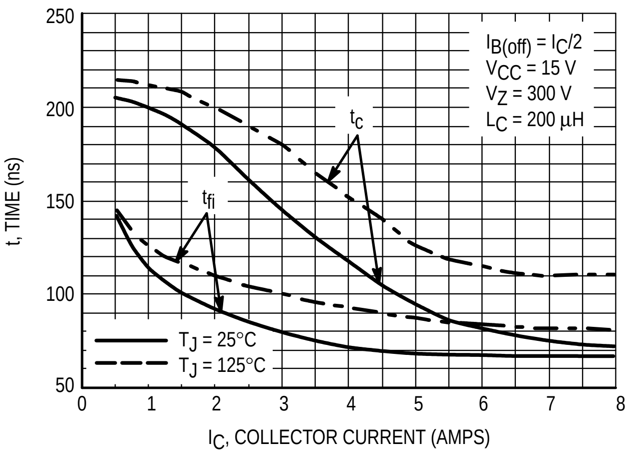


Figure 12. Inductive Switching, t_c and t_{fi}
I_C/I_B = 10

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

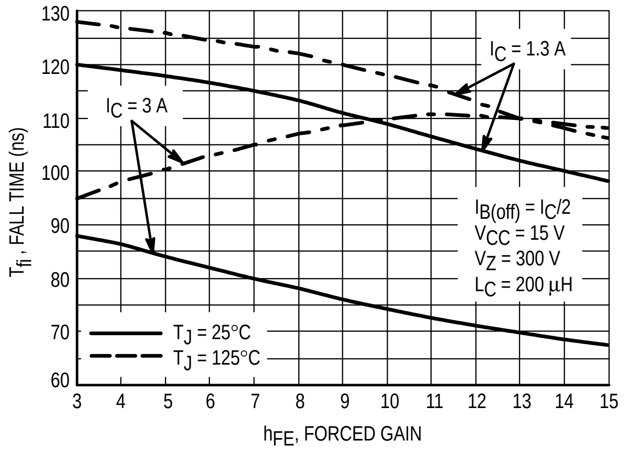


Figure 13. Inductive Fall Time

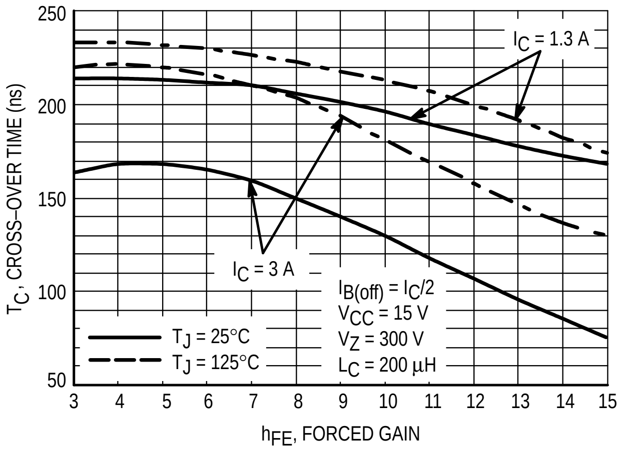


Figure 14. Inductive Cross–Over Time

GUARANTEED SAFE OPERATING AREA INFORMATION

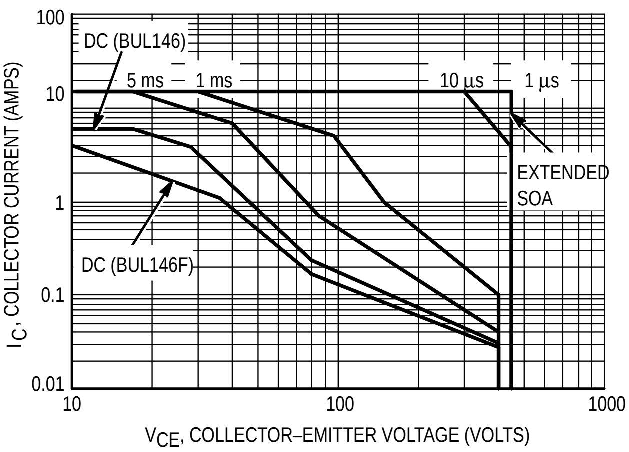


Figure 15. Forward Bias Safe Operating Area

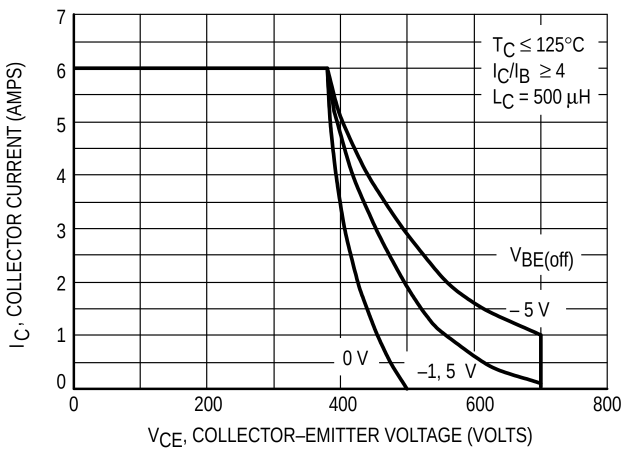


Figure 16. Reverse Bias Switching Safe Operating Area

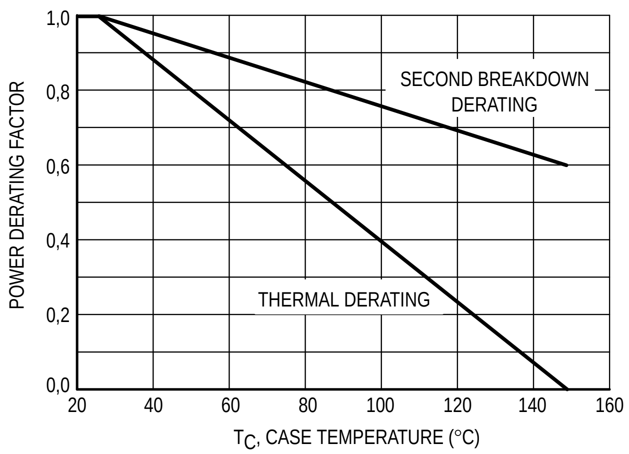


Figure 17. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 15 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown in Figure 15 may be found at any case temperature by using the appropriate curve on Figure 17. $T_{J(pk)}$ may be calculated from the data in Figure 20 and 21. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn–off with the base–to–emitter junction reverse–biased. The safe level is specified as a reverse–biased safe operating area (Figure 16). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

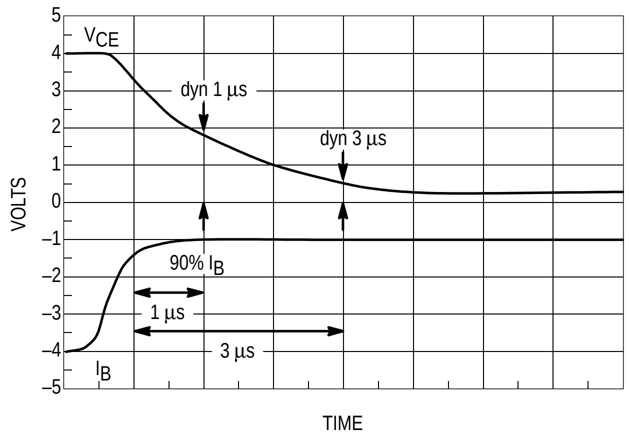


Figure 18. Dynamic Saturation Voltage Measurements

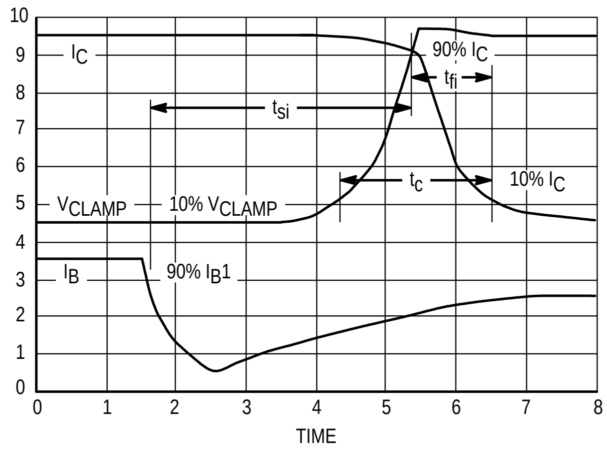
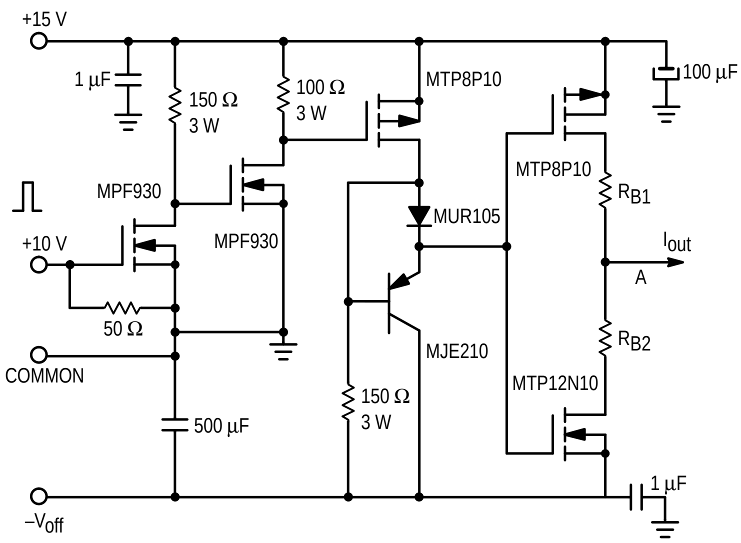
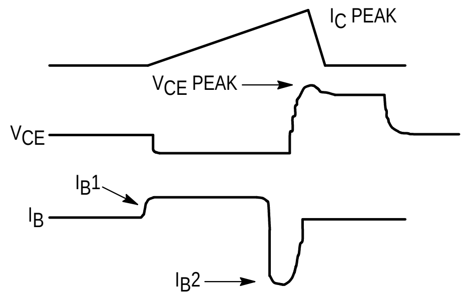


Figure 19. Inductive Switching Measurements





V(BR)CEO(sus)	INDUCTIVE SWITCHING	RBSOA
L = 10 mH	L = 200 µH	L = 500 µH
RB2 = ∞	RB2 = 0	RB2 = 0
V_{CC} = 20 VOLTS	V_{CC} = 15 VOLTS	V_{CC} = 15 VOLTS
I_C(pk) = 100 mA	RB1 SELECTED FOR DESIRED I_B1	RB1 SELECTED FOR DESIRED I_B1

Table 1. Inductive Load Switching Drive Circuit

TYPICAL THERMAL RESPONSE

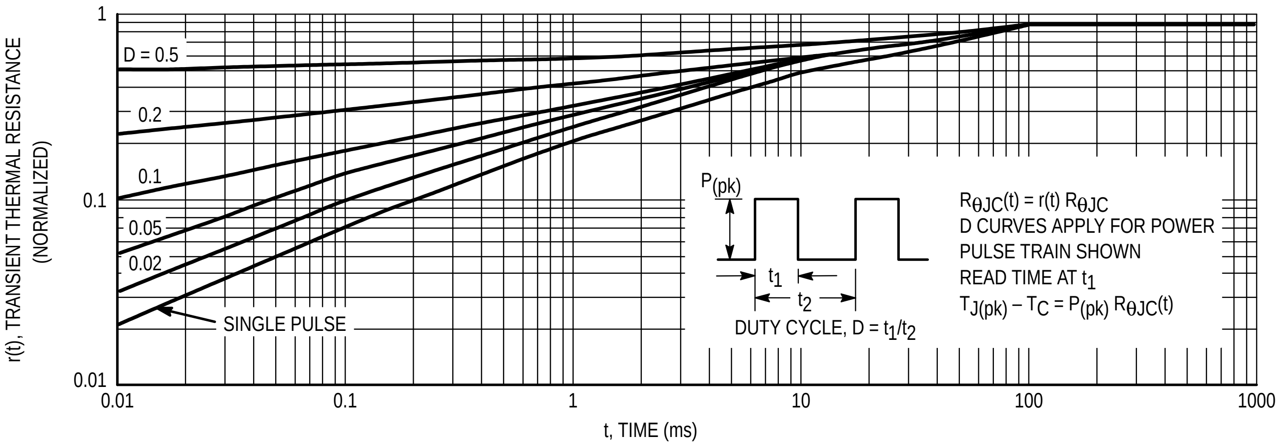


Figure 20. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUL146

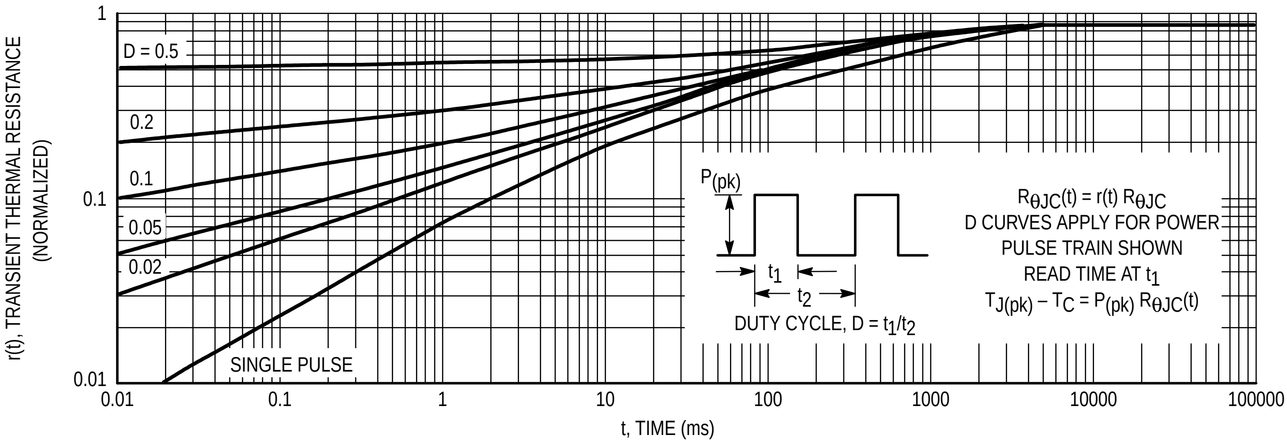


Figure 21. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUL146F

TEST CONDITIONS FOR ISOLATION TESTS*

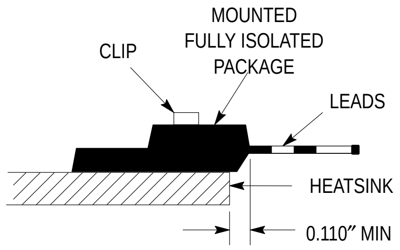


Figure 22a. Screw or Clip Mounting Position for Isolation Test Number 1

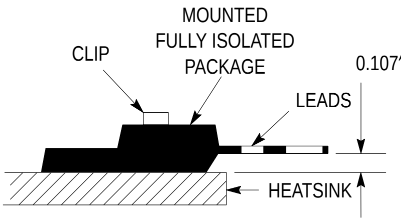


Figure 22b. Clip Mounting Position for Isolation Test Number 2

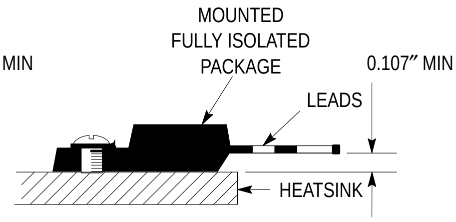


Figure 22c. Screw Mounting Position for Isolation Test Number 3

* Measurement made between leads and heatsink with all leads shorted together.

MOUNTING INFORMATION**

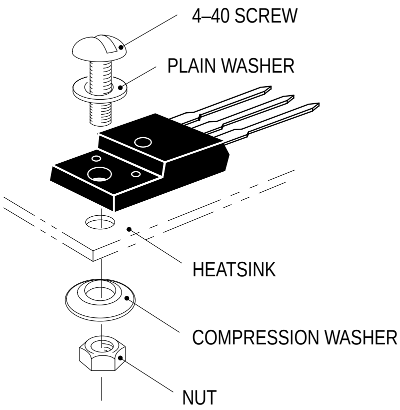


Figure 23a. Screw–Mounted

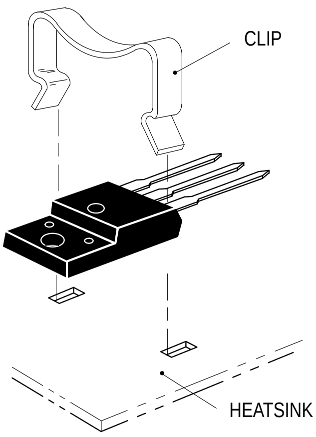


Figure 23b. Clip–Mounted

Figure 23. Typical Mounting Techniques for Isolated Package

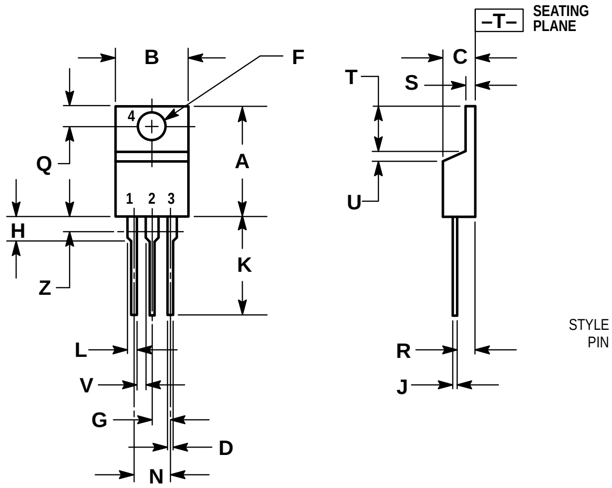
Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, Motorola does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

PACKAGE DIMENSIONS

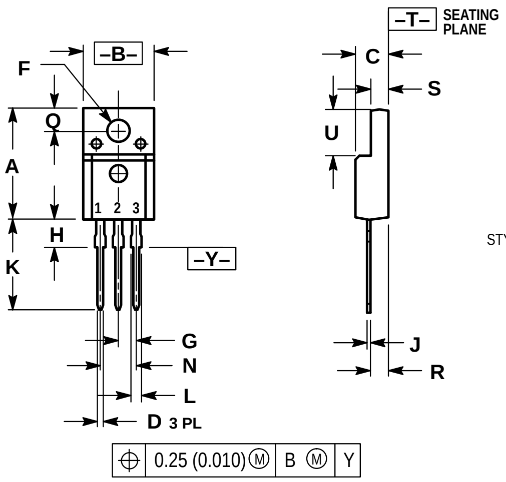


STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	—	1.15	—
Z	—	0.080	—	2.04

BUL44
CASE 221A–06
TO–220AB
ISSUE Y



STYLE 2:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.621	0.629	15.78	15.97
B	0.394	0.402	10.01	10.21
C	0.181	0.189	4.60	4.80
D	0.026	0.034	0.67	0.86
F	0.121	0.129	3.08	3.27
G	0.100 BSC		2.54 BSC	
H	0.123	0.129	3.13	3.27
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.14	1.52
N	0.200 BSC		5.08 BSC	
Q	0.126	0.134	3.21	3.40
R	0.107	0.111	2.72	2.81
S	0.096	0.104	2.44	2.64
U	0.259	0.267	6.58	6.78

BUL44F
CASE 221D–02
(ISOLATED TO–220 TYPE)
ISSUE D

How to reach us:
USA / EUROPE: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE (602) 244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, Toshikatsu Otsuki,
6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–3521–8315

HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298