Silicon Bidirectional Triode Thyristors

. . . designed for use in solid state relays, MPU interface, TTL logic and any other light industrial or consumer application. Supplied in an inexpensive TO–92 package which is readily adaptable for use in automatic insertion equipment.

- One–Piece, Injection–Molded Unibloc Package
- Sensitive Gate Triggering in Four Trigger Modes for all possible Combinations of Trigger Sources, and Especially for Circuits that Source Gate Drives
- All Diffused and Glassivated Junctions for Maximum Uniformity of Parameters and Reliability

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (Gate Open, T_J = –40 to +110°C)(1) 1/2 Sine Wave 50 to 60 Hz, Gate Open MAC97–4, MAC97A4 MAC97–6, MAC97A6 MAC97–8, MAC97A8	V_{DRM}	 200 400 600	Volts
On-State RMS Current Full Cycle Sine Wave 50 to 60 Hz (T_C = +50°C)	$I_{T(RMS)}$	0.8	Amp
Peak Non–repetitive Surge Current (One Full Cycle, 60 Hz, T_A = 110°C)	I_{TSM}	8.0	Amps
Circuit Fusing Considerations T_J = –40 to +110°C (t = 8.3 ms)	I^2t	0.26	A^2s
Peak Gate Voltage (t ≤ 2.0 μs)	V_{GM}	5.0	Volts
Peak Gate Power (t ≤ 2.0 μs)	P_{GM}	5.0	Watts
Average Gate Power (T_C = 80°C, t ≤ 8.3 ms)	$P_{G(AV)}$	0.1	Watt
Peak Gate Current (t ≤ 2.0 μs)	I_{GM}	1.0	Amp
Operating Junction Temperature Range	T_J	–40 to +110	°C
Storage Temperature Range	T_{stg}	–40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	75	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W

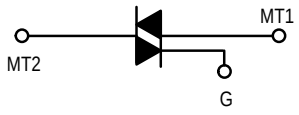
(1) V_{DRM} for all types can be applied on a continuous basis. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

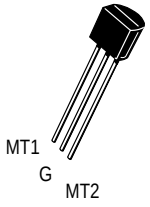
MAC97,A IMPROVED SERIES

(Device Date Code 9625 and Up)

Motorola preferred devices

TRIACs
0.8 AMPERE RMS
200 — 600 VOLTS





CASE 29–04
TO–226AA, STYLE 12
(TO–92)

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_C = 25°C, and Either Polarity of MT2 to MT1 Voltage unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Blocking Current(1) (V_D = Rated V_{DRM}, T_J = 110°C, Gate Open)	I_{RRM}	—	—	0.1	mA
Peak On-State Voltage (Either Direction) (I_{TM} = 1.1 A Peak; Pulse Width ≤ 2.0 ms, Duty Cycle ≤ 2.0%)	V_{TM}	—	—	1.65	Volts
Gate Trigger Current (Continuous dc) (V_D = 12 Vdc, R_L = 100 Ohms)	I_{GT}				mA
MT2(+), G(+)		—	—	10	
MT2(+), G(–)		—	—	10	
MT2(–), G(–)		—	—	10	
MT2(–), G(+) MAC97		—	—	10	
MT2(+), G(+)		—	—	5.0	
MT2(+), G(–)		—	—	5.0	
MT2(–), G(–)		—	—	5.0	
MT2(–), G(+) MAC97A		—	—	7.0	
Gate Trigger Voltage, (Continuous dc) (V_D = 12 Vdc, R_L = 100 Ohms)	V_{GT}				Volts
MT2(+), G(+) All Types		—	—	2.0	
MT2(+), G(–) All Types		—	—	2.0	
MT2(–), G(–) All Types		—	—	2.0	
MT2(–), G(+) All Types		—	—	2.5	
(V_D = Rated V_{DRM}, R_L = 10 k Ohms, T_J = 110°C)					
MT2(+), G(+); MT2(–), G(–); MT2(+), G(–) All Types		0.1	—	—	
MT2(–), G(+) All Types		0.1	—	—	
Holding Current (V_D = 12 Vdc, I_{TM} = 200 mA, Gate Open)	I_H	—	—	5.0	mA
Gate Controlled Turn–On Time (V_D = Rated V_{DRM}, I_{TM} = 1.0 A pk, I_G = 25 mA)	t_{gt}	—	2.0	—	μs
Critical Rate–of–Rise of Commutation Voltage (f = 250 Hz, I_{TM} = 1.0 A, Commutating di/dt = 1.5 A/mS, On–State Current Duration = 2.0 mS, V_{DRM} = 200 V, Gate Unenergized, T_C = 110°C, Gate Source Resistance = 150 Ω, See Figure 13)	dv/dt_c	1.5	—	—	V/μs
Critical Rate–of–Rise of Off State Voltage (V_{pk} = Rated V_{DRM}, T_C = 110°C, Gate Open, Exponential Method)	dv/dt	10	—	—	V/μs

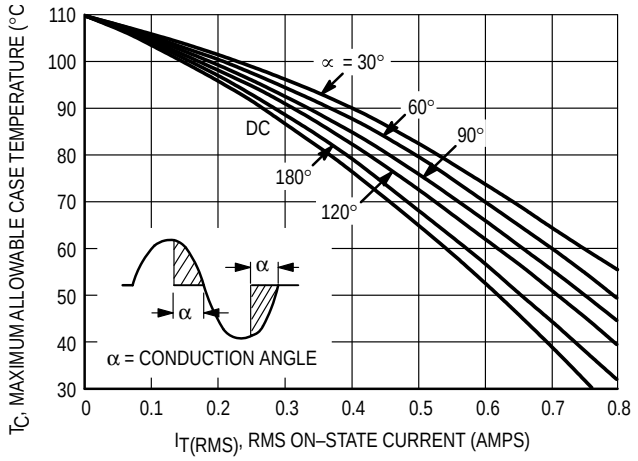


Figure 1. RMS Current Derating

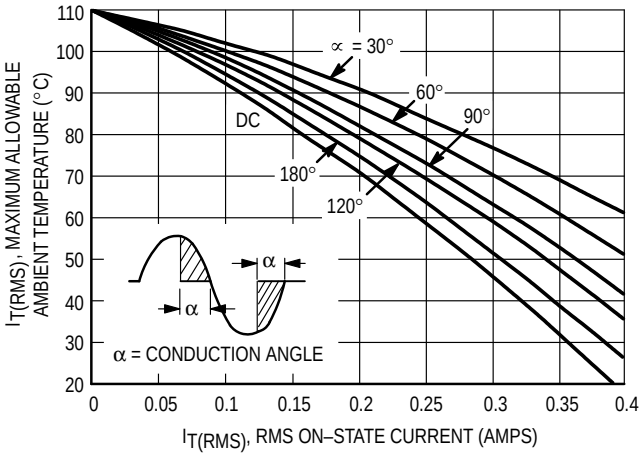


Figure 2. RMS Current Derating

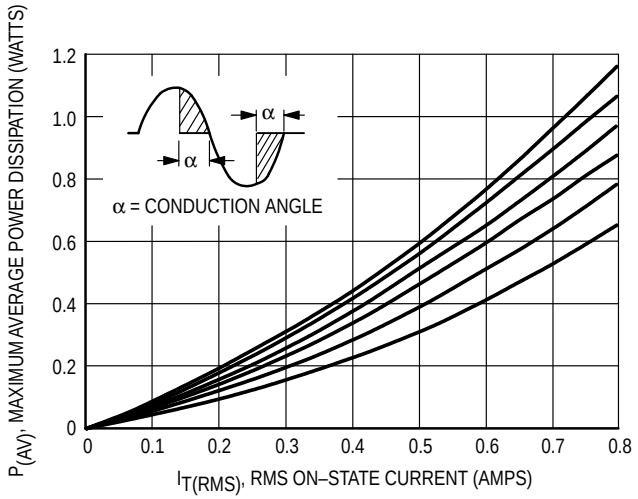


Figure 3. Power Dissipation

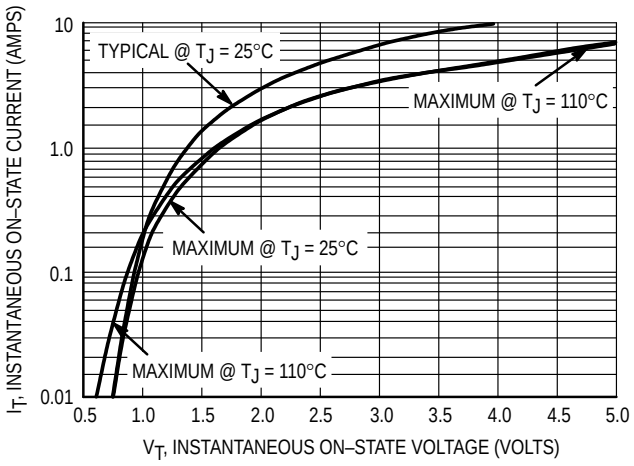


Figure 4. On–State Characteristics

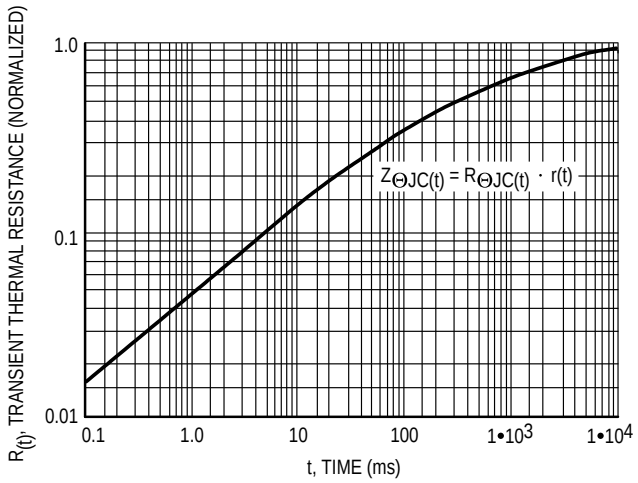


Figure 5. Transient Thermal Response

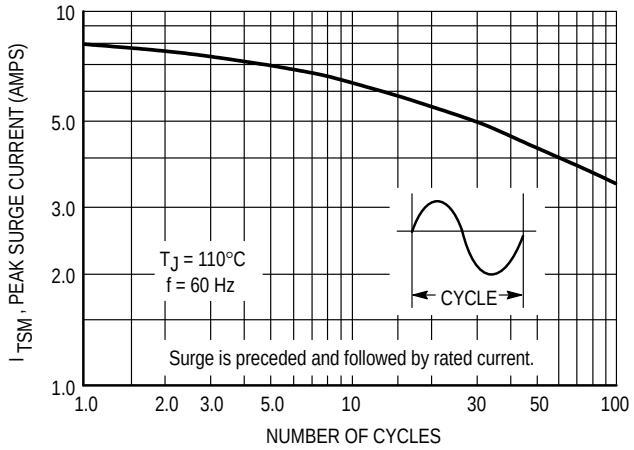


Figure 6. Maximum Allowable Surge Current

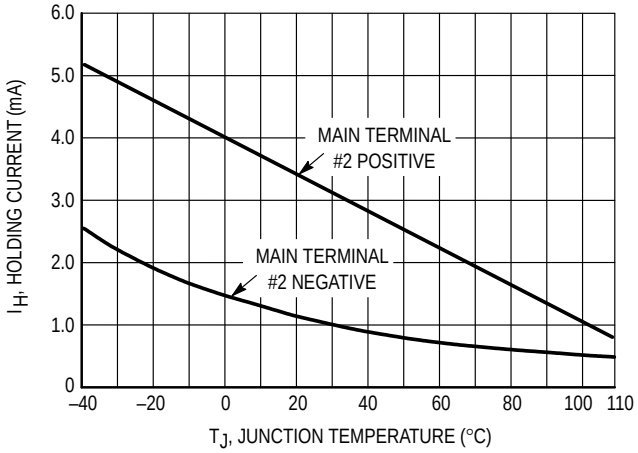


Figure 7. Typical Holding Current Variation

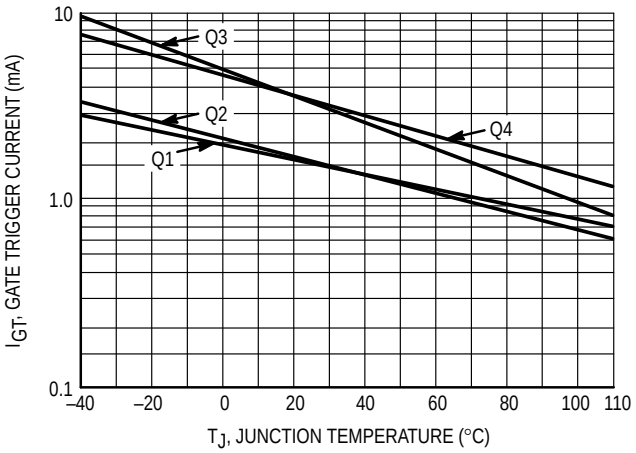


Figure 8. Typical Gate Trigger Current Variation

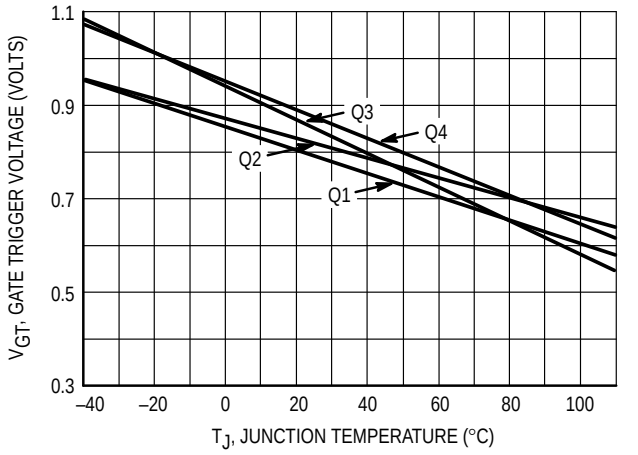


Figure 9. Gate Trigger Voltage Variation

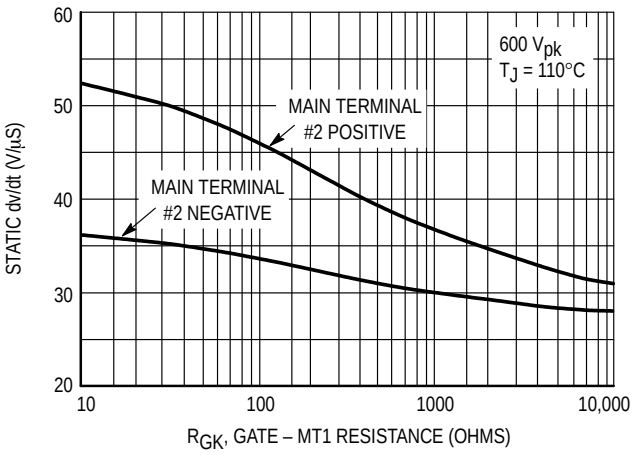


Figure 10. Exponential Static dv/dt versus Gate – MT1 Resistance

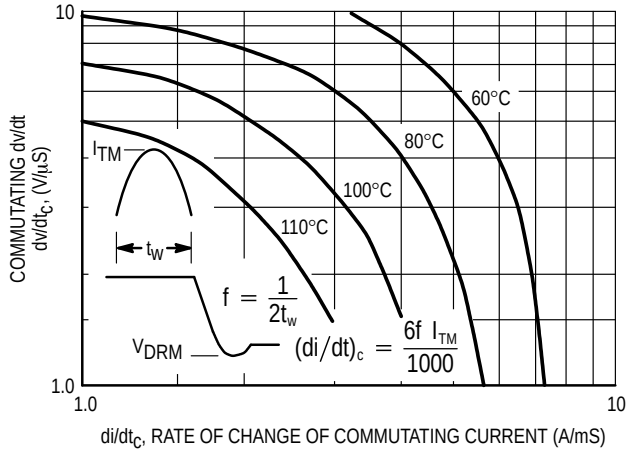


Figure 11. Typical Commutating dv/dt versus Current Crossing Rate and Junction Temperature

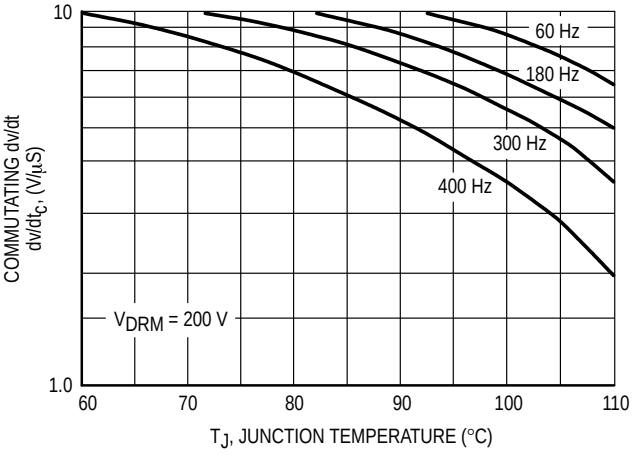
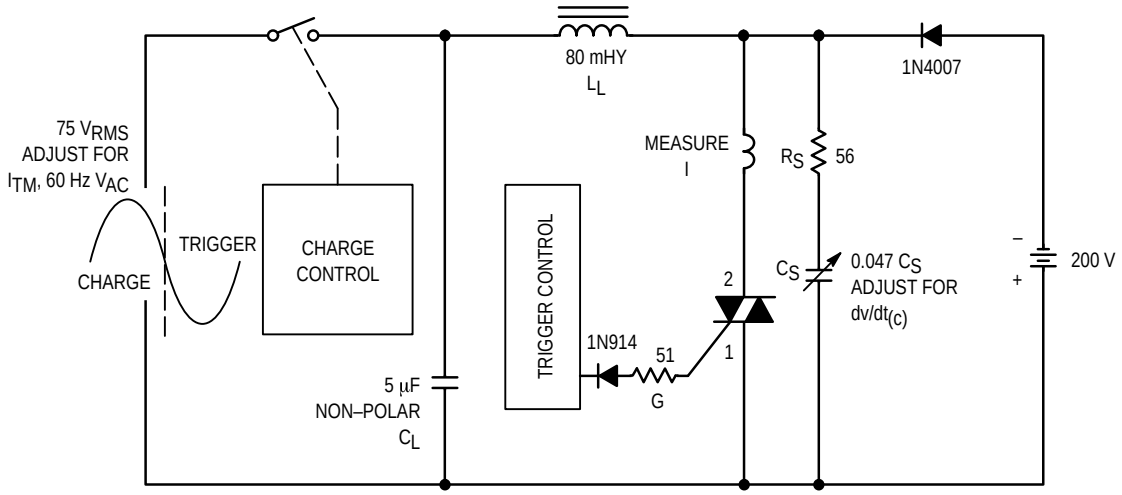


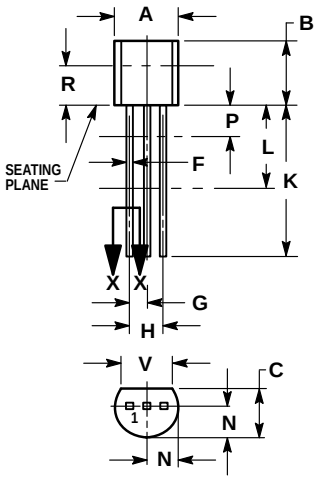
Figure 12. Typical Commutating dv/dt versus Junction Temperature at 0.8 Amps RMS



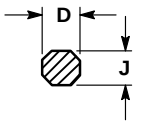
NOTE: Component values are for verification of rated $(dv/dt)_c$. See AN1048 for additional information.

Figure 13. Simplified Q_1 $(dv/dt)_c$ Test Circuit

PACKAGE DIMENSIONS



STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2



SECTION X–X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN P AND L. DIMENSION D AND J APPLY BETWEEN L AND K MINIMUM. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.022	0.41	0.55
F	0.016	0.019	0.41	0.48
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	—	12.70	—
L	0.250	—	6.35	—
N	0.080	0.105	2.04	2.66
P	—	0.100	—	2.54
R	0.115	—	2.93	—
V	0.135	—	3.43	—

CASE 29–04
(TO–226AA)
(TO–92)

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