

**MC14415**

**Quad Precision Timer/Driver**

MC14415 quad timer/driver is constructed with complementary MOS enhancement mode devices. The output pulse width of each digital timer is a function of the input clock frequency. Once the proper input sequence is detected the output buffer is set (turned on), and after 100 clock pulses are counted, the output buffer is reset (turned off).

The MC14415 was designed specifically for application in high speed line printers to provide the critical timing of the hammer drivers, but may be used in many applications requiring precision pulse widths.

- Four Precision Digital Time Delays
- Schmitt Trigger Clock Conditioning
- NPN Bipolar Output Drivers
- Timing Disable Capability Using Inhibit Output
- Positive or Negative Edge Strobing on the Inputs
- Synchronous Polynomial Counters Used for Delay Counting

**MAXIMUM RATINGS\*** (Voltages Referenced to  $V_{SS}$ )

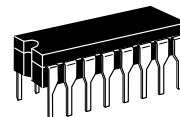
Rating	Symbol	Value	Unit
DC Supply Voltage MC14415FL, FP,DW MC14415VL, VP	$V_{DD}$	- 0.5 to + 18.0 - 0.5 to + 6.0	V
Input or Output Voltage (DC or Transient)	$V_{in}, V_{out}$	- 0.5 to $V_{DD} + 0.5$	V
Input Current (DC or Transient), per Pin	$I_{in}$	$\pm 10$	mA
Output Current (DC or Transient), per Pin	$I_{out}$	$\pm 20$	mA
Power Dissipation, per Package†	$P_D$	500	mW
Storage Temperature	$T_{stg}$	- 65 to + 150	°C
Lead Temperature (8-Second Soldering)	$T_L$	260	°C

\* Maximum Ratings are those values beyond which damage to the device may occur.

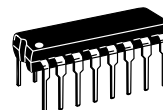
† Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

Ceramic "L" Packages: - 12 mW/°C From 100°C To 125°C



**L SUFFIX**  
CERAMIC  
CASE 620



**P SUFFIX**  
PLASTIC  
CASE 648



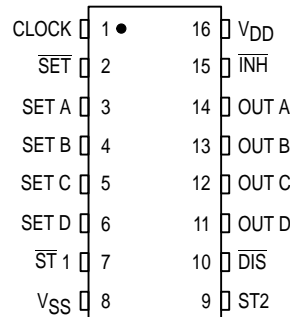
**DW SUFFIX**  
SOIC  
CASE 751G

**ORDERING INFORMATION**

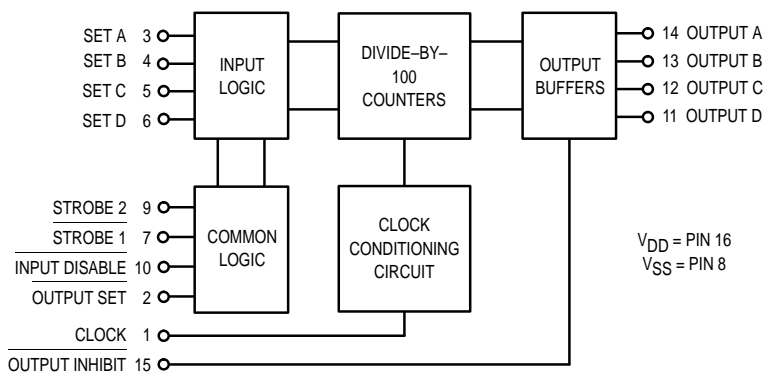
MC14415FP (3.0 V-18 V)	Plastic
MC14415VP (3.0 V-6.0 V)	Plastic
MC14415FL (3.0 V-18 V)	Ceramic
MC14415VL (3.0 V-6.0 V)	Ceramic
MC14415DW (3.0 V-18 V)	SOIC

$T_A = - 55^\circ$  to  $125^\circ\text{C}$  for all packages.

**PIN ASSIGNMENT**



**BLOCK DIAGRAM**



**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to  $V_{SS}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage (No Load)	"0" Level $V_{OL}$	5.0	—	0.01	—	0	0.01	—	0.05	Vdc
		10	—	0.01	—	0	0.01	—	0.05	
		15	—	—	—	—	—	—	—	
	"1" Level $V_{OH}$	5.0	—	—	3.0	4.14	—	—	—	
		10	—	—	8.0	9.09	—	—	—	
		15	—	—	—	14.12	—	—	—	
Noise Immunity ( $\Delta V_{out} \leq 1.5$ Vdc) ( $\Delta V_{out} \leq 3.0$ Vdc) ( $\Delta V_{out} \leq 4.5$ Vdc)	$V_{NL}$	5.0	1.5	—	1.5	2.25	—	1.4	—	Vdc
		10	3.0	—	3.0	4.50	—	2.9	—	
		15	—	—	—	6.75	—	—	—	
	$V_{NH}$	5.0	1.4	—	1.5	2.25	—	1.5	—	
		10	2.9	—	3.0	4.50	—	3.0	—	
		15	—	—	—	6.75	—	—	—	
Output Drive Voltage (NPN Driver) Source ( $I_{OH} = 0$ mA) ( $I_{OH} = 5.0$ mA) ( $I_{OH} = 10$ mA) ( $I_{OH} = 15$ mA)	$V_{OH}$	5.0	—	—	3.0	4.14	—	—	—	Vdc
			—	—	2.7	3.44	—	—	—	
			—	—	2.5	3.30	—	—	—	
			—	—	2.2	3.08	—	—	—	
	10	—	—	8.0	9.09	—	—	—	—	Vdc
		—	—	7.7	8.45	—	—	—		
		—	—	7.5	8.30	—	—	—		
		—	—	7.1	8.14	—	—	—		
	15	—	—	—	14.12	—	—	—	—	Vdc
		—	—	—	13.81	—	—	—		
		—	—	—	13.70	—	—	—		
		—	—	—	13.61	—	—	—		
Output Drive Current ( $V_{OL} = 0.4$ Vdc) ( $V_{OL} = 0.5$ Vdc) ( $V_{OL} = 1.5$ Vdc)	Sink $I_{OL}$	5.0	0.23	—	0.2	0.78	—	0.16	—	mAdc
		10	0.60	—	0.5	2.0	—	0.40	—	
		15	—	—	—	7.8	—	—	—	
		—	—	—	—	—	—	—	—	
Input Leakage Current	$I_{in}$	15	—	$\pm 0.3$	—	$\pm 0.00001$	$\pm 0.3$	—	$\pm 1.0$	$\mu$ Adc
Input Capacitance ( $V_{in} = 0$ )	$C_{in}$	—	—	—	—	5.0	—	—	—	pF
Quiescent Dissipation	$P_Q$	5.0	—	0.25	—	0.00005	0.25	—	3.5	mW
		10	—	1.0	—	0.00022	1.0	—	14	
		15	—	—	—	0.00050	—	—	—	
Power Dissipation** (Dynamic plus Quiescent) ( $C_L = 15$ pF)	$P_D$	5.0	$P_D (56 \text{ mW/MHz}) f + P_Q$							mW
		10	$P_D (225 \text{ mW/MHz}) f + P_Q$							
		15	$P_D (510 \text{ mW/MHz}) f + P_Q$							

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

\*\*The formulas given are for the typical characteristics only.

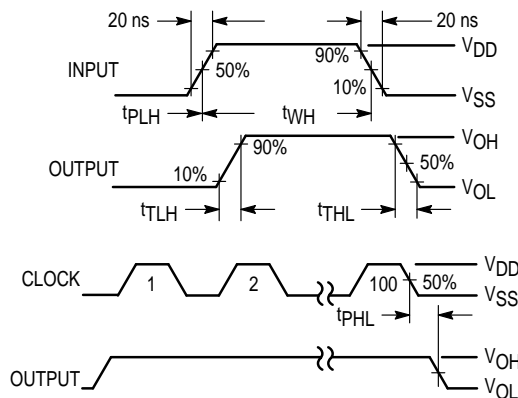
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

**SWITCHING CHARACTERISTICS\*** ( $C_L = 15 \text{ pF}$ ,  $T_A = 25^\circ\text{C}$ )

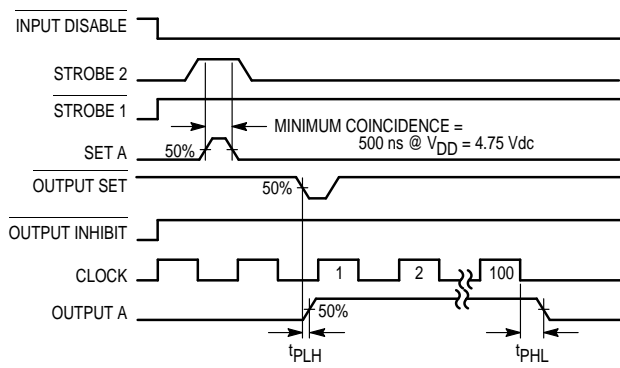
Characteristic	Symbol	V <sub>DD</sub> Vdc	Min	Typ #	Max	Unit
Output Rise Time $t_{TLH} = (2.0 \text{ ns/pF}) C_L + 10 \text{ ns}$ $t_{TLH} = (1.25 \text{ ns/pF}) C_L + 6 \text{ ns}$ $t_{TLH} = (1.10 \text{ ns/pF}) C_L + 3 \text{ ns}$	$t_{TLH}$	5.0 10 15	— — —	40 25 20	85 60 —	ns
Output Fall Time $t_{THL} = (1.5 \text{ ns/pF}) C_L + 47 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 24 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 17 \text{ ns}$	$t_{THL}$	5.0 10 15	— — —	70 35 25	150 80 —	ns
Turn-Off Delay Time $t_{PLH} = (2.7 \text{ ns/pF}) C_L + 560 \text{ ns}$ $t_{PLH} = (1.2 \text{ ns/pF}) C_L + 282 \text{ ns}$ $t_{PLH} = (0.91 \text{ ns/pF}) C_L + 286 \text{ ns}$	$t_{PLH}$	5.0 10 15	— — —	600 300 150	1200 600 —	ns
Turn-On Delay Time $t_{PHL} = (2.4 \text{ ns/pF}) C_L + 564 \text{ ns}$ $t_{PHL} = (1.0 \text{ ns/pF}) C_L + 285 \text{ ns}$ $t_{PHL} = (0.75 \text{ ns/pF}) C_L + 289 \text{ ns}$	$t_{PHL}$	5.0 10 15	— — —	600 300 150	1200 600 —	ns
Turn-On Delay Time (Inhibit to Output)	$t_{PHL}$	5.0 10 15	— — —	300 225 110	550 425 —	ns
Turn-Off Delay Time (Inhibit to Output)	$t_{PLH}$	5.0 10 15	— — —	300 225 110	550 425 —	ns
Input Pulse Coincidence (Figure 3)	PC <sub>min</sub>	5.0 10 15	500 450 —	450 350 —	— — —	ns
Input Pulse Width (Figure 1)	$t_{WH}$	5.0 10 15	500 450 —	450 350 —	— — —	ns
Input Clock Frequency	$f_{cl}$	5.0 10 15	— — —	0.7 1.0 1.5	— — —	MHz
Clock Input Rise and Fall Times (Figure 1)	$t_{TLH}$ , $t_{THL}$	5.0 10 15	— — —	— — —	15 5.0 4.0	$\mu\text{s}$

\* The formulas given are for the typical characteristics only at 25°C.

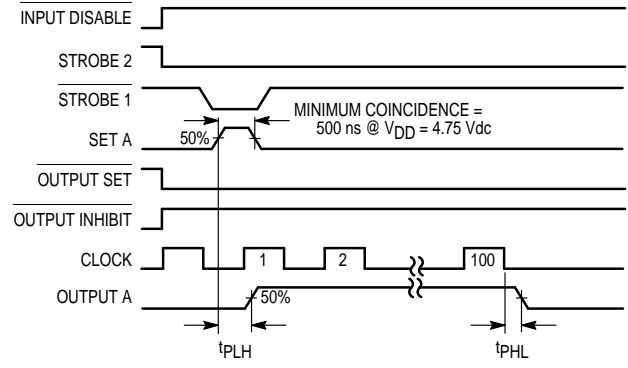
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



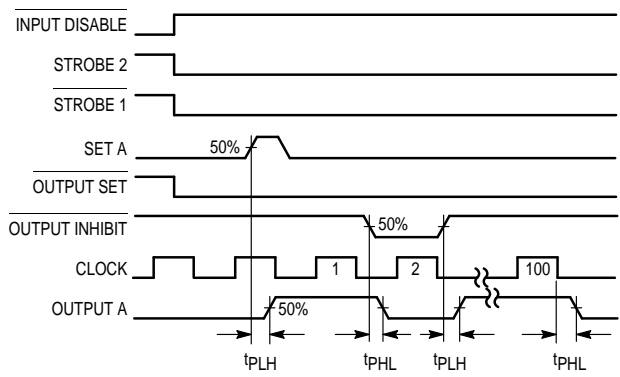
**Figure 1. Switching Characteristics — Waveform Relationships**



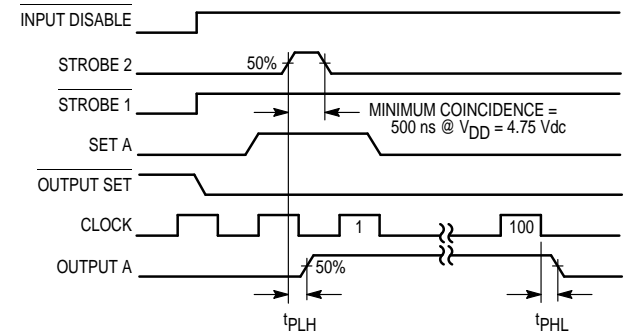
**Mode 1: OUTPUT SET Initiates Time Delay**



**Mode 2: Set A Initiates Time Delay**



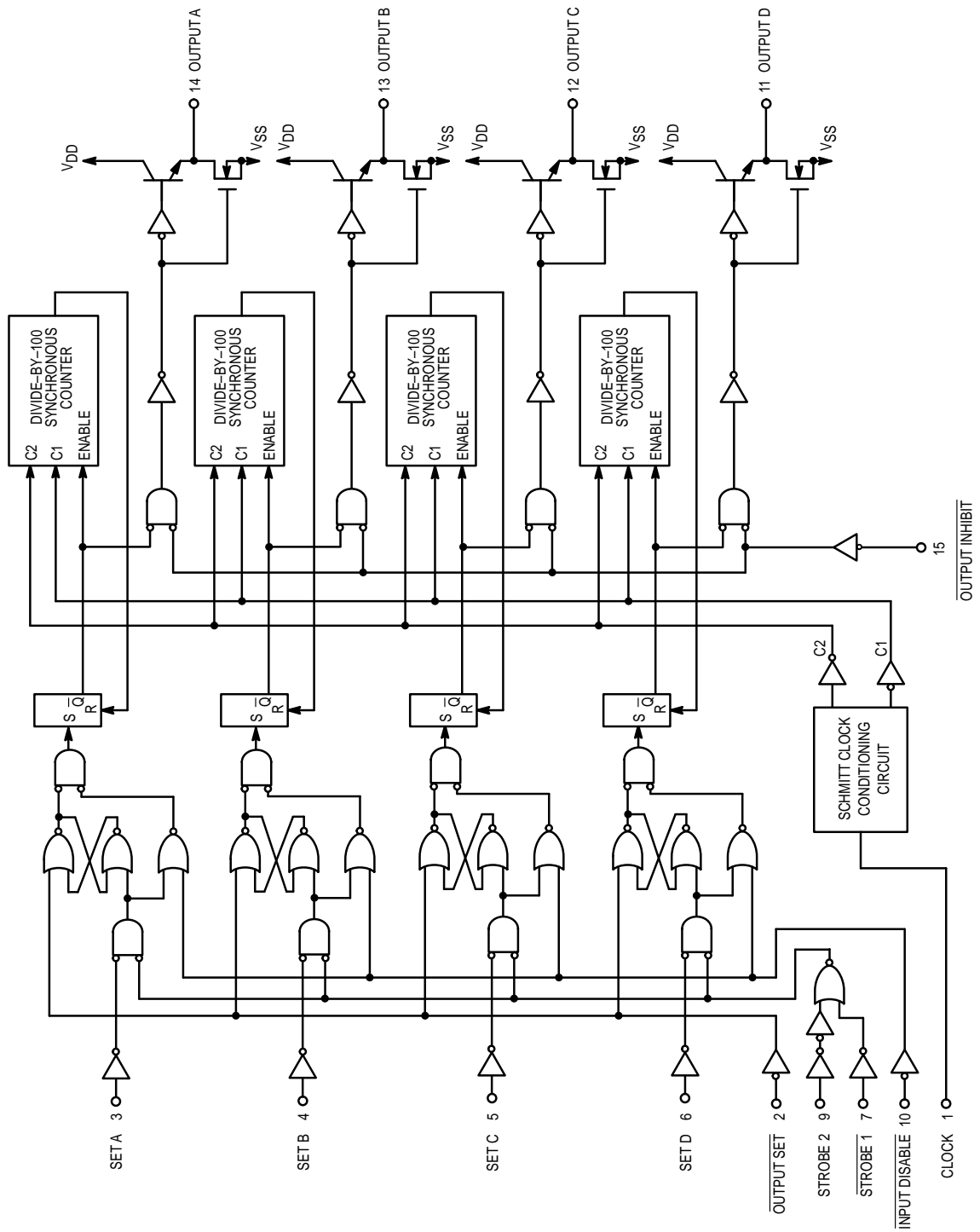
**Mode 3: OUTPUT INHIBIT Disables Time Delay**



**Mode 4: Positive-Edge Strobe (ST2) Initiates Time Delay**

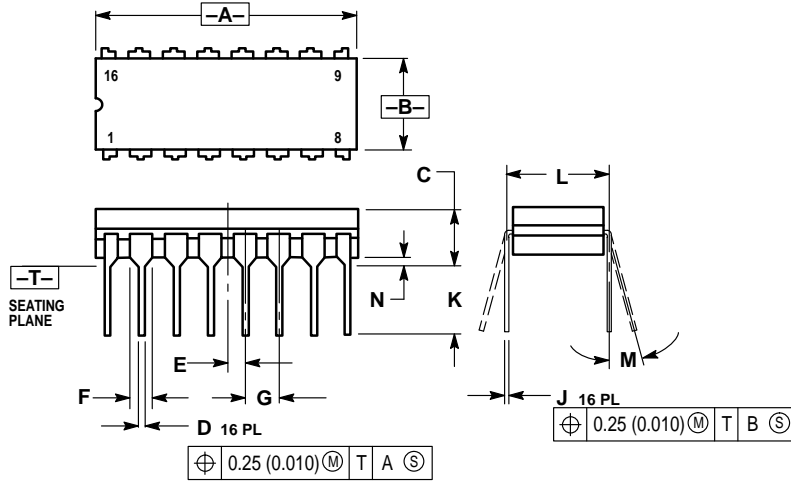
**Figure 2. Typical Operation Modes and Functional Timing Diagram**

# LOGIC DIAGRAM



## OUTLINE DIMENSIONS

### L SUFFIX CERAMIC DIP PACKAGE CASE 620-10 ISSUE V

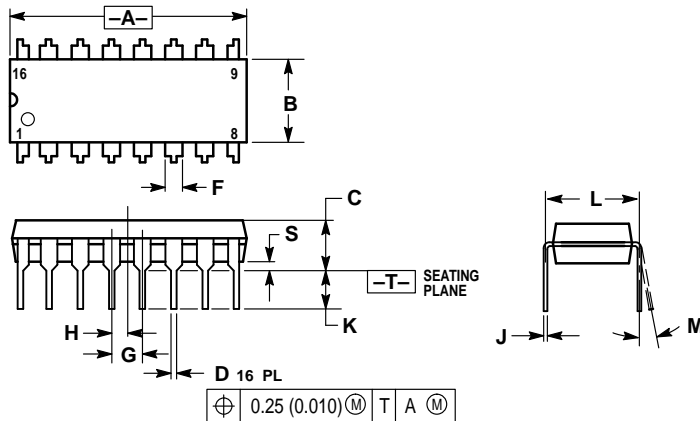


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

### P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



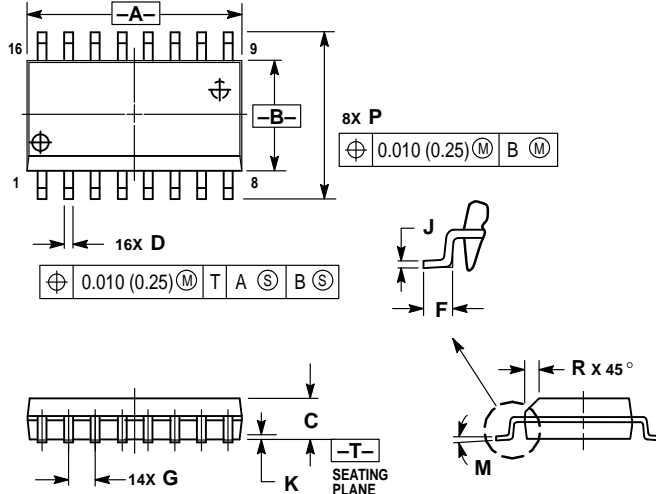
**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

## OUTLINE DIMENSIONS

### DW SUFFIX PLASTIC SOIC PACKAGE CASE 751G-02 ISSUE A



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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MC14415/D

