

Dual 2-Wide, 2-Input Expandable AND-OR-INVERT Gate

The MC14506UB is an expandable AND-OR-INVERT gate with inhibit and 3-state output. The expand option allows cascading with any other gate, which may be carried as far as desired as long as the propagation delay added with each gate is considered. For example, the second AOI gate in this device may be used to expand the first gate, giving an expanded 4-wide, 2-input AOI gate. This device is useful in data control and digital multiplexing applications.

- 3-State Output
- Separate Inhibit Line
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range

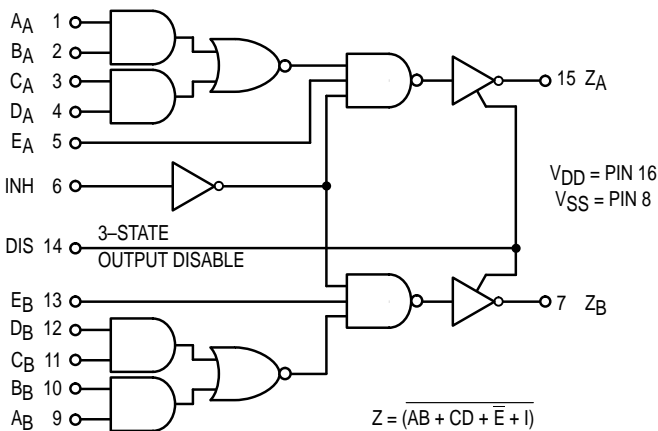
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	- 0.5 to + 18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	- 0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	- 65 to + 150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

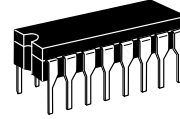
* Maximum Ratings are those values beyond which damage to the device may occur.
† Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: - 12 mW/°C From 100°C To 125°C

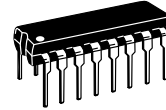
LOGIC DIAGRAM



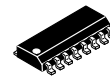
MC14506UB



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXUBCP	Plastic
MC14XXXUBCL	Ceramic
MC14XXXUBD	SOIC

T_A = - 55° to 125°C for all packages.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

TRUTH TABLE

A	B	C	D	E	Inhibit	Disable	Z
0	0	0	0	1	0	0	1
0	X	0	X	1	0	0	1
0	X	X	0	1	0	0	1
X	0	0	X	1	0	0	1
X	0	X	0	1	0	0	1
1	1	X	X	X	X	0	0
X	X	1	1	X	X	0	0
X	X	X	X	0	X	0	0
X	X	X	X	X	1	0	0
X	X	X	X	X	X	1	High Impedance

X = Don't Care



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	- 55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage V _{in} = V _{DD} or 0	"0" Level V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
	"1" Level V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95		—
			10	9.95	—	9.95	10	—	9.95		—
			15	14.95	—	14.95	15	—	14.95		—
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	"0" Level V _{IL}	5.0	—	1.0	—	2.25	1.0	—	1.0	Vdc	
		10	—	2.0	—	4.50	2.0	—	2.0		
		15	—	2.5	—	6.75	2.5	—	2.5		
	"1" Level (V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	4.0	—	4.0	2.75	—	4.0		—
			10	8.0	—	8.0	5.50	—	8.0		—
			15	12.5	—	12.5	8.25	—	12.5		—
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc	
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—		
		10	-1.6	—	-1.3	-2.25	—	-0.9	—		
	Sink I _{OL}	5.0	5.0	0.64	—	0.51	0.88	—	0.36		—
			10	1.6	—	1.3	2.25	—	0.9		—
			15	4.2	—	3.4	8.8	—	2.4		—
Input Current	I _{in}	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	μAdc	
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I _{DD}	5.0	—	1.0	—	0.002	1.0	—	30	μAdc	
		10	—	2.0	—	0.004	2.0	—	60		
		15	—	4.0	—	0.006	4.0	—	120		
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (0.6 μA/kHz) f + I _{DD}							μAdc	
		10	I _T = (1.1 μA/kHz) f + I _{DD}								
		15	I _T = (1.7 μA/kHz) f + I _{DD}								
Three-State Leakage Current	I _{TL}	15	—	± 0.1	—	± 0.0001	± 0.1	—	± 3.0	μAdc	

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

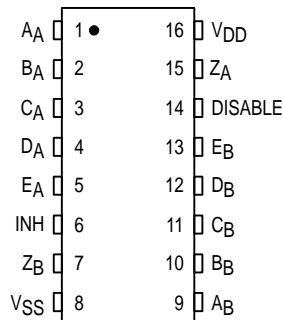
**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

PIN ASSIGNMENT



SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V _{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{TLH}, t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Data Propagation Delay Time $t_{PLH} = (1.7 \text{ ns/pF}) C_L + 210 \text{ ns}$ $t_{PLH} = (0.66 \text{ ns/pF}) C_L + 77 \text{ ns}$ $t_{PLH} = (0.5 \text{ ns/pF}) C_L + 50 \text{ ns}$ $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 185 \text{ ns}$ $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 62 \text{ ns}$ $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 40 \text{ ns}$	t_{PLH} t_{PHL}	5.0 10 15 5.0 10 15	— — — — — —	295 110 75 270 95 65	580 225 180 480 175 140	ns ns
Expand Propagation Delay Time $t_{PLH} = (1.7 \text{ ns/pF}) C_L + 95 \text{ ns}$ $t_{PLH} = (0.66 \text{ ns/pF}) C_L + 42 \text{ ns}$ $t_{PLH} = (0.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 115 \text{ ns}$ $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 47 \text{ ns}$ $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 30 \text{ ns}$	t_{PLH} t_{PHL}	5.0 10 15 5.0 10 15	— — — — — —	180 75 50 200 80 55	430 160 125 330 110 90	ns ns
Inhibit Propagation Delay Time $t_{PLH} = (1.7 \text{ ns/pF}) C_L + 135 \text{ ns}$ $t_{PLH} = (0.66 \text{ ns/pF}) C_L + 67 \text{ ns}$ $t_{PLH} = (0.5 \text{ ns/pF}) C_L + 40 \text{ ns}$ $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 145 \text{ ns}$ $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 62 \text{ ns}$ $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 35 \text{ ns}$	t_{PLH} t_{PHL}	5.0 10 15 5.0 10 15	— — — — — —	220 100 65 230 95 60	500 225 160 400 175 150	ns ns
3-State Propagation Delay Time "1" to High Impedance "0" to High Impedance High Impedance to "1" High Impedance to "0"	t_{PHZ} t_{PLZ} t_{PZH} t_{PZL}	5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15	— — — — — — — — — — — —	60 45 35 90 55 40 110 50 40 170 70 50	150 110 90 225 140 100 300 125 100 425 175 125	ns ns ns ns

* The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

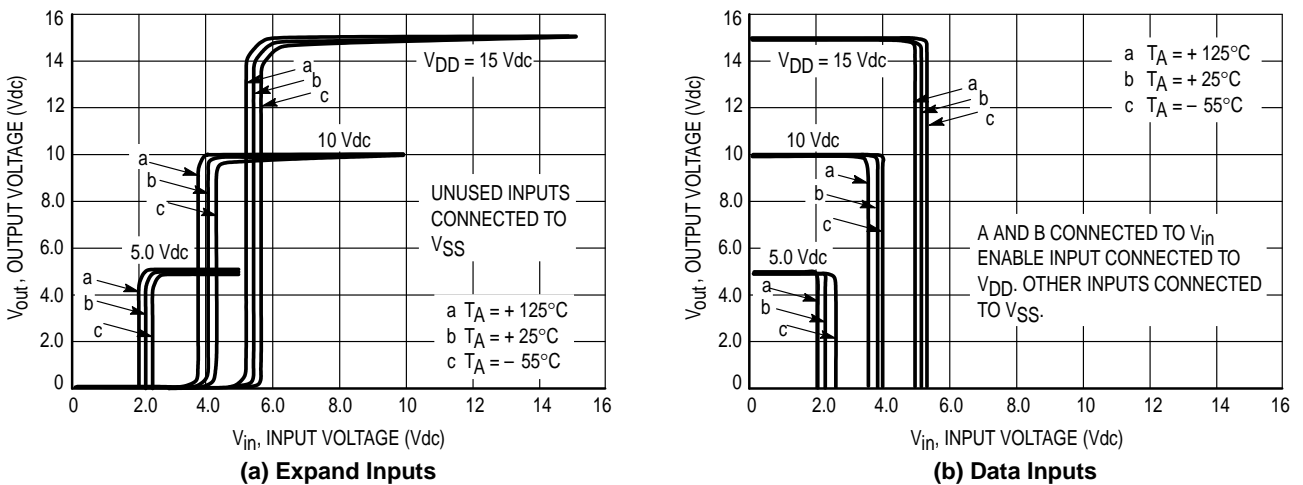


Figure 1. Typical Voltage Transfer Characteristics

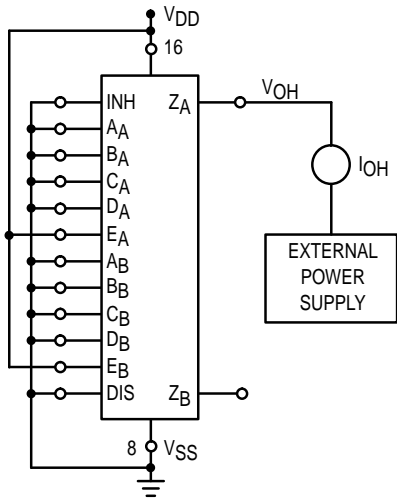


Figure 2. Typical Output Source Characteristics Test Circuit

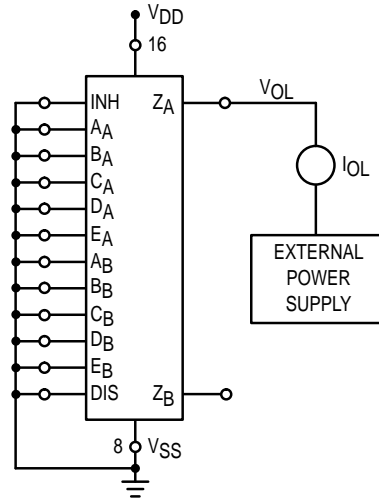


Figure 3. Typical Output Sink Characteristics Test Circuit

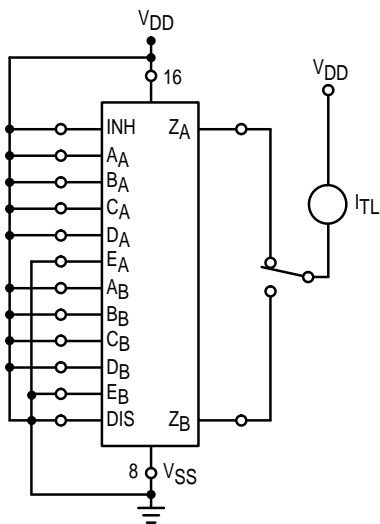


Figure 4. 3-State Leakage Current Test Circuit

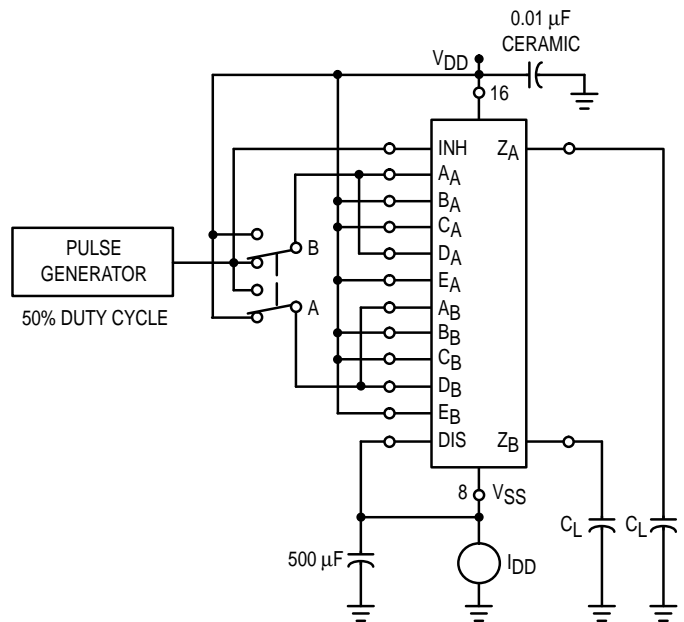


Figure 5. Typical Power Dissipation Test Circuit

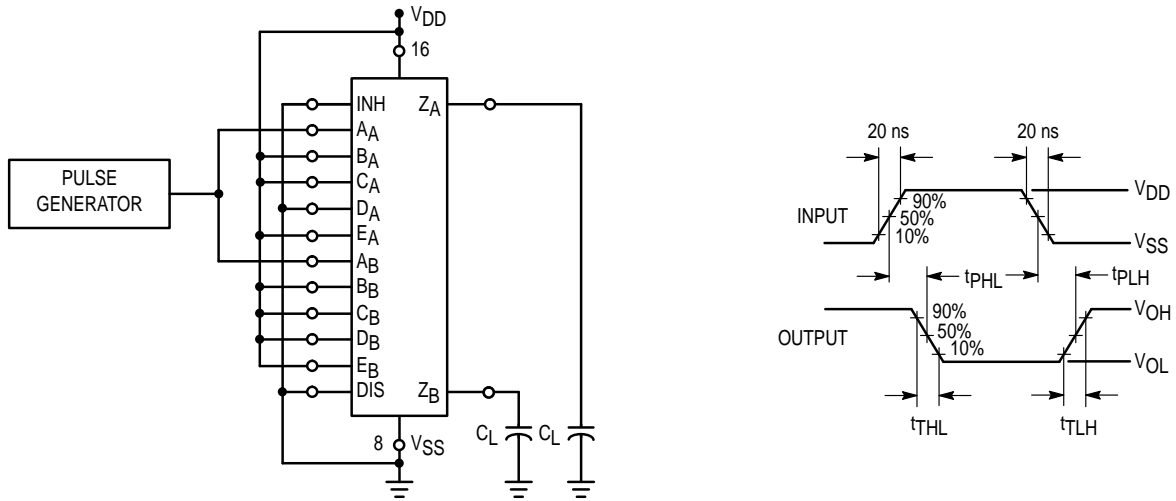
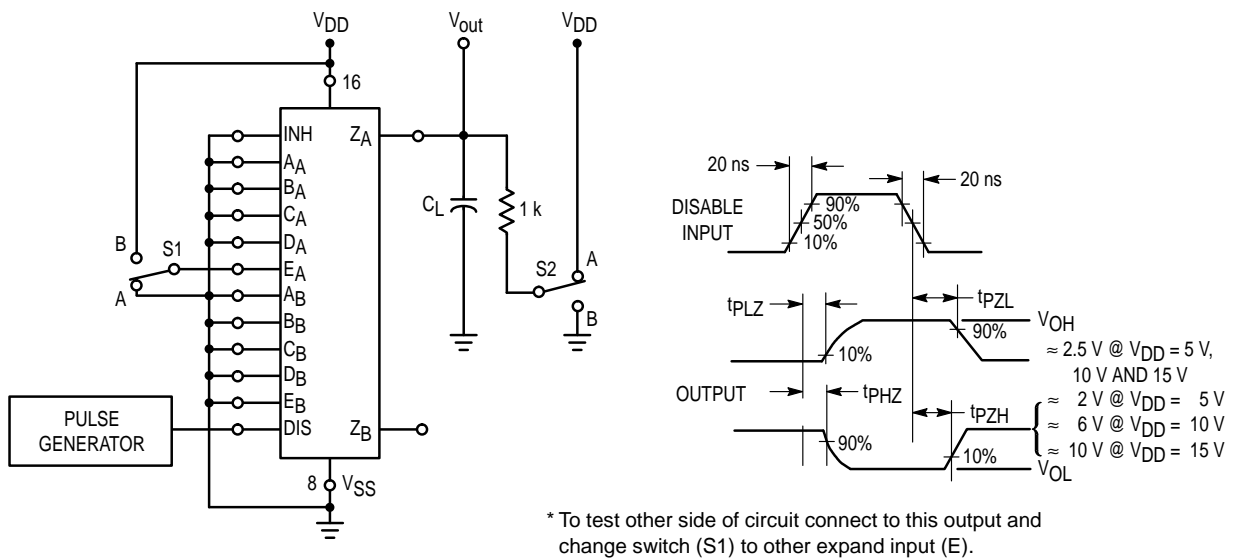


Figure 6. Switching Time Test Circuit and Waveforms (Data Inputs)



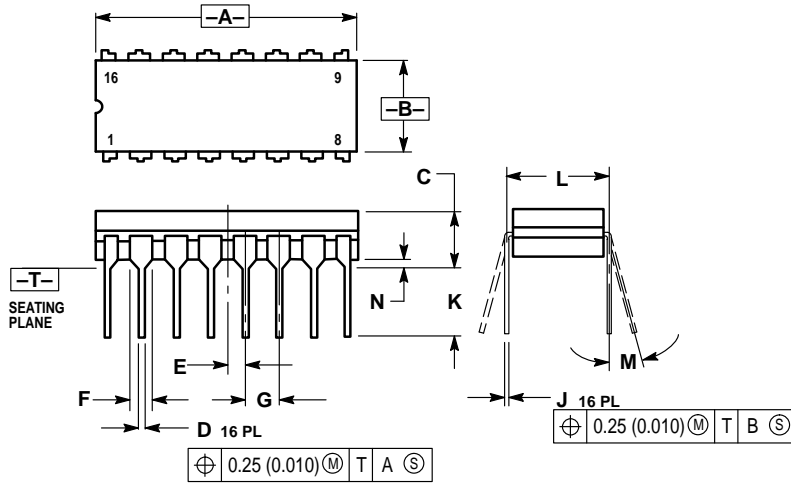
SWITCH POSITIONS

TEST	S1	S2
t _{PLZ}	A	A
t _{PHZ}	B	B
t _{PZL}	A	A
t _{PZH}	B	B

Figure 7. Switching Time Test Circuit and Waveforms (For 3-State Output)

OUTLINE DIMENSIONS

L SUFFIX CERAMIC DIP PACKAGE CASE 620-10 ISSUE V

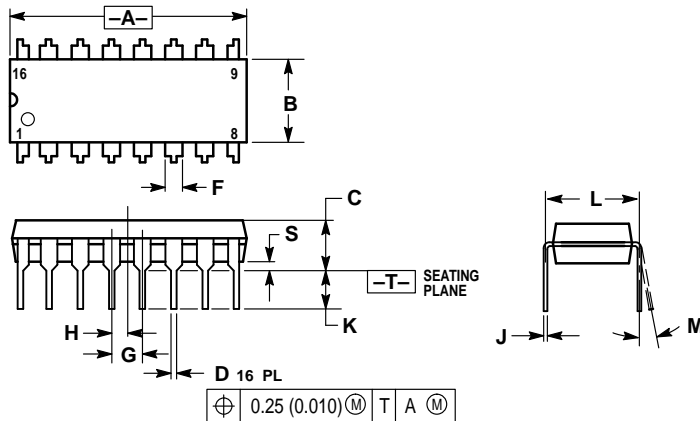


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



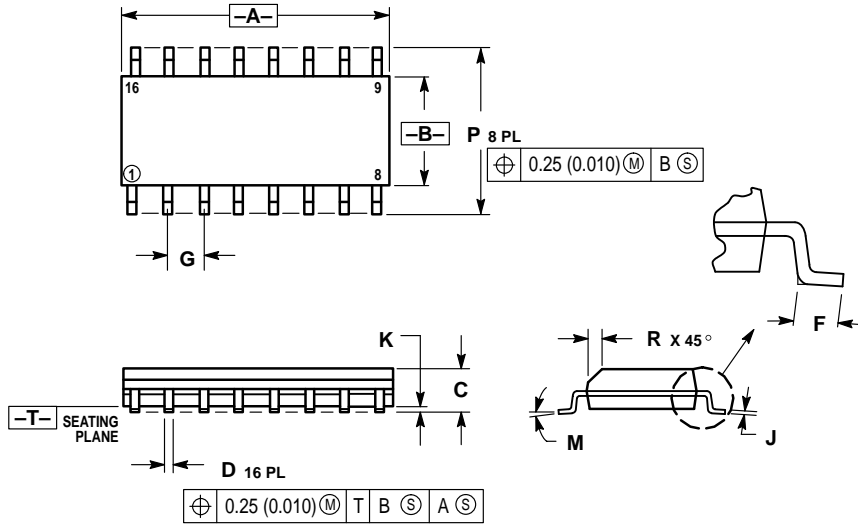
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

OUTLINE DIMENSIONS

D SUFFIX PLASTIC SOIC PACKAGE CASE 751B-05 ISSUE J



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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MC14506UB/D

