

Dual 4-Bit Latch

The MC14508B dual 4-bit latch is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The part consists of two identical, independent 4-bit latches with separate Strobe (ST) and Master Reset (MR) controls. Separate Disable inputs force the outputs to a high impedance state and allow the devices to be used in time sharing bus line applications.

These complementary MOS latches find primary use in buffer storage, holding register, or general digital logic functions where low power dissipation and/or high noise immunity is desired.

- 3-State Output
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load over the Rated Temperature Range

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

| Symbol | Parameter | Value | Unit |
|------------------------------------|--|--------------------------------|------|
| V _{DD} | DC Supply Voltage | - 0.5 to + 18.0 | V |
| V _{in} , V _{out} | Input or Output Voltage (DC or Transient) | - 0.5 to V _{DD} + 0.5 | V |
| I _{in} , I _{out} | Input or Output Current (DC or Transient), per Pin | ± 10 | mA |
| P _D | Power Dissipation, per Package† | 500 | mW |
| T _{stg} | Storage Temperature | - 65 to + 150 | °C |
| T _L | Lead Temperature (8-Second Soldering) | 260 | °C |

* Maximum Ratings are those values beyond which damage to the device may occur.

† Temperature Derating:

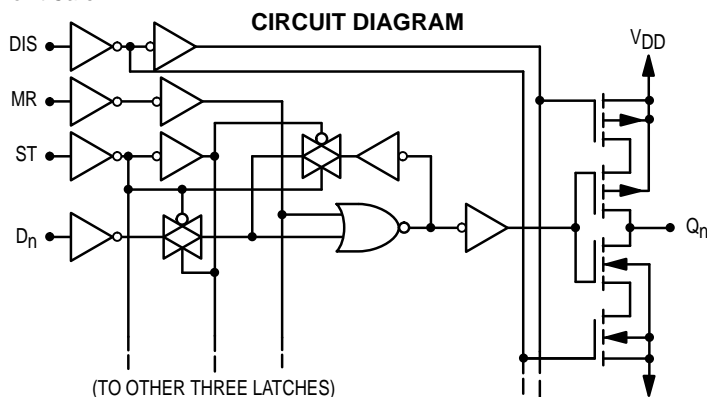
Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

Ceramic "L" Packages: - 12 mW/°C From 100°C To 125°C

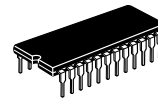
TRUTH TABLE

| MR | ST | Disable | D3 | D2 | D1 | D0 | Q3 | Q2 | Q1 | Q0 |
|----|----|---------|----|----|----|----|----------------|----|----|----|
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | X | X | X | X | Latched | | | |
| 1 | X | 0 | X | X | X | X | 0 | 0 | 0 | 0 |
| X | X | 1 | X | X | X | X | High Impedance | | | |

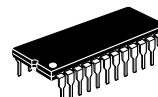
X = Don't Care



MC14508B



L SUFFIX
CERAMIC
CASE 623



P SUFFIX
PLASTIC
CASE 709



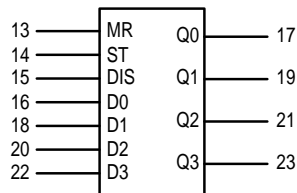
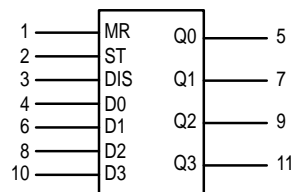
DW SUFFIX
SOIC
CASE 751E

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBDW SOIC

T_A = - 55° to 125°C for all packages.

BLOCK DIAGRAM



V_{DD} = PIN 24
V_{SS} = PIN 12



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

| Characteristic | Symbol | V_{DD} Vdc | - 55°C | | 25°C | | | 125°C | | Unit |
|---|---------------------------|-----------------|---|-----------|--------|---------------|-----------|--------|-----------|-----------|
| | | | Min | Max | Min | Typ # | Max | Min | Max | |
| Output Voltage $V_{in} = V_{DD}$ or 0 $V_{in} = 0$ or V_{DD} | "0" Level V_{OL} | 5.0 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | Vdc |
| | | 10 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | |
| | | 15 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | |
| | "1" Level V_{OH} | 5.0 | 4.95 | — | 4.95 | 5.0 | — | 4.95 | — | Vdc |
| | | 10 | 9.95 | — | 9.95 | 10 | — | 9.95 | — | |
| | | 15 | 14.95 | — | 14.95 | 15 | — | 14.95 | — | |
| Input Voltage ($V_O = 4.5$ or 0.5 Vdc) ($V_O = 9.0$ or 1.0 Vdc) ($V_O = 13.5$ or 1.5 Vdc) ($V_O = 0.5$ or 4.5 Vdc) ($V_O = 1.0$ or 9.0 Vdc) ($V_O = 1.5$ or 13.5 Vdc) | "0" Level V_{IL} | 5.0 | — | 1.5 | — | 2.25 | 1.5 | — | 1.5 | Vdc |
| | | 10 | — | 3.0 | — | 4.50 | 3.0 | — | 3.0 | |
| | | 15 | — | 4.0 | — | 6.75 | 4.0 | — | 4.0 | |
| | "1" Level V_{IH} | 5.0 | 3.5 | — | 3.5 | 2.75 | — | 3.5 | — | Vdc |
| | | 10 | 7.0 | — | 7.0 | 5.50 | — | 7.0 | — | |
| | | 15 | 11 | — | 11 | 8.25 | — | 11 | — | |
| Output Drive Current ($V_{OH} = 2.5$ Vdc) ($V_{OH} = 4.6$ Vdc) ($V_{OH} = 9.5$ Vdc) ($V_{OH} = 13.5$ Vdc) ($V_{OL} = 0.4$ Vdc) ($V_{OL} = 0.5$ Vdc) ($V_{OL} = 1.5$ Vdc) | Source I_{OH} | 5.0 | - 3.0 | — | - 2.4 | - 4.2 | — | - 1.7 | — | mAdc |
| | | 5.0 | - 0.64 | — | - 0.51 | - 0.88 | — | - 0.36 | — | |
| | | 10 | - 1.6 | — | - 1.3 | - 2.25 | — | - 0.9 | — | |
| | | 15 | - 4.2 | — | - 3.4 | - 8.8 | — | - 2.4 | — | |
| | Sink I_{OL} | 5.0 | 0.64 | — | 0.51 | 0.88 | — | 0.36 | — | mAdc |
| | | 10 | 1.6 | — | 1.3 | 2.25 | — | 0.9 | — | |
| 15 | 4.2 | — | 3.4 | 8.8 | — | 2.4 | — | — | | |
| Input Current | I_{in} | 15 | — | ± 0.1 | — | ± 0.00001 | ± 0.1 | — | ± 1.0 | μ Adc |
| Input Capacitance ($V_{in} = 0$) | C_{in} | — | — | — | — | 5.0 | 7.5 | — | — | pF |
| Quiescent Current (Per Package) | I_{DD} | 5.0 | — | 5.0 | — | 0.005 | 5.0 | — | 150 | μ Adc |
| | | 10 | — | 10 | — | 0.010 | 10 | — | 300 | |
| | | 15 | — | 20 | — | 0.015 | 20 | — | 600 | |
| Total Supply Current**† (Dynamic plus Quiescent, Per Package) ($C_L = 50$ pF on all outputs, all buffers switching) | I_T | 5.0 | $I_T = (1.46 \mu\text{A/kHz}) f + I_{DD}$ | | | | | | | μ Adc |
| | | 10 | $I_T = (2.91 \mu\text{A/kHz}) f + I_{DD}$ | | | | | | | |
| | | 15 | $I_T = (4.37 \mu\text{A/kHz}) f + I_{DD}$ | | | | | | | |
| Three-State Leakage Current | I_{TL} | 15 | — | ± 0.1 | — | ± 0.0001 | ± 0.1 | — | ± 3.0 | μ Adc |

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and $k = 0.008$.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

| Characteristic | Symbol | V_{DD} | All Types | | | Unit |
|--|-----------------------|-----------------|------------------|-----------------|-------------------|------|
| | | | Min | Typ # | Max | |
| Output Rise and Fall Time t_{TLH} , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ t_{TLH} , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ t_{TLH} , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$ | t_{TLH} , t_{THL} | 5.0 10 15 | — — — | 100 50 40 | 200 100 80 | ns |
| Propagation Delay Time, Dn or MR to Q t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 135 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 57 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 35 \text{ ns}$ | t_{PLH} , t_{PHL} | 5.0 10 15 | — — — | 220 90 60 | 440 180 120 | ns |
| Master Reset Pulse Width | $t_{WH(R)}$ | 5.0 10 15 | 200 100 70 | 100 50 35 | — — — | ns |
| Master Reset Removal Time | t_{rem} | 5.0 10 15 | 30 25 20 | -15 0 0 | — — — | ns |
| Strobe Pulse Width | $t_{WH(S)}$ | 5.0 10 15 | 140 70 40 | 70 35 20 | — — — | ns |
| Setup Time Data to Strobe | t_{su} | 5.0 10 15 | 50 20 10 | 25 10 5.0 | — — — | ns |
| Hold Time Strobe to Data | t_h | 5.0 10 15 | 50 35 35 | 20 10 10 | — — — | ns |
| 3-State Propagation Delay Time Output "1" to High Impedance | t_{PHZ} | 5.0 10 15 | — — — | 55 35 30 | 170 100 70 | ns |
| Output "0" to High Impedance | t_{PLZ} | 5.0 10 15 | — — — | 75 40 35 | 170 100 70 | |
| High Impedance to "1" Level | t_{PZH} | 5.0 10 15 | — — — | 80 35 30 | 170 100 70 | |
| High Impedance to "0" Level | t_{PZL} | 5.0 10 15 | — — — | 105 50 35 | 210 100 70 | |

* The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

PIN ASSIGNMENT

| | | | |
|----------|----|----|----------|
| MR_A | 1 | 24 | V_{DD} |
| ST_A | 2 | 23 | $Q3_B$ |
| DIS_A | 3 | 22 | $D3_B$ |
| $D0_A$ | 4 | 21 | $Q2_B$ |
| $Q0_A$ | 5 | 20 | $D2_B$ |
| $D1_A$ | 6 | 19 | $Q1_B$ |
| $Q1_A$ | 7 | 18 | $D1_B$ |
| $D2_A$ | 8 | 17 | $Q0_B$ |
| $Q2_A$ | 9 | 16 | $D0_B$ |
| $D3_A$ | 10 | 15 | DIS_B |
| $Q3_A$ | 11 | 14 | ST_B |
| V_{SS} | 12 | 13 | MR_B |

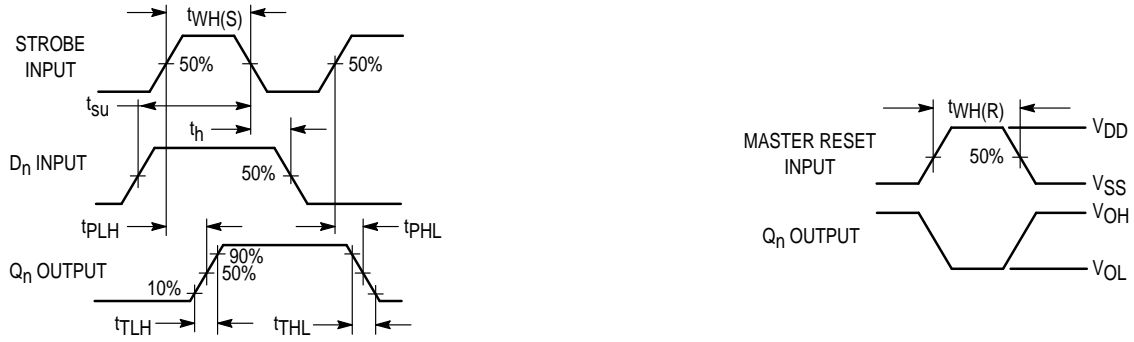
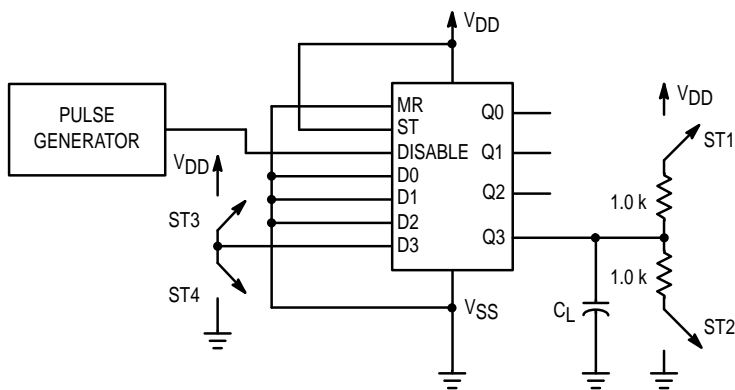


Figure 1. AC Waveforms



| Test | ST1 | ST2 | ST3 | ST4 |
|------|-------|-------|-------|-------|
| tPHZ | Open | Close | Close | Open |
| tPLZ | Close | Open | Open | Close |
| tPZL | Close | Open | Open | Close |
| tPZH | Open | Close | Close | Open |

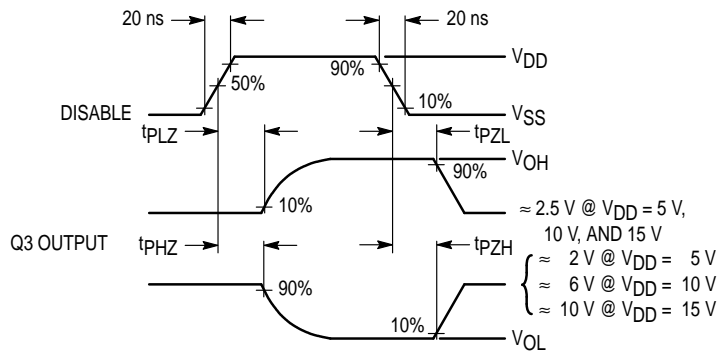


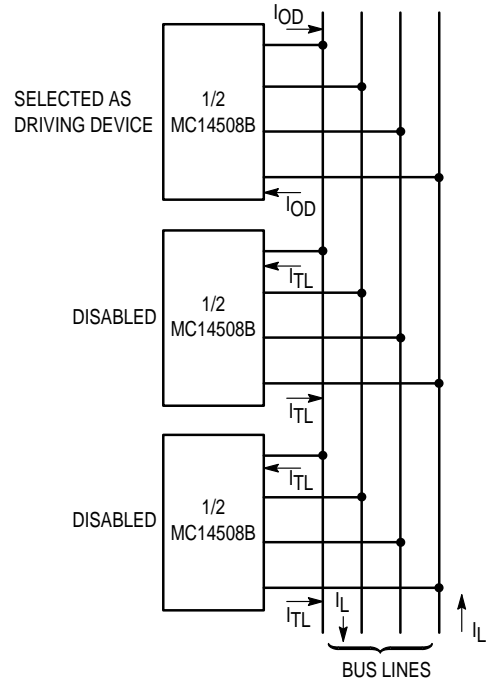
Figure 2. 3-State AC Test Circuit and Waveforms

3-STATE MODE OF OPERATION

The MC14508B can be used in bussed systems as shown. The output terminals of N 4-bit latches can be directly wired to a bus line, and to one of the 4-bit latches selected. The selected latch controls the logic state of the bus line and the remaining (N-1) 4-bit latches are disabled into a high impedance "off" state. The number of latches, N, which may be connected to a bus line is determined from the output drive current, I_{OD} , the 3-state or disabled output leakage current, I_{TL} , and the load current, I_L , required to drive the bus line (including fanout to other device inputs) and can be calculated by the following:

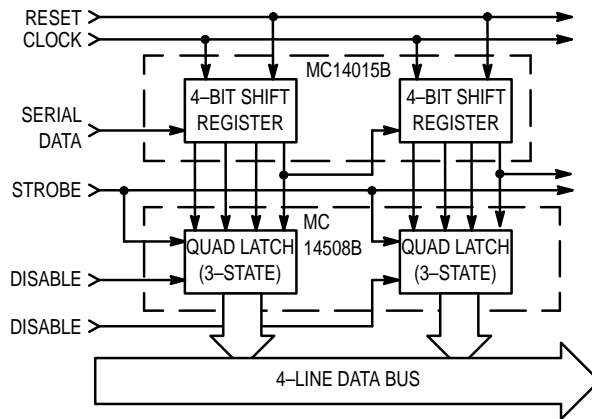
$$N = \frac{I_{OD} - I_L}{I_{TL}} + 1$$

N must be calculated for both high and low logic states of the bus line.

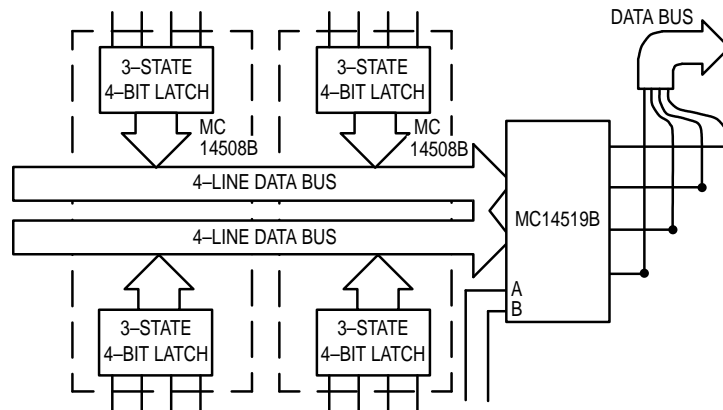


TYPICAL 3-STATE APPLICATIONS

EXAMPLE 1

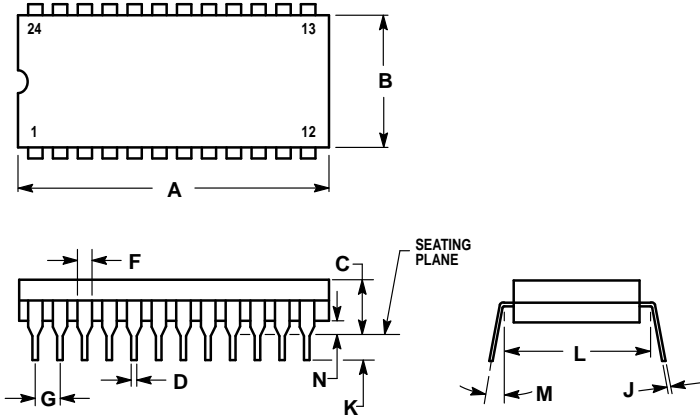


EXAMPLE 2



OUTLINE DIMENSIONS

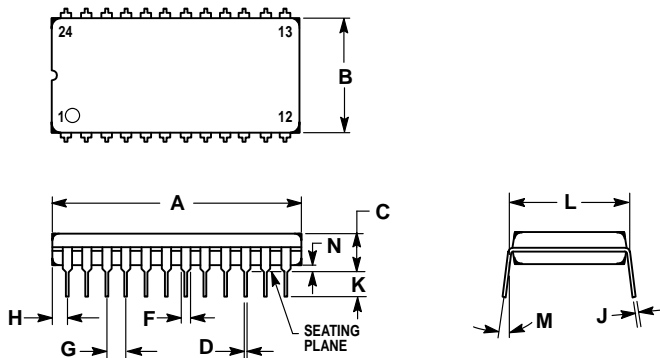
L SUFFIX CERAMIC DIP PACKAGE CASE 623-05 ISSUE M



- NOTES:
1. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 2. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (WHEN FORMED PARALLEL).

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 31.24 | 32.77 | 1.230 | 1.290 |
| B | 12.70 | 15.49 | 0.500 | 0.610 |
| C | 4.06 | 5.59 | 0.160 | 0.220 |
| D | 0.41 | 0.51 | 0.016 | 0.020 |
| F | 1.27 | 1.52 | 0.050 | 0.060 |
| G | 2.54 BSC | | 0.100 BSC | |
| J | 0.20 | 0.30 | 0.008 | 0.012 |
| K | 3.18 | 4.06 | 0.125 | 0.160 |
| L | 15.24 BSC | | 0.600 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.51 | 1.27 | 0.020 | 0.050 |

P SUFFIX PLASTIC DIP PACKAGE CASE 709-02 ISSUE C

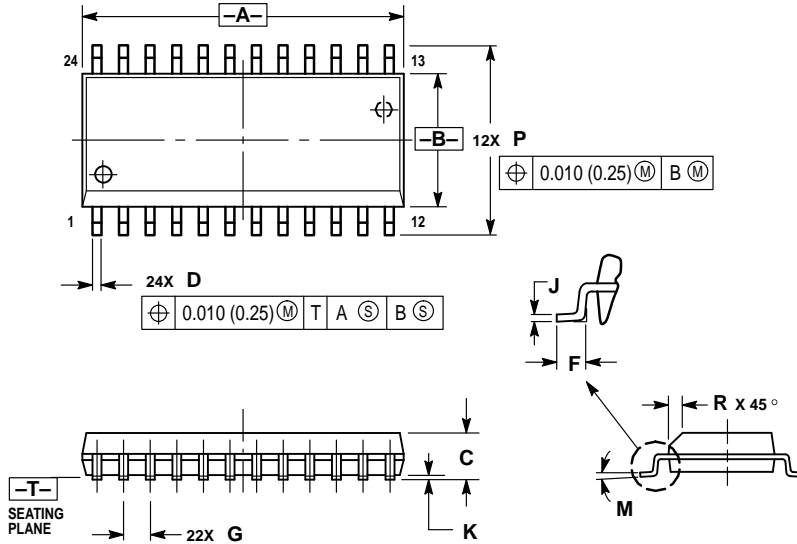


- NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
 2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 31.37 | 32.13 | 1.235 | 1.265 |
| B | 13.72 | 14.22 | 0.540 | 0.560 |
| C | 3.94 | 5.08 | 0.155 | 0.200 |
| D | 0.36 | 0.56 | 0.014 | 0.022 |
| F | 1.02 | 1.52 | 0.040 | 0.060 |
| G | 2.54 BSC | | 0.100 BSC | |
| H | 1.65 | 2.03 | 0.065 | 0.080 |
| J | 0.20 | 0.38 | 0.008 | 0.015 |
| K | 2.92 | 3.43 | 0.115 | 0.135 |
| L | 15.24 BSC | | 0.600 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.51 | 1.02 | 0.020 | 0.040 |

OUTLINE DIMENSIONS

DW SUFFIX PLASTIC SOIC PACKAGE CASE 751E-04 ISSUE E



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 15.25 | 15.54 | 0.601 | 0.612 |
| B | 7.40 | 7.60 | 0.292 | 0.299 |
| C | 2.35 | 2.65 | 0.093 | 0.104 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.41 | 0.90 | 0.016 | 0.035 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.23 | 0.32 | 0.009 | 0.013 |
| K | 0.13 | 0.29 | 0.005 | 0.011 |
| M | 0° | 8° | 0° | 8° |
| P | 10.05 | 10.55 | 0.395 | 0.415 |
| R | 0.25 | 0.75 | 0.010 | 0.029 |

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MC14508B/D

