Dual Binary to 1-of-4 Decoder/Demultiplexer

MC14555B
MC14556B

The MC14555B and MC14556B are constructed with complementary MOS (CMOS) enhancement mode devices. Each Decoder/Demultiplexer has two select inputs (A and B), an active low Enable input (E), and four mutually exclusive outputs (Q0, Q1, Q2, Q3). The MC14555B has the selected output go to the "high" state, and the MC14556B has the selected output go to the "low" state. Expanded decoding such as binary–to–hexadecimal (1–of–16), etc., can be achieved by using other MC14555B or MC14556B devices.

Applications include code conversion, address decoding, memory selection control, and demultiplexing (using the Enable input as a data input) in digital data transmission systems.

- Diode Protection on All Inputs
- Active High or Active Low Outputs
- Expandable
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low–Power TTL Loads or One Low–Power Schottky TTL Load Over the Rated Temperature Range

L SUFFIX
CERAMIC
CASE 620

P SUFFIX
PLASTIC
CASE 648

D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic
MC14XXXBD	SOIC

$T_A = -55°$ to $125°C$ for all packages.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

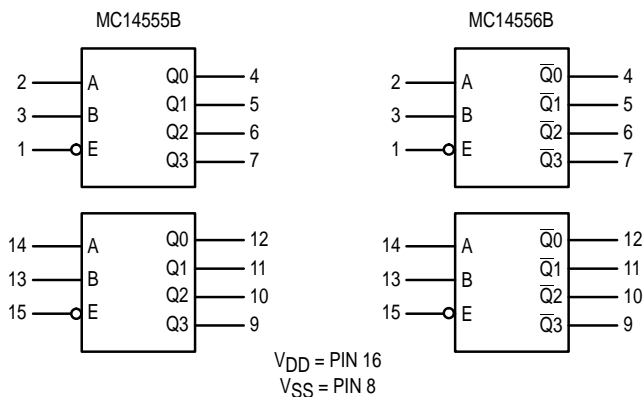| Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to $+18.0$	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	-65 to $+150$	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
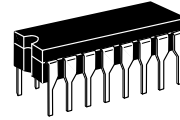† Temperature Derating:
   "P and D/DW" Packages: -7.0 mW/C From $65°C$ To $125°C$ Ceramic
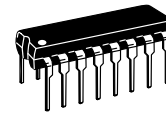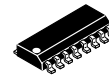   "L" Packages: -12 mW/$°C$ From $100°C$ To $125°C$

TRUTH TABLE

Inputs			Outputs							
Enable	Select		MC14555B				MC14556B			
E	B	A	Q3	Q2	Q1	Q0	Q3	Q2	Q1	Q0
0	0	0	0	0	0	1	1	1	1	0
0	0	1	0	0	1	0	1	1	0	1
0	1	0	0	1	0	0	1	0	1	1
0	1	1	1	0	0	0	0	1	1	1
1	X	X	0	0	0	0	1	1	1	1

X = Don't Care

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

BLOCK DIAGRAM

MC14555B

```
2 ── A      Q0 ── 4
3 ── B      Q1 ── 5
1 ──o E     Q2 ── 6
            Q3 ── 7

14 ── A     Q0 ── 12
13 ── B     Q1 ── 11
15 ──o E    Q2 ── 10
            Q3 ── 9
```

MC14556B

```
2 ── A      Q̄0 ── 4
3 ── B      Q̄1 ── 5
1 ──o E     Q̄2 ── 6
            Q̄3 ── 7

14 ── A     Q̄0 ── 12
13 ── B     Q̄1 ── 11
15 ──o E    Q̄2 ── 10
            Q̄3 ── 9
```

V_{DD} = PIN 16
V_{SS} = PIN 8

MOTOROLA

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level $V_{in} = V_{DD}$ or 0	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level $V_{in} = 0$ or V_{DD}	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level ($V_O = 4.5$ or 0.5 Vdc) ($V_O = 9.0$ or 1.0 Vdc) ($V_O = 13.5$ or 1.5 Vdc)	V_{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
"1" Level ($V_O = 0.5$ or 4.5 Vdc) ($V_O = 1.0$ or 9.0 Vdc) ($V_O = 1.5$ or 13.5 Vdc)	V_{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current Source ($V_{OH} = 2.5$ Vdc) ($V_{OH} = 4.6$ Vdc) ($V_{OH} = 9.5$ Vdc) ($V_{OH} = 13.5$ Vdc)	I_{OH}	5.0	− 3.0	—	− 2.4	− 4.2	—	− 1.7	—	mAdc
		5.0	− 0.64	—	− 0.51	− 0.88	—	− 0.36	—	
		10	− 1.6	—	− 1.3	− 2.25	—	− 0.9	—	
		15	− 4.2	—	− 3.4	− 8.8	—	− 2.4	—	
Sink ($V_{OL} = 0.4$ Vdc) ($V_{OL} = 0.5$ Vdc) ($V_{OL} = 1.5$ Vdc)	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance ($V_{in} = 0$)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) ($C_L = 50$ pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (0.85\ \mu A/kHz)\ f + I_{DD}$							μAdc
		10	$I_T = (1.70\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (2.60\ \mu A/kHz)\ f + I_{DD}$							

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
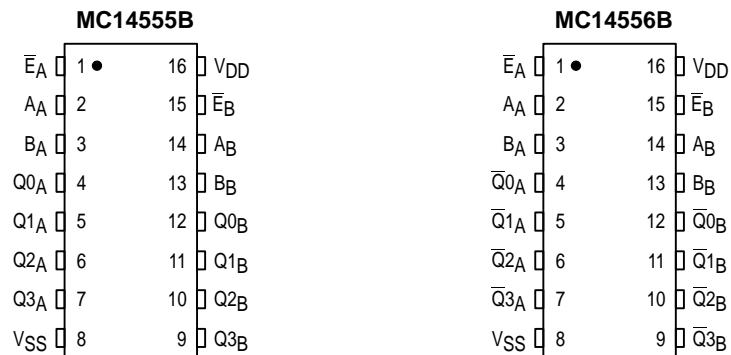
** The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L − 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = ($V_{DD} − V_{SS}$) in volts, f in kHz is input frequency, and k = 0.002.

PIN ASSIGNMENTS

MC14555B

$\overline{E}_A$	1 •	16	V_{DD}
A_A	2	15	$\overline{E}_B$
B_A	3	14	A_B
$Q0_A$	4	13	B_B
$Q1_A$	5	12	$Q0_B$
$Q2_A$	6	11	$Q1_B$
$Q3_A$	7	10	$Q2_B$
V_{SS}	8	9	$Q3_B$

MC14556B

$\overline{E}_A$	1 •	16	V_{DD}
A_A	2	15	$\overline{E}_B$
B_A	3	14	A_B
$\overline{Q0}_A$	4	13	B_B
$\overline{Q1}_A$	5	12	$\overline{Q0}_B$
$\overline{Q2}_A$	6	11	$\overline{Q1}_B$
$\overline{Q3}_A$	7	10	$\overline{Q2}_B$
V_{SS}	8	9	$\overline{Q3}_B$

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns	t_{TLH}, t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time — A, B to Output t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 135 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 62 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 45 ns	t_{PLH}, t_{PHL}	5.0 10 15	— — —	220 95 70	440 190 140	ns
Propagation Delay Time — E to Output t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 115 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 52 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 40 ns	t_{PLH}, t_{PHL}	5.0 10 15	— — —	200 85 65	400 170 130	ns

* The formulas given are for the typical characteristics only at 25°C.
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
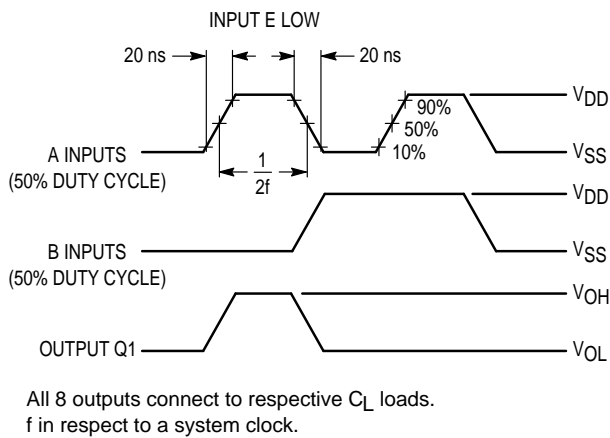
Figure 1. Dynamic Power Dissipation Signal Waveforms

All 8 outputs connect to respective C_L loads.
f in respect to a system clock.
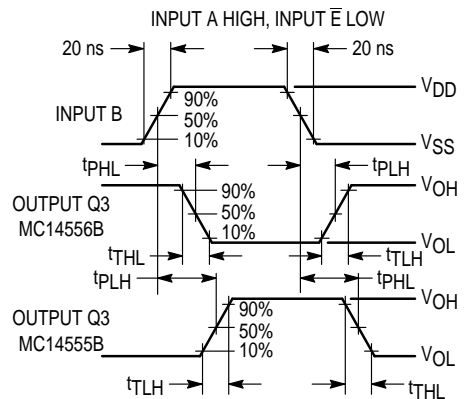
Figure 2. Dynamic Signal Waveforms

LOGIC DIAGRAM
(1/2 of Dual)
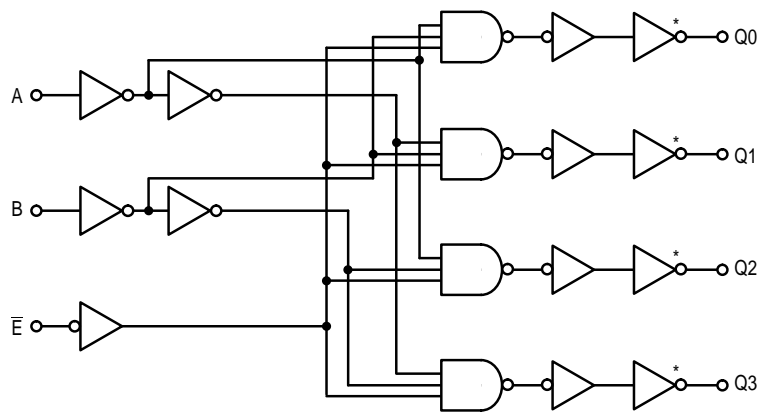
* Eliminated for MC14555B

OUTLINE DIMENSIONS

L SUFFIX
CERAMIC DIP PACKAGE
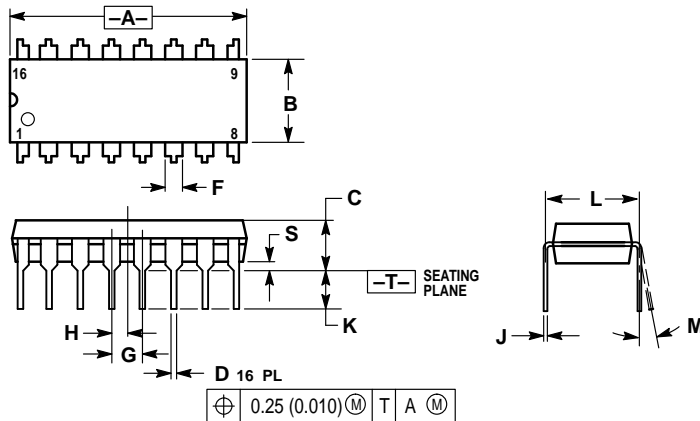### CASE 620–10
ISSUE V
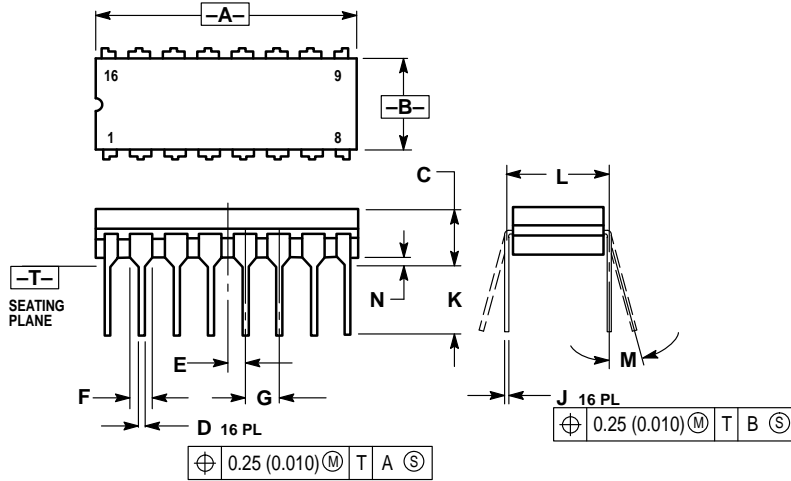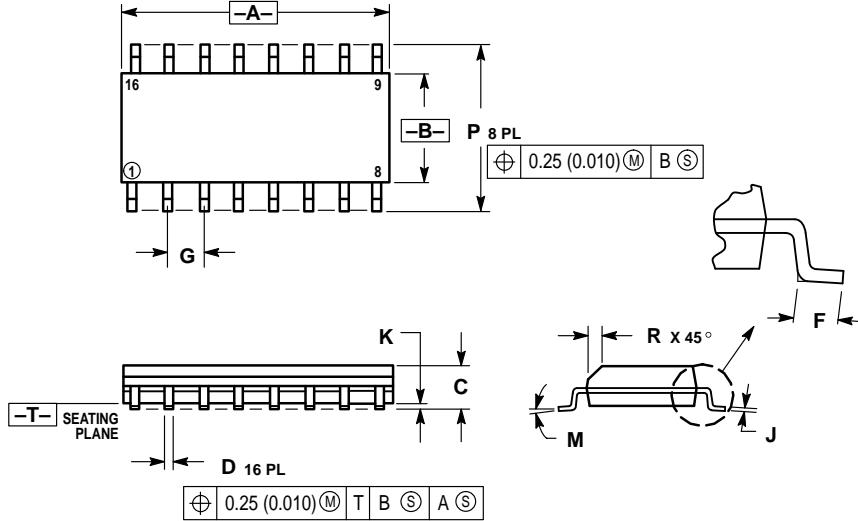

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0 °	15 °	0 °	15 °
N	0.020	0.040	0.51	1.01

P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

OUTLINE DIMENSIONS

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

MOTOROLA

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MC14555B/D