



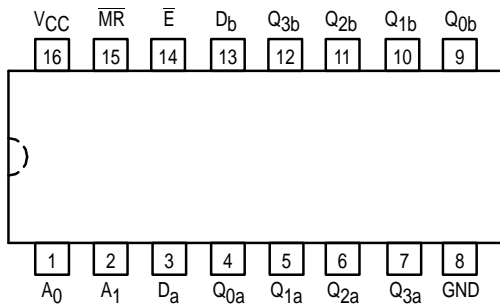
DUAL 4-BIT ADDRESSABLE LATCH

The MC54/74F256 dual addressable latch has four distinct modes of operation which are selectable by controlling the Clear and Enable inputs (see Function Table). In the addressable latch mode, data at the Data (D) inputs is written into the addressed latches. The addressed latches will follow the Data input with all unaddressed latches remaining in their previous states.

In the memory mode, all latches remain in their previous states and are unaffected by the Data or Address inputs. To eliminate the possibility of entering erroneous data in the latches, the enable should be held HIGH (inactive) while the address lines are changing. In the dual 1-of-4 decoding or demultiplexing mode ($\overline{MR} = \overline{E} = \text{LOW}$), addressed outputs will follow the level of the D inputs with all other outputs LOW. In the clear mode, all outputs are LOW and unaffected by the Address and Data inputs.

- Combines Dual Demultiplexer and 8-Bit Latch
- Serial-to-Parallel Capability
- Output from Each Storage Bit Available
- Random (Addressable) Data Entry
- Easily Expandable
- Common Clear Input
- Useful as Dual 1-of-4 Active HIGH Decoder

CONNECTION DIAGRAM



FUNCTION TABLE

Operating Mode	Inputs					Outputs			
	\overline{MR}	\overline{E}	D	A ₀	A ₁	Q ₀	Q ₁	Q ₂	Q ₃
Master Reset	L	H	X	X	X	L	L	L	L
Demultiplex (Active HIGH Decoder when D = H)	L	L	d	L	L	Q=d	L	L	L
	L	L	d	H	L	L	Q=d	L	L
	L	L	d	L	H	L	L	Q=d	L
Store (Do Nothing)	H	H	X	X	X	q ₀	q ₁	q ₂	q ₃
Addressable Latch	H	L	d	L	L	Q=d	q ₁	q ₂	q ₃
	H	L	d	H	L	q ₀	Q=d	q ₂	q ₃
	H	L	d	L	H	q ₀	q ₁	Q=d	q ₃
	H	L	d	H	H	q ₀	q ₁	q ₂	Q=d

H = HIGH Voltage Level Steady State

L = LOW Voltage Level Steady State

X = Immaterial

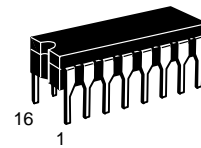
d = HIGH or LOW Data one setup time prior to the LOW-to-HIGH Enable transition.

q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

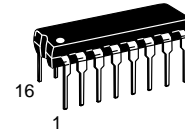
MC54/74F256

DUAL 4-BIT ADDRESSABLE LATCH

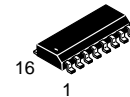
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

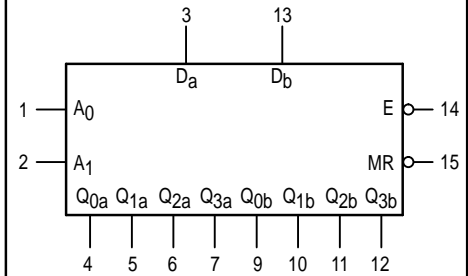


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

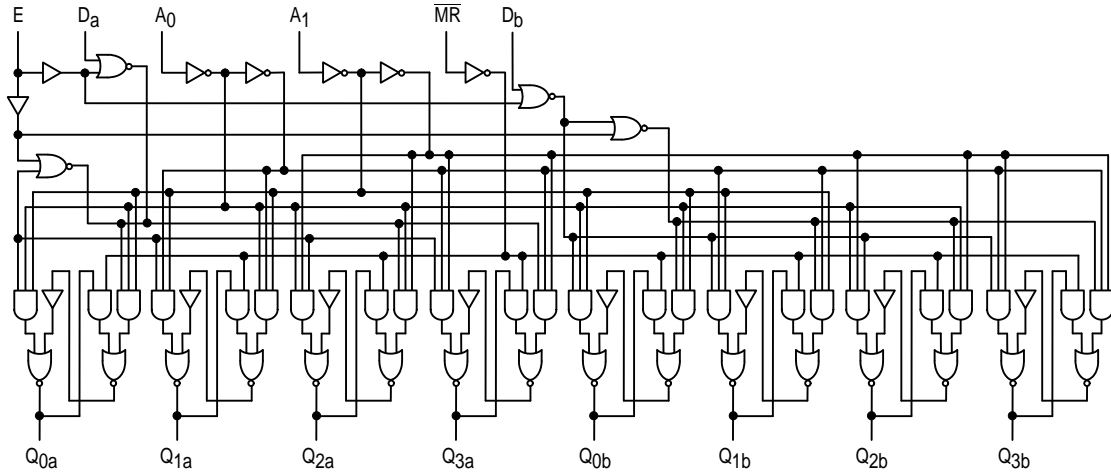
MC54FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXD SOIC

LOGIC SYMBOL



MC54/74F256

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-1.0	mA
I _{OL}	Output Current — Low	54, 74			20	mA

MC54/74F256

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage
V _{IK}	Input Clamp Diode Voltage			-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54, 74	2.5		V	I _{OL} = -1.0 mA, V _{CC} = MIN
		74	2.7		V	I _{OL} = -1.0 mA, V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage			0.5	V	I _{OL} = 20 mA, V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-0.6	mA	V _{CC} = MAX, V _{IN} = 0.5 V
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V
I _{CC}	Power Supply Current Total, Output HIGH Total, Output LOW			42	mA	V _{CC} = MAX
				60	mA	V _{CC} = MAX

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

MC54/74F256

AC CHARACTERISTICS

Symbol	Parameter	54/74F		54F		74F		Unit
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$ $C_L = 50\text{ pF}$		$T_A = -55\text{ to }+125^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 10\%$ $C_L = 50\text{ pF}$		$T_A = 0\text{ to }70^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 5\%$ $C_L = 50\text{ pF}$		
		Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay \bar{E} to Q_n	4.0 3.0	10.5 7.0	4.0 3.0	13 8.5	4.0 3.0	12 7.5	ns
t_{PLH} t_{PHL}	Propagation Delay D_n to Q_n	3.5 3.0	9.0 7.0	3.5 2.5	11.5 8.5	3.5 2.5	10 7.5	ns
t_{PLH} t_{PHL}	Propagation Delay A_n to Q_n	3.5 4.0	14 9.5	3.5 4.0	15.5 11	3.5 4.0	14.5 10	ns
t_{PHL}	Propagation Delay \overline{MR} to Q_n	5.0	9.0	4.5	11.5	4.5	10	ns

AC OPERATING REQUIREMENTS

Symbol	Parameter	54/74F		54F		74F		Unit
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$		$T_A = -55\text{ to }+125^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 10\%$		$T_A = 0\text{ to }70^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 5\%$		
		Min	Max	Min	Max	Min	Max	
$t_{S(H)}$ $t_{S(L)}$	Setup Time, HIGH or LOW D_n to \bar{E}	4.0 4.0		5.0 5.0		4.0 4.0		ns
$t_{H(H)}$ $t_{H(L)}$	Hold Time, HIGH or LOW D_n to \bar{E}	2.0 2.0		2.0 2.0		2.0 2.0		ns
$t_{S(H)}$ $t_{S(L)}$	Setup Time, HIGH or LOW A to \bar{E} (a)	4.0 4.0		4.0 4.0		4.0 4.0		ns
$t_{H(H)}$ $t_{H(L)}$	Hold Time HIGH or LOW A to \bar{E} (b)	0 0		0 0		0 0		ns
t_W	\bar{E} Pulse Width	4.0		4.0		4.0		ns
t_W	\overline{MR} Pulse Width	4.0		4.0		4.0		ns

NOTES:

1. The Address to Enable setup time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
2. The Address to Enable hold time is the time after the LOW-to-HIGH Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.