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Printed on:Mon, Feb 6, 1995 09:48:26
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MOTOROLA

8-INPUT SHIFT/STORAGE REGISTER WITH SYNCHRONOUS RESET AND COMMON I/O PINS

MC74F323

8-INPUT SHIFT/STORAGE REGISTER WITH SYNCHRONOUS RESET AND COMMON I/O PINS

FAST™ SCHOTTKY TTL

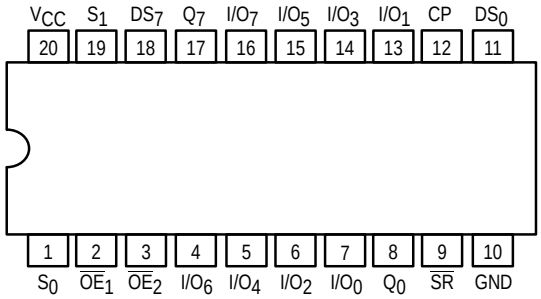
The MC74F323 is an 8-Bit Universal Shift/Storage Register with 3-state outputs. Its function is similar to the F299 with the exception of Synchronous Reset.

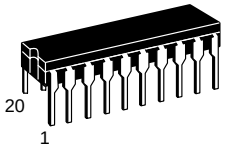
The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Separate outputs are provided for flip-flops Q_0 and Q_7 to allow easy cascading. A separate active LOW Master Reset is used to reset the register.

Four modes of operation are possible: hold (store), shift left, shift right and parallel load. All modes are activated on the LOW-to-HIGH transition of the clock.

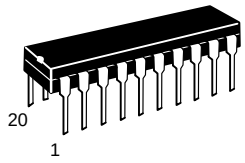
- Common I/O For Reduced Pin Count
- Four Operation Modes: Shift Left, Shift Right, Parallel Load and Store
- Separate Continuous Inputs and Outputs from Q_0 and Q_7 Allow Easy Cascading
- Fully Synchronous Reset
- 3-State Outputs for Bus Oriented Applications
- Input Clamp Diodes Limit High-Speed Termination Effects

CONNECTION DIAGRAM

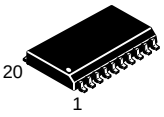




J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03



DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

MC74FXXXJ	Ceramic
MC74FXXXN	Plastic
MC74FXXXDW	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	74	0	25	70	°C
I_{OH}	Output Current — High	74			–1.0/–3.0	mA
I_{OL}	Output Current — Low	74			20/24	mA

FUNCTION TABLE

Inputs				Response
SR	S_1	S_0	CP	
L	X	X	↑	Synchronous Reset: Q_0–Q_7 = LOW
H	H	H	↑	Parallel Load: I/O_n Q_n
H	L	H	↑	Shift Right: DS_0 Q_0, Q_0 Q_1, etc.
H	H	L	↑	Shift Left: DS_7 Q_7, Q_7 Q_6, etc.
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↑ = LOW-to-HIGH clock transition.

FUNCTIONAL DESCRIPTION

The MC74F323 contains eight edge-triggered D-type flips-flops and the interstage logic necessary to perform synchronous reset, shift left, shift right, parallel load and hold operations. The type of operation is determined by S_0 and S_1, as shown in the Function Table. All flip-flop outputs are brought out through 3-state buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on $\overline{SR}$ overrides the Select inputs and allows the flip-flops to be reset by the next rising edge of CP. All other state changes are initiated by the LOW-to-HIGH CP transition. Inputs can change when the clock is in either state provided only that the recommended set-up and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on either $\overline{OE}_1$ or $\overline{OE}_2$ disables the 3-state buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-state buffers are also disabled by HIGH signals on both S_0 and S_1 in preparation for a parallel load operation.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless otherwise specified)

Symbol	Parameter			Limits Min	Typ	Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage			2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage					0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage					–1.2	V	V_{CC} = MIN, I_{IN} = –18 mA	
V_{OH}	Output HIGH Voltage	Q_0/Q_7	74	2.5			V	I_{OH} = –1.0 mA	V_{CC} = 4.5 V
			74	2.7					V_{CC} = 4.75 V
		I/O	74	2.7	3.4		V	I_{OH} = –3.0 mA	V_{CC} = 4.75 V
			74	2.4					V_{CC} = 4.5 V
V_{OL}	Output LOW Voltage		Q_0/Q_7			0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
			I/O			0.5		I_{OL} = 24 mA	
I_{IH}	Input HIGH Current		Q_0/Q_7			20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
			I/O			70			
			Q_0/Q_7			0.1	mA	V_{CC} = MAX	V_{IN} = 7.0 V
			I/O			1.0			V_{IN} = 5.5 V
I_{IL}	Input LOW Current		S_0, S_1			–1.2	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
			Other Inputs			–0.6			
I_{OZH}	Off-State Output Current, High-Level Voltage Applied					70	μA	V_{CC} = MAX	V_{OUT} = 2.7 V
						1.0	mA		V_{OUT} = 5.5 V
I_{OZL}	Off-State Output Current, Low-Level Voltage Applied					–0.6	mA	V_{CC} = MAX, V_{OUT} = 0.5 V	
I_{OS}	Output Short Circuit Current (Note 2)			–60		–150	mA	V_{CC} = MAX	V_{OUT} = 0 V
I_{CC}	Total Supply Current					95	mA		Outputs Disabled

NOTES:
1. For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF		74F T_A = 0°C to +70°C, V_{CC} = +5.0 V ±10%, C_L = 50 pF		Unit
		Min	Max	Min	Max	
f_{MAX}	Maximum Input Frequency	70		70		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q_0 or Q_7	3.5 3.5	9.0 8.5	3.5 3.5	10 9.5	ns
t_{PLH} t_{PHL}	Propagation Delay CP to I/O_n	3.5 5.0	9.0 11	3.5 5.0	10 12	ns
t_{PZH} t_{PZL}	Output Enable Time to HIGH or LOW Level	3.5 4.0	8.0 10	3.5 4.0	9.0 11	ns
t_{PHZ} t_{PLZ}	Output Disable Time to HIGH or LOW Level	2.0 2.0	6.0 5.5	2.0 2.0	7.0 6.5	ns

AC SETUP REQUIREMENTS

Symbol	Parameter	74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			74F T_A = 0°C to +70°C, V_{CC} = +5.0 V ±10%, C_L = 50 pF		Unit
		Min	Typ	Max	Min	Max	
$t_{s(H)}$ $t_{s(L)}$	Set-Up Time, HIGH or LOW S_0 or S_1 to CP	8.5 8.5			8.5 8.5		ns
$t_{h(H)}$ $t_{h(L)}$	Hold Time, HIGH or LOW S_0 or S_1 to CP	0.0 0.0			0.0 0.0		ns
$t_{s(H)}$ $t_{s(L)}$	Set-Up Time, HIGH or LOW I/O_n, DS_0, DS_7 to CP	5.0 5.0			5.0 5.0		ns
$t_{h(H)}$ $t_{h(L)}$	Hold Time, HIGH or LOW I/O_n, DS_0, DS_7 to CP	2.0 2.0			2.0 2.0		ns
$t_{s(H)}$ $t_{s(L)}$	Set-Up Time, HIGH or LOW $\overline{SR}$ to CP	10 10			10 10		ns
$t_{h(H)}$ $t_{h(L)}$	Hold Time, HIGH or LOW $\overline{SR}$ to CP	0.0 0.0			0.0 0.0		ns
$t_{w(H)}$ $t_{w(L)}$	CP Pulse Width, HIGH or LOW	7.0 7.0			7.0 7.0		ns

LOGIC DIAGRAM