MOTOROLA

MC74F579

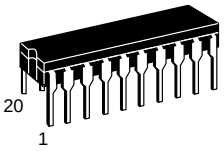
8-BIT BIDIRECTIONAL BINARY COUNTER (3-STATE)

The MC74F579 is a fully synchronous 8-stage up/down counter with multiplexed 3-state I/O ports for bus-oriented applications. It features a preset capability for programmable operation, carry look-ahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, except for the case of asynchronous reset, are initiated by the rising edge of the clock. $\overline{TC}$ output is not recommended for use as a clock or asynchronous reset due to the possibility of decoding spikes.

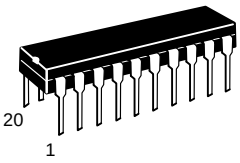
- Multiplexed 3-State I/O Ports For Bus-oriented Applications
- Built-In Cascading Carry Capability
- Count Frequency 115 MHz Typ
- Supply Current 100 mA Typ
- Fully Synchronous Operation
- U/D Pin to Control Direction of Counting
- Separate Pins for Master Reset and Synchronous Reset
- Center Power Pins to Reduce Effects of Package Inductance
- See F269 for 24-Pin Separate I/O Port Version
- See F779 for 16-Pin Version
- ESD Protection > 4000 Volts

8-BIT BIDIRECTIONAL BINARY COUNTER (3-STATE)

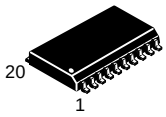
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03

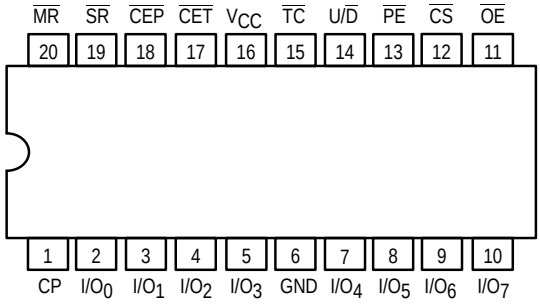


DW SUFFIX
SOIC
CASE 751D-03

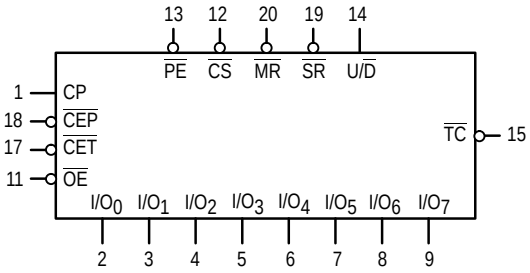
ORDERING INFORMATION

MC74FXXXJ	Ceramic
MC74FXXXN	Plastic
MC74FXXXDW	SOIC

PIN ASSIGNMENT



LOGIC SYMBOL



GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage		4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range		0	25	70	°C
I_{OH}	Output Current — High	$\overline{TC}$			–1.0	mA
		I/O_n			–3.0	
I_{OL}	Output Current — Low	$\overline{TC}$			20	mA
		I/O_n			24	

FUNCTION TABLE

$\overline{MR}$	$\overline{SR}$	$\overline{CS}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	$\overline{OE}$	CP	Function
X	X	H	X	X	X	X	X	X	I/O_0 to I/O_7 in Hi-Z ($\overline{PE}$ disabled)
X	X	L	H	X	X	X	H	X	I/O_0 to I/O_7 in Hi-Z
X	X	L	H	X	X	X	L	X	Flip-Flop outputs appear on I/O lines
L	X	X	X	X	X	X	X	X	Asynchronous reset for all flip-flops
H	L	X	X	X	X	X	X	↑	Synchronous reset for all flip-flops
H	H	L	L	X	X	X	X	↑	Parallel load all flip-flops
H	H	(not LL)		H	X	X	X	↑	Hold
H	H	(not LL)		X	H	X	X	↑	Hold ($\overline{TC}$ held high)
H	H	(not LL)		L	L	H	X	↑	Count up
H	H	(not LL)		L	L	L	X	↑	Count down

H = High voltage level L = Low voltage level
X = Don't care ↑ = Low-to-High clock transition
(not LL) = CS and PE should never both be low voltage at the same time

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		74F Min	74F Typ (2)	74F Max	Unit	Test Conditions (Note 1)	
V_{OH}	Output HIGH Voltage	TC	2.5			V	I_{OH} = –1.0 mA V_{IL} = MAX V_{IH} = MIN	V_{CC} = 4.5 V
			2.7	3.4				V_{CC} = 4.75 V
		I/O_n	2.4	3.3		V	I_{OH} = –3.0 mA V_{IL} = MAX V_{IH} = MIN	V_{CC} = 4.5 V
			2.7	3.3				V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage	$\overline{TC}$		0.35	0.5	V	I_{OL} = 20 mA	V_{CC} = 4.5 V V_{IL} = MAX V_{IH} = MIN
		I/O_n					I_{OL} = 24 mA	
V_{IK}	Input Clamp Diode Voltage			–0.73	–1.2	V	V_{CC} = 4.5 V, I_{IN} = –18 mA	
I_{IH}	Input HIGH Current	I/O_n			1.0	mA	V_{CC} = 5.5 V	V_{IN} = 5.5 V
		others			100	µA		V_{IN} = 7.0 V
		I/O_n			70	µA	V_{CC} = 5.5 V, V_{IN} = 2.7 V	
		others			20			
I_{IL}	Input LOW Current	Except I/O_n			–0.6	mA	V_{CC} = 5.5 V, V_{IN} = 0.5 V	
I_{OZH}	OFF-State Current High-Level Voltage Applied	I/O_n			70	µA	V_{CC} = 5.5 V	V_{OUT} = 2.7 V
I_{OZL}	OFF-State Current Low-Level Voltage Applied				–600			V_{OUT} = 0.5 V
I_{OS}	Output Short Circuit Current (Note 3)		–60	–80	–150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Total Supply Current (total)	I_{CCH}		95	135	mA	V_{CC} = MAX	
		I_{CCL}		105	145			
		I_{CCZ}		105	150			

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating conditions for the applicable device type.
2. All typical values are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For I_{OS} testing, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

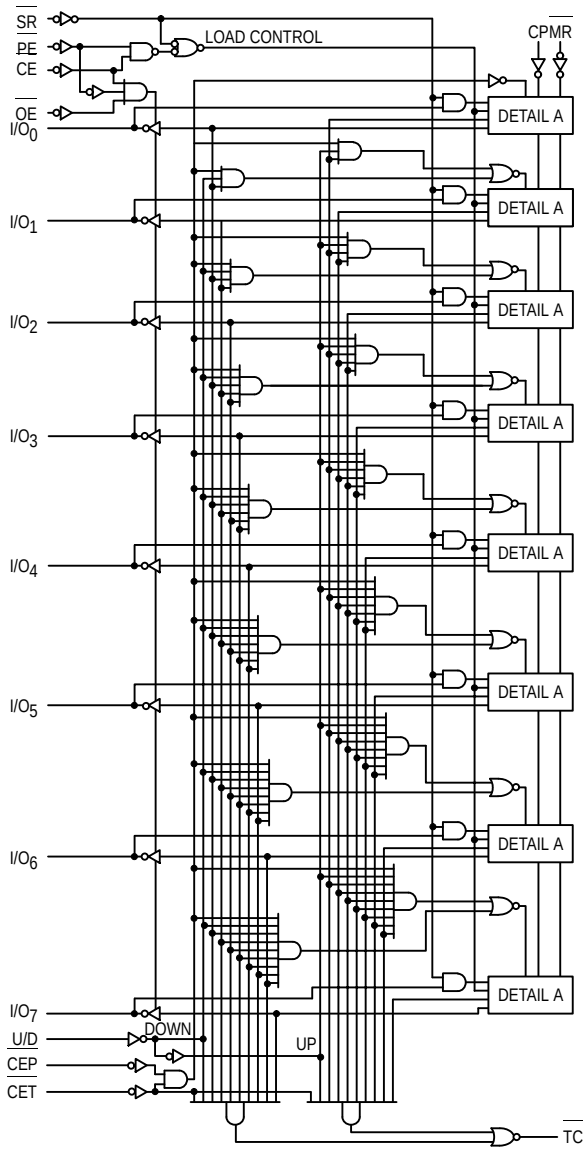
AC ELECTRICAL CHARACTERISTICS

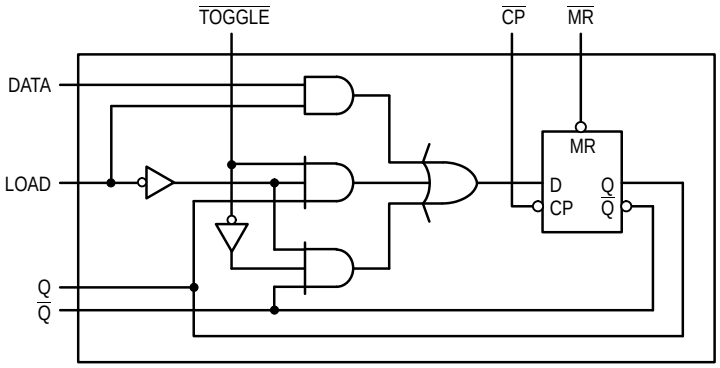
Symbol	Parameter	74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			74F T_A = 0°C to +70°C, V_{CC} = +5.0 V ±10%, C_L = 50 pF		Unit
		Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	100			80		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to I/O_n	5.0 5.0		10.5 10.5	5.0 5.0	11.5 11.5	ns
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$	4.5 5.5		10 10	4.5 5.0	11 11	ns
t_{PLH} t_{PHL}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$	3.5 4.5		8.0 8.0	3.5 4.5	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	3.5 3.5		7.0 8.0	3.5 3.5	8.5 8.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_n	5.0		10	5.0	11	ns
t_{PZH} t_{PZL}	Output Enable Time to HIGH or LOW Level $\overline{CS}$, $\overline{PE}$ to I/O_n	4.5 6.5		10.5 10.5	4.5 6.0	11.5 11.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time to HIGH or LOW Level $\overline{CS}$, $\overline{PE}$ to I/O_n	3.0 4.0		7.5 9.5	3.0 4.0	9.0 11	ns
t_{PZH} t_{PZL}	Output Enable Time to HIGH or LOW Level $\overline{OE}$ to I/O_n	4.0 6.0		8.5 9.5	4.0 5.0	9.5 10.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time to HIGH or LOW Level $\overline{OE}$ to I/O_n	1.0 2.5		6.0 7.0	1.0 2.5	6.5 8.0	ns

AC SETUP REQUIREMENTS

Symbol	Parameter	74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			74F T_A = 0°C to +70°C, V_{CC} = +5.0 V ±10%, C_L = 50 pF			Unit
		Min	Typ	Max	Min	Typ	Max	
$t_{s(H)}$ $t_{s(L)}$	Setup Time, HIGH or LOW I/O_n to CP	3.0 3.0			4.0 4.0			ns
$t_{h(H)}$ $t_{h(L)}$	Hold Time, HIGH or LOW I/O_n to CP	1.0 1.0			1.0 1.0			ns
$t_{s(H)}$ $t_{s(L)}$	Setup Time, HIGH or LOW $\overline{PE}$, $\overline{SR}$ or $\overline{CS}$ to CP	9.5 9.5			10 10			ns
$t_{h(H)}$ $t_{h(L)}$	Hold Time, HIGH or LOW $\overline{PE}$, $\overline{SR}$ or $\overline{CS}$ to CP	0 0			0 0			ns
$t_{s(H)}$ $t_{s(L)}$	Setup Time, HIGH or LOW $\overline{CET}$, $\overline{CEP}$ to CP	5.0 9.0			5.5 10.5			ns
$t_{h(H)}$ $t_{h(L)}$	Hold Time, HIGH or LOW $\overline{CET}$, $\overline{CEP}$ to CP	0 0			0 0			ns
t_w	CP Pulse Width	4.5			6.0			ns
$t_{w(L)}$	$\overline{MR}$ Pulse Width	3.5			4.5			ns
t_{rec}	$\overline{MR}$ Recovery Time	4.0			4.5			ns

LOGIC DIAGRAM





Detail A