MJH16006A

Designer's™ Data Sheet

NPN Silicon Power Transistor
1 kV SWITCHMODE Series

These transistors are designed for high–voltage, high–speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line–operated switchmode applications.

Typical Applications: Features:

- Switching Regulators
- Inverters
- Solenoids
- Relay Drivers
- Motor Controls
- Deflection Circuits

- Collector–Emitter Voltage — V_{CEV} = 1000 Vdc
- Fast Turn–Off Times
    80 ns Inductive Fall Time — 100°C (Typ)
    120 ns Inductive Crossover Time — 100°C (Typ)
    800 ns Inductive Storage Time — 100°C (Typ)
- 100°C Performance Specified for:
    Reverse–Biased SOA with Inductive Load
    Switching Times with Inductive Loads
    Saturation Voltages
    Leakage Currents
- Extended FBSOA Rating Using Ultra–fast Rectifiers
- Extremely High RBSOA Capability

**POWER TRANSISTORS
8 AMPERES
500 VOLTS
150 WATTS**

CASE 340D–01
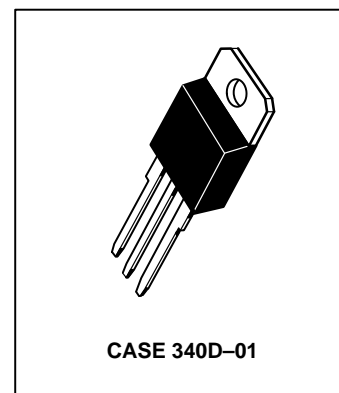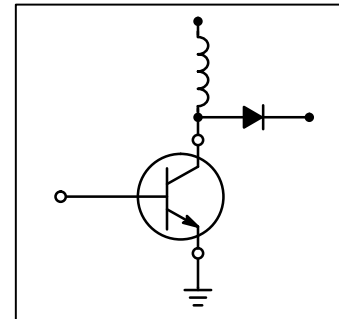
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	500	Vdc
Collector–Emitter Voltage	V_{CEV}	1000	Vdc
Emitter–Base Voltage	V_{EB}	6	Vdc
Collector Current — Continuous — Peak[1]	I_C I_{CM}	8 16	Adc
Base Current — Continuous — Peak[1]	I_B I_{BM}	6 12	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above T_C = 25°C	P_D	125 50 1	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

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REV 3

MOTOROLA

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS[1]					
Collector–Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	500	—	—	Vdc
Collector Cutoff Current (V_{CEV} = 1000 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = 1000 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	I_{CEV}	 — —	 0.003 0.020	 0.15 1.0	mAdc
Collector Cutoff Current (V_{CE} = 1000 Vdc, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	0.020	1.0	mAdc
Emitter Cutoff Current (V_{EB} = 6 Vdc, I_C = 0)	I_{EBO}	—	0.005	0.15	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$		See Figure 14a or 14b		
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 15		
ON CHARACTERISTICS[1]					
Collector–Emitter Saturation Voltage (I_C = 3 Adc, I_B = 0.6 Adc) (I_C = 5 Adc, I_B = 1 Adc) (I_C = 5 Adc, I_B = 1 Adc, T_C = 100°C)	$V_{CE(sat)}$	 — — —	 0.35 0.50 0.60	 0.7 1 1.5	Vdc
Base–Emitter Saturation Voltage (I_C = 5 Adc, I_B = 1 Adc) (I_C = 5 Adc, I_B = 1 Adc, T_C = 100°C)	$V_{BE(sat)}$	 — —	 1 1	 1.5 1.5	Vdc
DC Current Gain (I_C = 8 Adc, V_{CE} = 5 Vdc)	h_{FE}	5	8	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 kHz)	C_{ob}	—	—	350	pF
SWITCHING CHARACTERISTICS					

Inductive Load (Table 1)

			Symbol	Min	Typ	Max	Unit
Storage Time	(I_C = 5 Adc, I_{B1} = 0.66 Adc, $V_{BE(off)}$ = 5 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_J = 100°C)	t_{sv}	—	800	2000	ns
Fall Time			t_{fi}	—	80	200	
Crossover Time			t_c	—	120	300	
Storage Time		(T_J = 150°C)	t_{sv}	—	1000	—	
Fall Time			t_{fi}	—	90	—	
Crossover Time			t_c	—	150	—	

Resistive Load (Table 2)

			Symbol	Min	Typ	Max	Unit
Delay Time	(I_C = 5 Adc, V_{CC} = 250 Vdc, I_{B1} = 0.66 Adc, PW = 30 μs, Duty Cycle ≤ 2%)	(I_{B2} = 1.3 Adc, R_{B1} = R_{B2} = 4 Ω)	t_d	—	25	100	ns
Rise Time			t_r	—	400	700	
Storage Time			t_s	—	1400	3000	
Fall Time			t_f	—	175	400	
Storage Time		($V_{BE(off)}$ = 5 Vdc)	t_s	—	475	—	
Fall Time			t_f	—	100	—	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

TYPICAL STATIC CHARACTERISTICS

Figure 1. DC Current Gain

- h_{FE}, DC CURRENT GAIN (vertical axis)
- I_C, COLLECTOR CURRENT (AMPS) (horizontal axis)
- $T_J = 100°C$
- $25°C$
- $-55°C$
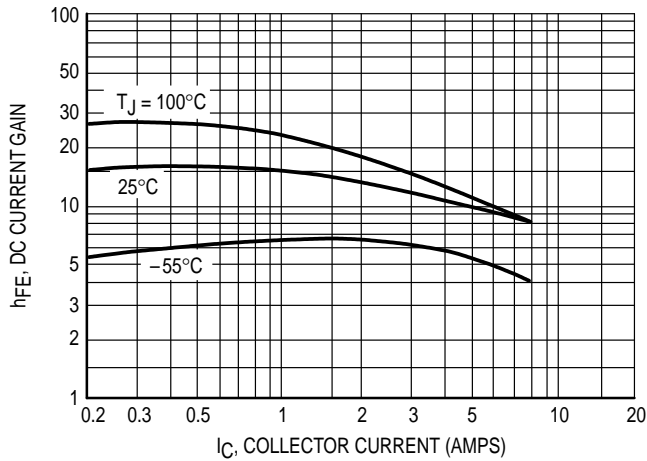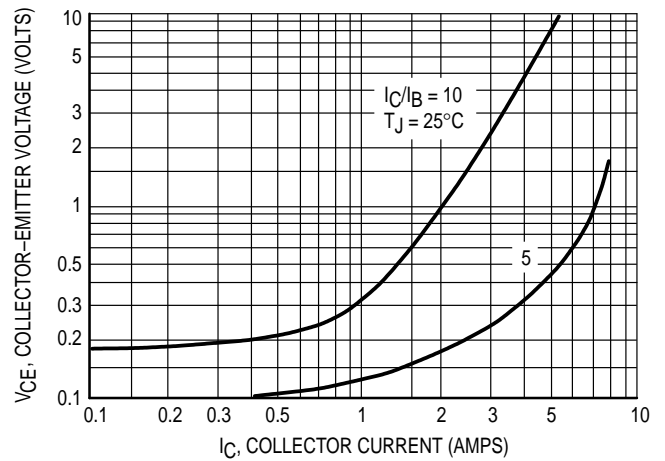
Figure 2. Collector–Emitter Saturation Region

- V_{CE}, COLLECTOR–EMITTER VOLTAGE (VOLTS) (vertical axis)
- I_C, COLLECTOR CURRENT (AMPS) (horizontal axis)
- $I_C/I_B = 10$
- $T_J = 25°C$
- 5
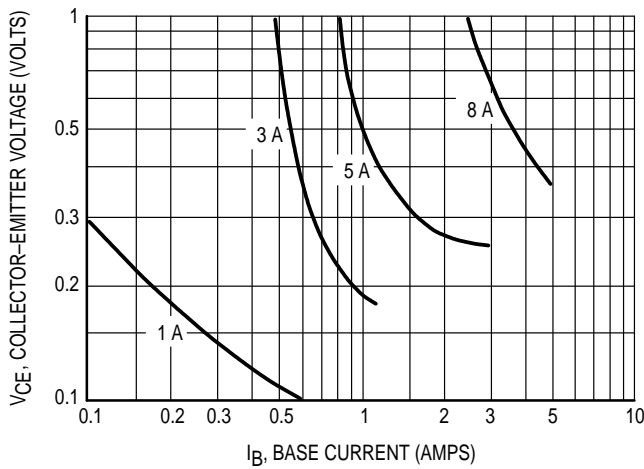
Figure 3. Collector–Emitter Saturation Region

- V_{CE}, COLLECTOR–EMITTER VOLTAGE (VOLTS) (vertical axis)
- I_B, BASE CURRENT (AMPS) (horizontal axis)
- 1 A
- 3 A
- 5 A
- 8 A
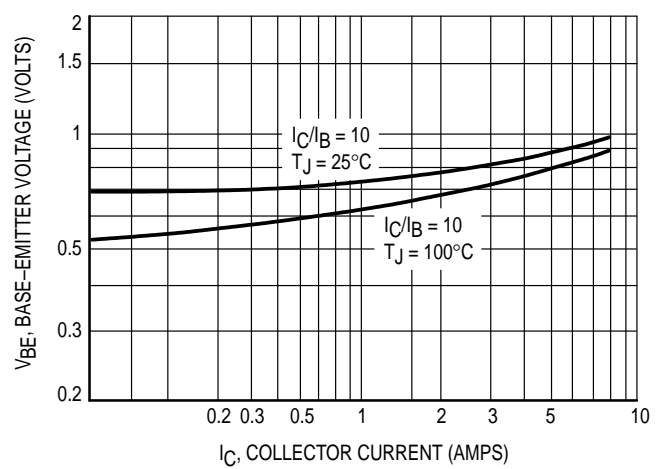
Figure 4. Base–Emitter Saturation Region

- V_{BE}, BASE–EMITTER VOLTAGE (VOLTS) (vertical axis)
- I_C, COLLECTOR CURRENT (AMPS) (horizontal axis)
- $I_C/I_B = 10$
- $T_J = 25°C$
- $I_C/I_B = 10$
- $T_J = 100°C$

Figure 5. Capacitance

- C, CAPACITANCE (pF) (vertical axis)
- V_R, REVERSE VOLTAGE (VOLTS) (horizontal axis)
- C_{ib}
- C_{ob}
- $T_J = 25°C$
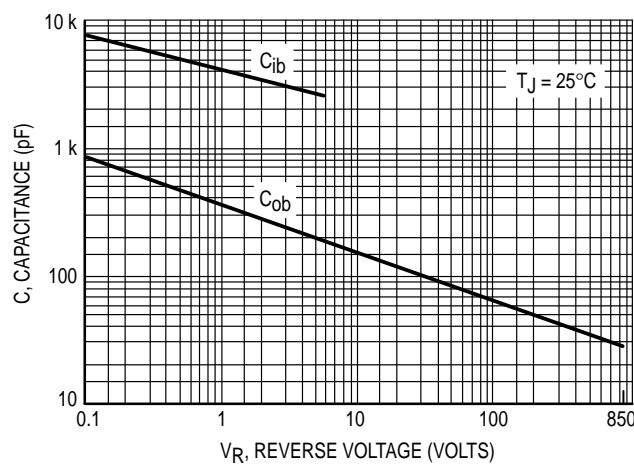
TYPICAL INDUCTIVE SWITCHING CHARACTERISTICS

I$_C$/I$_{B1}$ = 5, T$_C$ = 75°C, V$_{CE(pk)}$ = 400 V

I$_C$/I$_{B1}$ = 10, T$_C$ = 75°C, V$_{CE(pk)}$ = 400 V
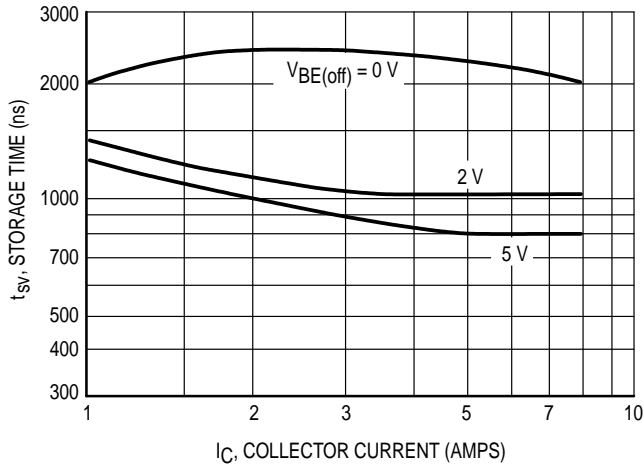
Figure 6. Storage Time
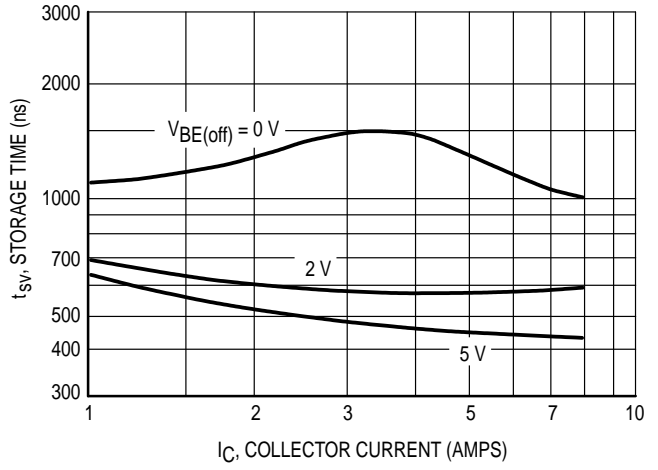
Figure 7. Storage Time
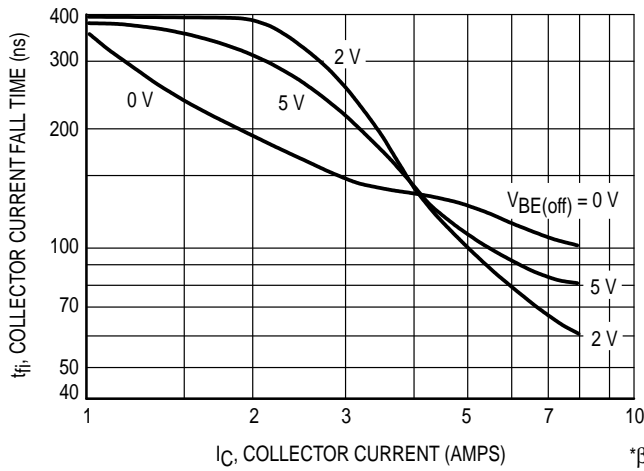
Figure 8. Collector Current Fall Time
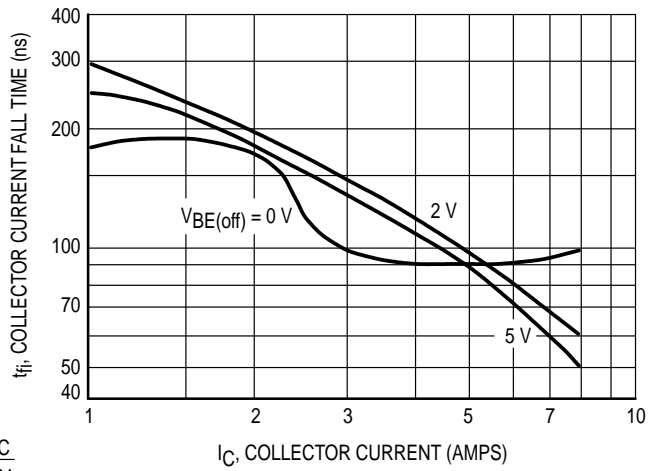
$$*\beta_f = \frac{I_C}{I_{B1}}$$

Figure 9. Collector Current Fall Time
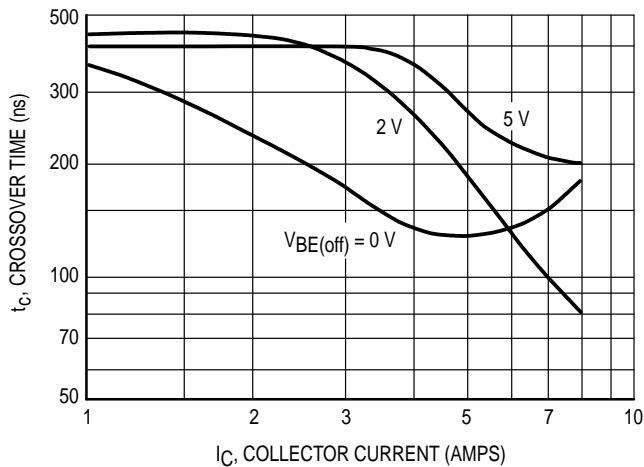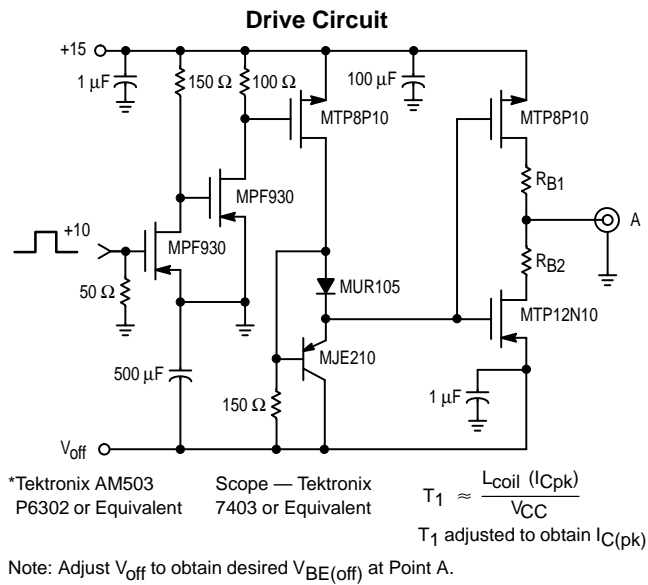

Figure 10. Crossover Time
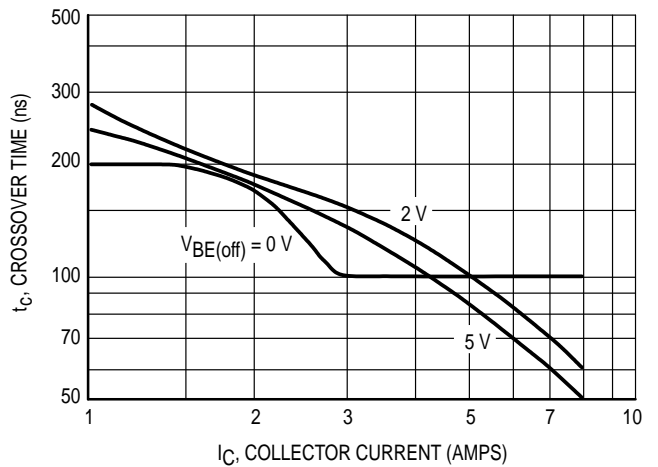
Figure 11. Crossover Time

Table 1. Inductive Load Switching

Drive Circuit

$V_{CEO(sus)}$
L = 10 mH
R_{B2} = ∞
V_{CC} = 20 Volts

Inductive Switching
L = 750 μH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

RBSOA
L = 750 μH
R_{B2} = 0
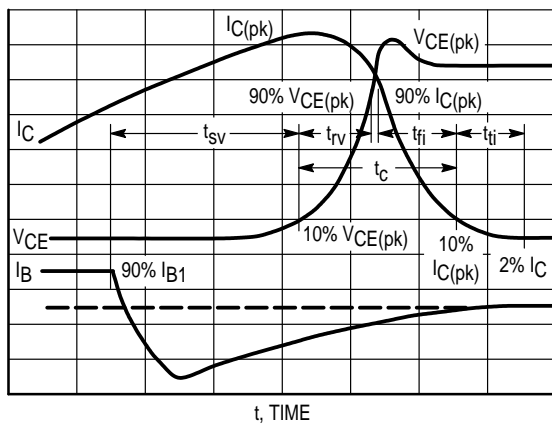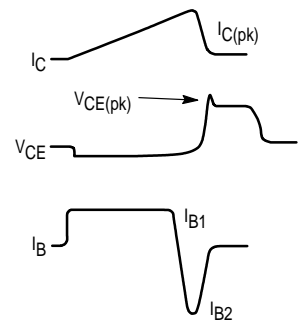V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

*Tektronix AM503
 P6302 or Equivalent

Scope — Tektronix
7403 or Equivalent

$$T_1 \approx \frac{L_{coil} \, (I_{Cpk})}{V_{CC}}$$

T_1 adjusted to obtain $I_{C(pk)}$

Note: Adjust V_{off} to obtain desired $V_{BE(off)}$ at Point A.

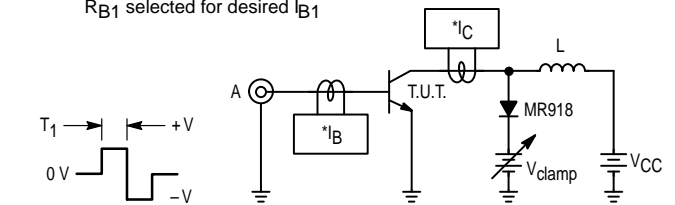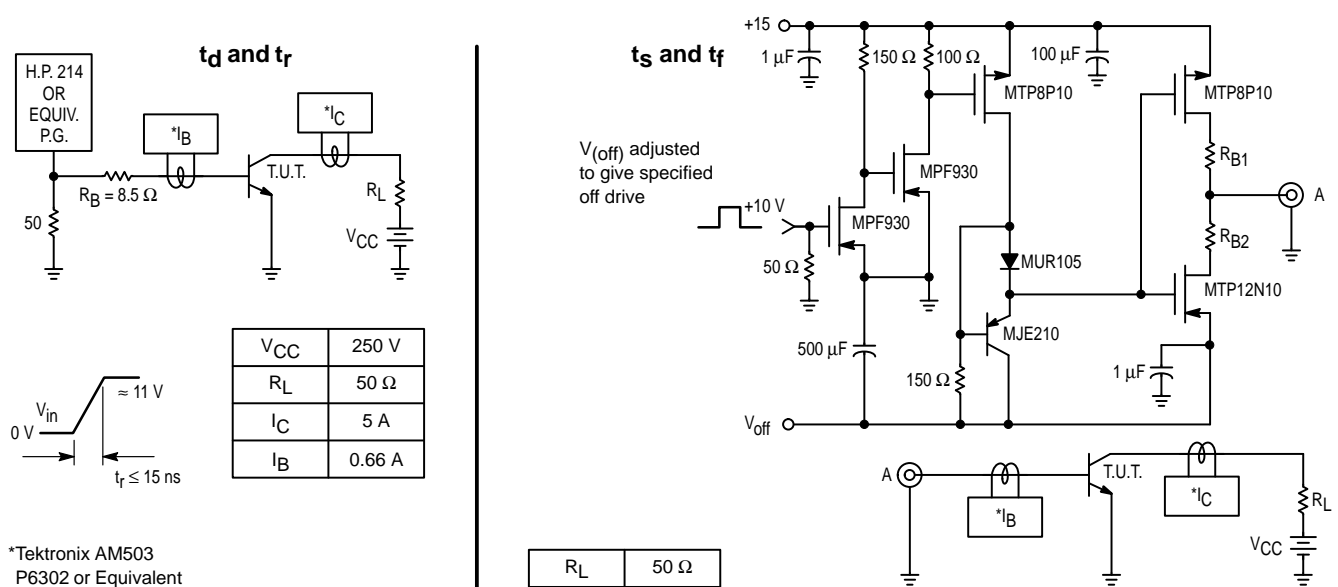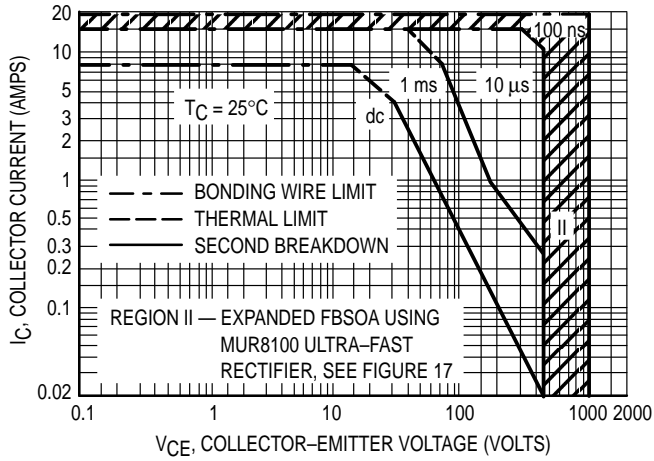

Figure 12. Inductive Switching Measurements
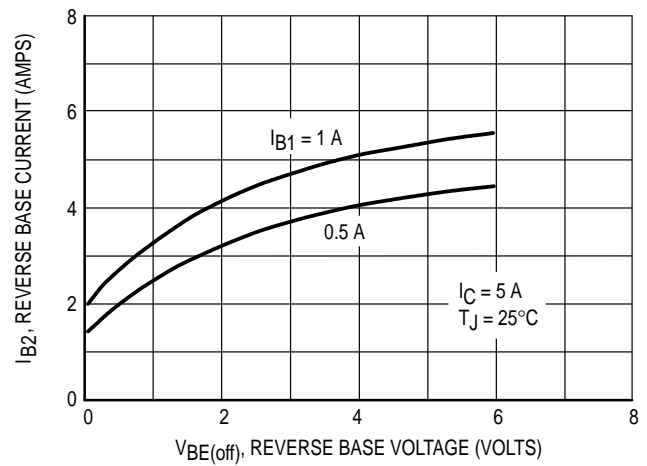
Figure 13. Peak Reverse Base Current

Table 2. Resistive Load Switching

t_d and t_r

t_S and t_f

V_{CC}	250 V
R_L	50 Ω
I_C	5 A
I_B	0.66 A

t_r ≤ 15 ns

*Tektronix AM503
 P6302 or Equivalent

$V_{(off)}$ adjusted
to give specified
off drive

R_L	50 Ω

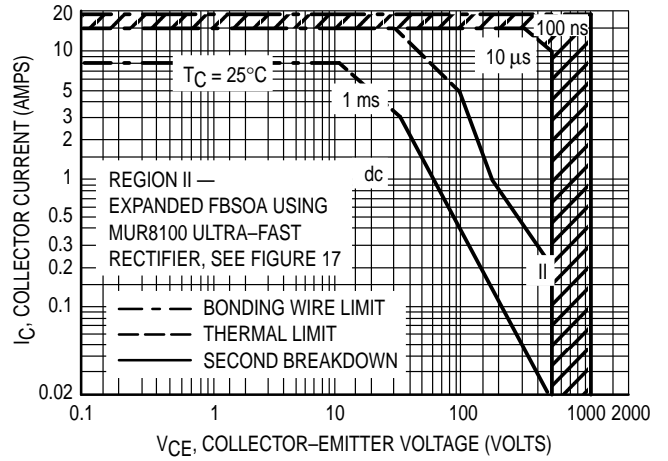## GUARANTEED SAFE OPERATING AREA LIMITS

a. MJ16006A

a. MJH16006A

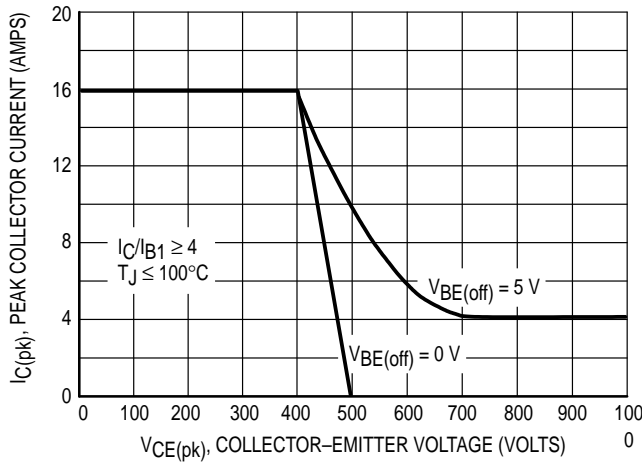**Figure 14. Maximum Rated Forward Biased Safe Operating Area**

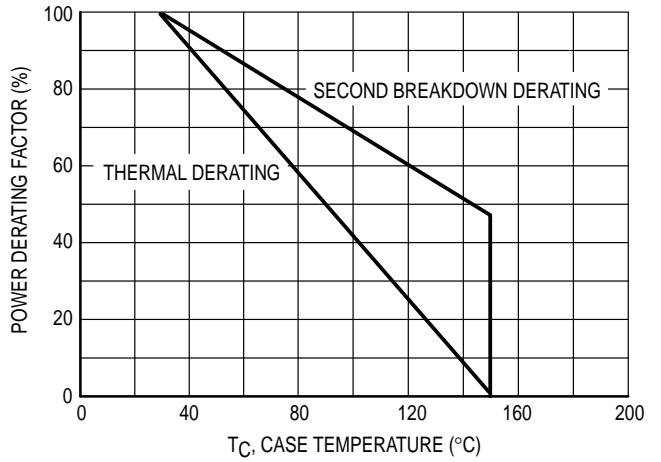**Figure 15. Maximum Reverse Biased Safe Operating Area**
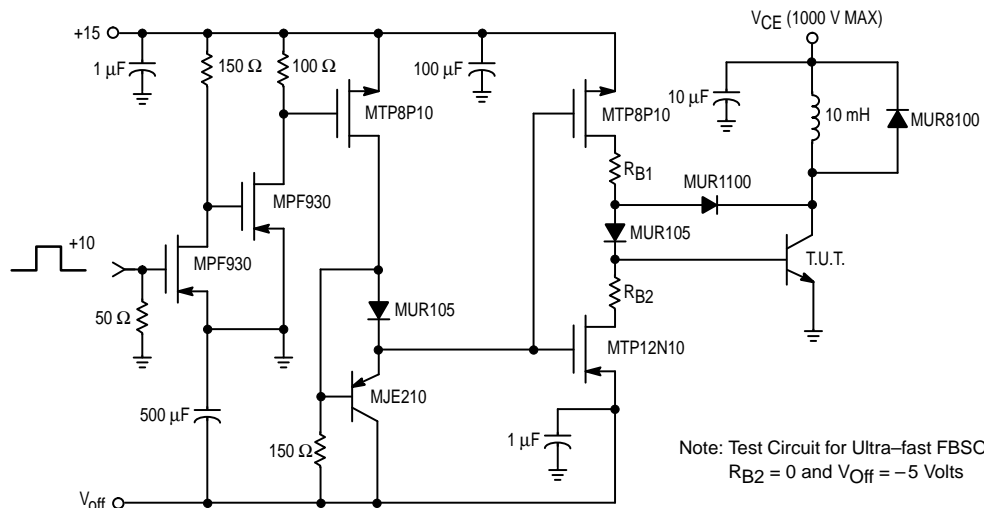

Figure 16. Power Derating

Figure 17. Switching Safe Operating Area

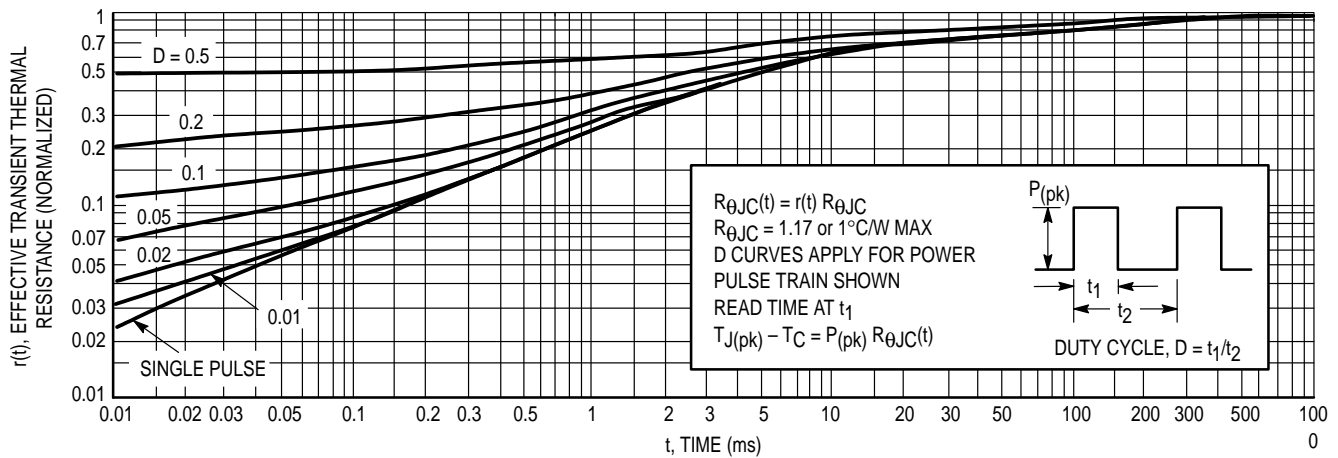Figure 18. Thermal Response

Inside the figure:

$$R_{\theta JC}(t) = r(t)\, R_{\theta JC}$$
$R_{\theta JC} = 1.17$ or $1°C/W$ MAX
D CURVES APPLY FOR POWER
PULSE TRAIN SHOWN
READ TIME AT t_1
$$T_{J(pk)} - T_C = P_{(pk)}\, R_{\theta JC}(t)$$
DUTY CYCLE, $D = t_1/t_2$

Axis labels: r(t), EFFECTIVE TRANSIENT THERMAL RESISTANCE (NORMALIZED); t, TIME (ms)

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second break-down. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 14a and 14b is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second break-down pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figures 14a and 14b may be found at any case temperature by using the appropriate curve on Figure 16.

$T_{J(pk)}$ may be calculated from the data in Figure 18. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base–to–emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Biased Safe Operating Area and represents the voltage current condition allowable during reverse biased turnoff. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 15 gives the RBSOA character-istics.

SWITCHMODE III DESIGN CONSIDERATIONS

1. FBSOA —

Allowable dc power dissipation in bipolar power transistors decreases dramatically with increasing collector emitter voltage. A transistor which safely dissipates 100 watts at 10 volts will typically dissipate less than 10 watts at its rated $V_{CEO(sus)}$. From a power handling point of view, current and voltage are not interchangeable (see Application Note AN875).

2. TURN–ON —

Safe turn–on load line excursions are bounded by pulsed FBSOA curves. The 10 μs curve applies for resistive loads, most capacitive loads, and inductive loads that are clamped by standard or fast recovery rectifiers. Similarly, the 100 ns curve applies to inductive loads which are clamped by ultra–fast recovery rectifiers, and are valid for turn–on crossover times less than 100 ns (see Application Note AN952).

At voltages above 75% of $V_{CEO(sus)}$, it is essential to pro-vide the transistor with an adequate amount of base drive VERY RAPIDLY at turn–on. More specifically, safe operation according to the curves is dependent upon base current rise time being less than collector current rise time. As a general rule, a base drive compliance voltage in excess of 10 volts is required to meet this condition (see Application Note AN875).

3. TURN–OFF —

A bipolar transistor's ability to withstand turn–off stress is dependent upon its forward base drive. Gross overdrive vio-lates the RBSOA curve and risks transistor failure. For this reason, circuits which use fixed base drive are often more likely to fail at light loads due to heavy overdrive (see Ap-plication Note AN875).

4. OPERATION ABOVE $V_{CEO(sus)}$ —

When bipolars are operated above collector–emitter breakdown, base drive is crucial. A rapid application of ade-quate forward base current is needed for safe turn–on, as is a stiff negative bias needed for safe turn–off. Any hiccup in the base–drive circuitry that even momentarily violates either of these conditions will likely cause the transistor to fail. Therefore, it is important to design the driver so that its out-put is negative in the absence of anything but a clean crisp input signal (see Application Note AN952).

SWITCHMODE DESIGN CONSIDERATIONS (Cont.)

5. RBSOA —

Reverse Biased Safe Operating Area has a first order dependency on circuit configuration and drive parameters. The RBSOA curves in this data sheet are valid only for the conditions specified. For a comparison of RBSOA results in several types of circuits (see Application Note AN951).

6. DESIGN SAMPLES —

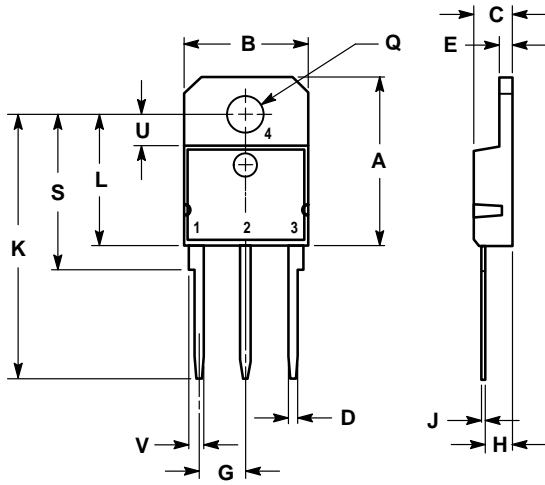Transistor parameters tend to vary much more from wafer lot to wafer lot, over long periods of time, than from one device to the next in the same wafer lot. For design evaluation it is advisable to use transistors from several different date codes.

7. BAKER CLAMPS —

Many unanticipated pitfalls can be avoided by using Baker Clamps. MUR105 and MUR1100 diodes are recommended for base drives less than 1 amp. Similarly, MUR405 and MUR4100 types are well–suited for higher drive requirements (see Article Reprint AR131).

PACKAGE DIMENSIONS

	MILLIMETERS		INCHES	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A	19.00	19.60	0.749	0.771
B	14.00	14.50	0.551	0.570
C	4.20	4.70	0.165	0.185
D	1.00	1.30	0.040	0.051
E	1.45	1.65	0.058	0.064
G	5.21	5.72	0.206	0.225
H	2.60	3.00	0.103	0.118
J	0.40	0.60	0.016	0.023
K	28.50	32.00	1.123	1.259
L	14.70	15.30	0.579	0.602
Q	4.00	4.25	0.158	0.167
S	17.50	18.10	0.689	0.712
U	3.40	3.80	0.134	0.149
V	1.50	2.00	0.060	0.078

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 340D–01
ISSUE A

MOTOROLA

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