

*Advance Information*  
**Field Programmable  
Analog Array  
20-Cell Version**

**MPAA020**

**FIELD PROGRAMMABLE  
ANALOG ARRAY**

The MPAA020 is a field programmable analog array based on a general purpose analog cell that may be configured, either alone or in combinations, as any of a wide range of analog functions from simple comparators to complex filters. These cells are arranged in a 4 x 5 array with supporting circuitry to provide input/output signal buffering, programmable reference voltages, cell to cell interconnections, etc. Each cell's function may be programmed to connect with any of the other cells in the array. Unused cells are powered down individually to minimize power dissipation. Digital interface circuitry is provided to write the analog circuit configuration data to on-chip SRAM in the same manner as Motorola's digital FPGAs (serial & parallel PROM, and microprocessor mode).

Analog circuit design is simplified with EasyAnalog™ Design Software, which handles bit level circuit configuration details, allowing the user to do analog design using functional macros in an easy to use point-and-click graphical environment.

**Table 1: Hardware Features**

Feature	Value
Number of Programmable Cells	20
Analog I/O Cells	13
Anti-aliasing/Smoothing Filtering	Sallen-Key External RC
Additional Auxiliary Opamps	8
Internal Voltage Reference	8-Bit Programmable
Internal Clock Dividers	4 Independent 5-Bit Dividers
Package	160-Pin QFP

This document contains information on a new product. Specifications and information herein are subject to change without notice.



**Table 2: EasyAnalog Design Software Macros**

Macro Type	Definable Parameters	Range
Comparator	Inverting/Non-inverting Reference level One/Two Input	V <sub>MR</sub> ±2.5 volts
Filters	Low Pass/ High Pass/Band Pass/Band Stop Single-Pole/Biquad/Cosine Filter Pass Band Gain(s)	±(0.004 to 20)
	Q	0.5 to 255
	Corner Frequencies	F <sub>clk</sub> /250 to F <sub>clk</sub> /10
Gain Stages	Inverting/Noninverting/Summing Offset compensating Gain Value	±(0.004 to 20)
Oscillators	Square Wave/Sine Wave Frequency	F <sub>clk</sub> /1000 to F <sub>clk</sub> /4
Rectifiers	Full/Half Wave Inverting/Noninverting Gain	±(0.004 to 20)
	Low Pass Pole	F <sub>clk</sub> /250 to F <sub>clk</sub> /10
Signal Conditioning	Sample-and-Hold Track-and-Hold	
Miscellaneous	Differentiator / Integrators / Limiter	0.1 to 2.5 volts
	Ramp Generator	< 1 Hz to >20 kHz

**Table 3: Performance Specifications**

Specification	Typical Value
System Master Clock Frequency ( <b>clock</b> )	TBD
Internal Sampling Clock Rate	1 MHz (max)
Maximum Signal Frequency – Recommended – Nyquist	200 kHz 500 kHz
Input Signal Range	0.5 to (V <sub>dd</sub> – 0.5)
Analog Output Drive	100 pF (max) 1 kohm (min)
DC Offset	< 10 mV
Harmonic Distortion – 1 kHz – 200 kHz	< 0.1% < 0.5%
Differential Non-Linearity	< 0.15 LSB
Integral Non-Linearity	< 0.24 LSB
Slew Rate	10 V/usec
Signal to Noise Ratio (SNR)	> 60 dB
Power Supply Rejection Ratio (PSRR)	TBD
Power Dissipation (max)	200 mW
Each cell individually selectable	(10 mW/cell)
Operating Temperature Range	–40 to + 85°C

**Table 4: Recommended Operating Conditions**

Symbol	Parameter	Min	Max	Unit
AVDD, BVDD, DVDD, SVDD	DC Supply Voltages	4.5	5.5	V
V <sub>in</sub>	Input Voltage	Analog Digital – VOH Digital – VOL	VDD – 0.5 DVDD 0.8	V

**Table 5: Absolute Maximum Ratings**

Symbol	Parameter	Min	Max	Unit
AVDD, BVDD, DVDD, SVDD	DC Supply Voltages	–0.5	6.5	V
V <sub>in</sub>	Input Voltage	–0.5	VDD + 0.5	V
T <sub>A</sub>	Operating Temperature Range	–40	85	C
T <sub>stg</sub>	Storage Temperature	–65	150	C

**Table 6: Pin Descriptions**

Pin	Pin Name	Type	Description	
1	por	Digital Input	Power On Reset	
2	mode0	Digital Input	Configuration mode control pins	
3	mode1	Digital Input		
4	mode2	Digital Input		
5	mode3	Digital Input		
6	cfg_clk	Digital Input		External Configuration Clock
7	DClk	Digital Output		Internal Configuration Clock
8	Data0	Digital Input		Data Pins Used for Loading Configuration Data
9	Data1	Digital Input		
10	Data2	Digital Input		
11	Data3	Digital Input		
12	Data4	Digital Input		
13	Data5	Digital Input		
14	Data6	Digital Input		
15	Data7	Digital Input	Address Pins Used for Loading Configuration Data	
16	A0	Digital Output		
17	A1	Digital Output		
18	A2	Digital Output		
19	A3	Digital Output		
20	A4	Digital Output		
21	A5	Digital Output		
22	A6	Digital Output		

Table 6: Pin Descriptions

Pin	Pin Name	Type	Description
23	A7	Digital Output	Address Pins Used for Loading Configuration Data
24	A8	Digital Output	
25	A9	Digital Output	
26	A10	Digital Output	
27	A11	Digital Output	
28	A12	Digital Output	
29	A13	Digital Output	
30	A14	Digital Output	
31	A15	Digital Output	
32	A16	Digital Output	
33	A17	Digital Output	
34	F1 ( $\overline{\text{ERR}}$ , $\overline{\text{RD}}$ )	Digital I/O	Configuration Function Pins
35	F2 ( $\overline{\text{MEMCE}}$ , $\overline{\text{WR}}$ )	Digital I/O	
36	F0 ( $\overline{\text{BFR}}$ , $\overline{\text{CS}}$ )	Digital I/O	
37	F3 ( $\overline{\text{PWRUP}}$ , $\overline{\text{RS}}$ )	Digital I/O	
38	F4 ( $\overline{\text{END}}$ , $\overline{\text{BUSY}}$ )	Digital I/O	
39	opampDisable	Digital Input	Array opamp power-down
40	reset	Digital Input	Chip RESET
41	No Connect	Unused	
42	No Connect	Unused	
43	No Connect	Unused	
44	No Connect	Unused	
45	No Connect	Unused	
46	No Connect	Unused	
47	No Connect	Unused	
48	No Connect	Unused	
49	ioLDX	Analog Input	Unbuffered Analog Input
50	ioLDY	Analog Input	Buffered Analog Input
51	ioLDZ	Analog Output	Buffered Analog Output
52	No Connect		
53	ioLDZ2	Analog Output	Uncommitted Opamp Output
54	ioLDY2	Analog Input	Uncommitted Opamp Input
55	No Connect	Unused	
56	ioLCY2	Analog Input	Uncommitted Opamp Input
57	ioLCZ2	Analog Output	Uncommitted Opamp Output

Table 6: Pin Descriptions


Pin	Pin Name	Type	Description
58	No Connect		
59	<b>ioLCZ</b>	Analog Output	Uncommitted Opamp Output
60	<b>ioLCY</b>	Analog Input	Buffered Analog Input
61	<b>ioLCX</b>	Analog Input	Unbuffered Analog Input
62	<b>avdd</b>	Power Supply	Analog VDD; 5 volts
63	<b>avss</b>	Power Supply	Analog VSS; 0 volts
64	<b>svss</b>	Power Supply	Substrate VSS; 0 volts
65	<b>ioLBX</b>	Analog Input	Unbuffered Analog Input
66	<b>ioLBY</b>	Analog Input	Buffered Analog Input
67	<b>ioLBZ</b>	Analog Output	Buffered Analog Output
68	<b>ioLBZ2</b>	Analog Output	Uncommitted Opamp Output
69	<b>ioLBY2</b>	Analog Input	Uncommitted Opamp Input
70	No Connect	Unused	
71	<b>ioLAY2</b>	Analog Input	Uncommitted Opamp Input
72	<b>ioLAZ2</b>	Analog Output	Uncommitted Opamp Output
73	<b>ioLAZ</b>	Analog Output	Uncommitted Opamp Output
74	<b>ioLAY</b>	Analog Input	Buffered Analog Input
75	<b>ioLAX</b>	Analog Input	Unbuffered Analog Input
76	<b>bvdd</b>	Power Supply	VDD; 5 volts
77	<b>bvss</b>	Power Supply	VSS; 0 volts
78	No Connect	Unused	
79	No Connect	Unused	
80	No Connect	Unused	
81	<b>vrefOut</b>	Analog Output	Reference Voltage
82	<b>vmr</b>	Analog Output	Signal Ground; 2.5 volts
83	<b>opamp_vmr</b>	Analog Output	Signal Ground; 2.5 volts
84	<b>cext</b>		External VMR capacitor
85	No Connect	Unused	
86	<b>ioD5Z</b>	Analog Output	Uncommitted Opamp Output
87	<b>ioD5Y</b>	Analog Input	Buffered Analog Input
88	<b>ioD5X</b>	Analog Input	Unbuffered Analog Input
89	No Connect	Unused	
90	No Connect	Unused	
91	No Connect	Unused	
92	<b>ioD4Z</b>	Analog Output	Uncommitted Opamp Output

Table 6: Pin Descriptions

Pin	Pin Name	Type	Description
93	<b>ioD4Y</b>	Analog Input	Buffered Analog Input
94	<b>ioD4X</b>	Analog Input	Unbuffered Analog Input
95	No Connect	Unused	
96	<b>esd_vdd</b>	Power Supply	VDD; 5 volts
97	<b>esd_vss</b>	Power Supply	VSS; 0 volts
98	No Connect	Unused	
99	No Connect	Unused	
100	No Connect	Unused	
101	<b>ioD3Z</b>	Analog Output	Uncommitted Opamp Output
102	<b>ioD3Y</b>	Analog Input	Buffered Analog Input
103	<b>ioD3X</b>	Analog Input	Unbuffered Analog Input
104	No Connect	Unused	
105	No Connect	Unused	
106	<b>ioD2Z</b>	Analog Output	Uncommitted Opamp Output
107	<b>ioD2Y</b>	Analog Input	Buffered Analog Input
108	<b>ioD2X</b>	Analog Input	Unbuffered Analog Input
109	No Connect	Unused	
110	No Connect	Unused	
111	No Connect	Unused	
112	<b>ioD1Z</b>	Analog Output	Uncommitted Opamp Output
113	<b>ioD1Y</b>	Analog Input	Buffered Analog Input
114	<b>ioD1X</b>	Analog Input	Unbuffered Analog Input
115	No Connect	Unused	
116	No Connect	Unused	
117	No Connect	Unused	
118	No Connect	Unused	
119	No Connect	Unused	
120	No Connect	Unused	
121	No Connect	Unused	
122	No Connect	Unused	
123	No Connect	Unused	
124	No Connect	Unused	
125	No Connect	Unused	
126*	<b>ioRAX</b>	Analog Input	Unbuffered Analog Input
127	<b>ioRAY</b>	Analog Input	Buffered Analog Input

Table 6: Pin Descriptions

Pin	Pin Name	Type	Description
128	ioRAZ	Analog Output	Buffered Analog Output
129	ioRAZ2	Analog Output	Uncommitted Opamp Output
130	ioRAY2	Analog Input	Uncommitted Opamp Input
131	No Connect	Unused	
132	ioRBY2	Analog Input	Uncommitted Opamp Input
133	ioRBZ2	Analog Output	Uncommitted Opamp Output
134	ioRBZ	Analog Output	Buffered Analog Output
135	ioRBY	Analog Input	Buffered Analog Input
136	ioRBX	Analog Input	Unbuffered Analog Input
137	cfg_vdd	Power Supply	Digital VDD; 5 volts
138	svss	Power Supply	Substrate VSS; 0 volts
139	svdd	Power Supply	Substrate VDD; 5 volts
140	clock	Digital Input	System Master Clock
141	No Connect	Unused	
142	ioRCX	Analog Input	Unbuffered Analog Input
143	ioRCY	Analog Input	Buffered Analog Input
144	ioRCZ	Analog Output	Buffered Analog Output
145	ioRCZ2	Analog Output	Uncommitted Opamp Output
146	ioRCY2	Analog Input	Uncommitted Opamp Input
147	No Connect	Unused	
148	ioRDY2	Analog Input	Uncommitted Opamp Input
149	ioRDZ2	Analog Output	Uncommitted Opamp Output
150	cfg_vss	Power Supply	Digital config logic VSS; 0 volts
151	No Connect	Unused	
152	ioRDZ	Analog Output	Buffered Analog Output
153	ioRDY	Analog Input	Buffered Analog Input
154	ioRDY	Analog Input	Unbuffered Analog Input
155	No Connect	Unused	
156	No Connect	Unused	
157	No Connect	Unused	
158	No Connect	Unused	
159	No Connect	Unused	
160	No Connect	Unused	

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