MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

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MPC2104P
MPC2105P

Product Preview

256KB/512KB BurstRAM™ Secondary Cache Modules for PowerPC™ PReP/CHRP Platforms

The MPC2104P (256KB) and MPC2105P (512KB) are designed to provide burstable, high performance L2 cache for the PowerPC 60x microprocessor family in conformance with the PowerPC Reference Platform (PReP) and the PowerPC Common Hardware Reference Platform (CHRP) specifications.

The MPC2104P and MPC2105P utilize synchronous BurstRAMs. The MPC2104P module is configured as 32K x 64 bits and uses two of the 3.3 V 32K x 32 data RAMs. The MPC2105P is configured as 64K x 64 bits and uses two of the 3.3 V 64K x 32 data RAMs. Both modules are in a 178 (89 x 2) pin DIMM format. For tag bits on the 2104P, a 5 V cache tag RAM configured as 8K x 14 for tag field plus 8K x 2 for valid and dirty status bits is used. For tag bits on the 2105P, a 5 V cache tag RAM configured as 16K x 14 for tag field plus 16K x 2 for valid and dirty status bits is used.

Bursts can be initiated with the ADS signal. Subsequent burst addresses are generated internally to the BurstRAM by the CNTEN signal.

Write cycles are internally self–timed and are initiated by the rising edge of the clock (CLKx) inputs. Writes are global with two inputs for reduced loading.

Presence detect pins are available for auto configuration of the cache control.

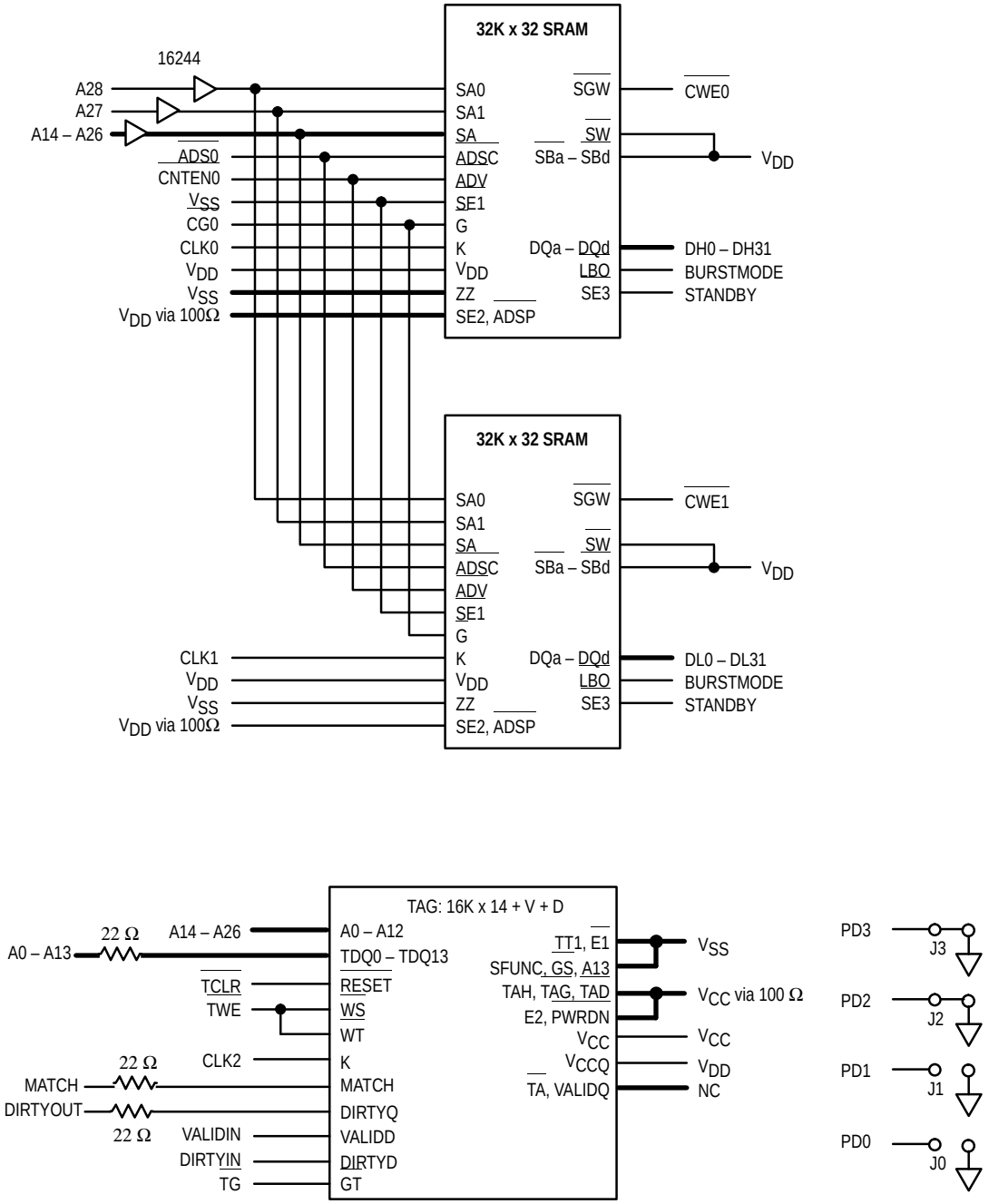
The module family pinout will support 5 V and 3.3 V components for a clear path to lower voltage and power savings. Both power supplies must be connected.

All of these cache modules are plug and pin compatible with each other.

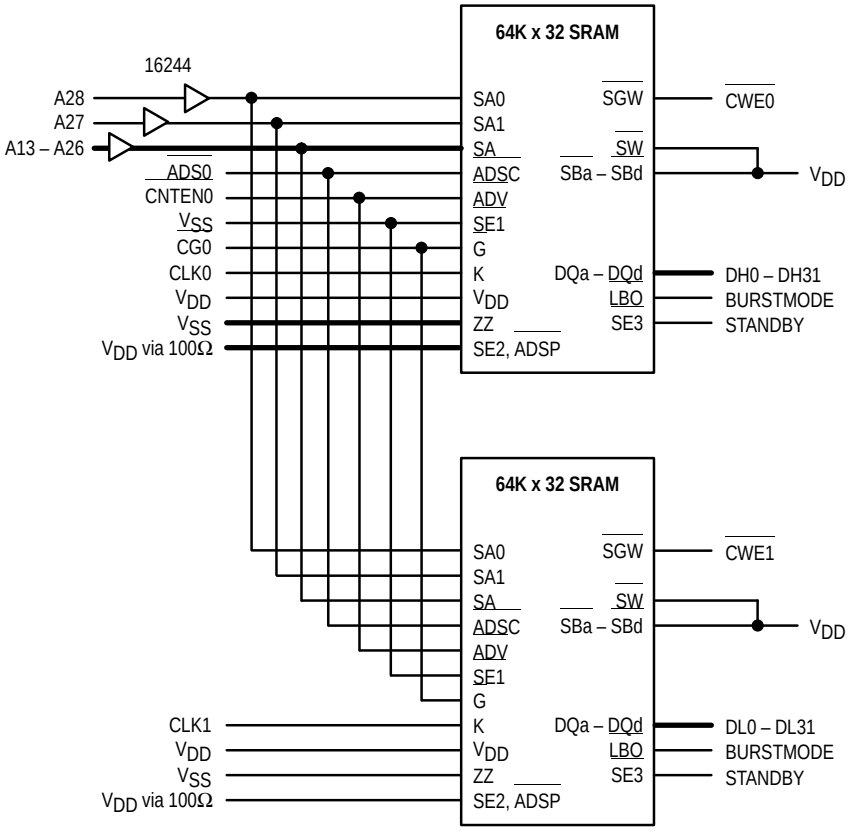
- PowerPC–Style Burst Counter On Chip
- Pipeline Data I/O
- Plug and Pin Compatibility
- Multiple Clock Pins for Reduced Loading
- All Cache Data and Tag I/Os are LVTTL (3.3 V) Compatible
- Three State Outputs
- Buffered Addresses to Data RAMs for Reduced Loading
- Fast Module Clock Rates: Up to 66 MHz
- Fast SRAM Access Times: 9 ns for Tag RAM Match
  8 ns for Data RAM
- Decoupling Capacitors for Each Fast Static RAM
- High Quality Multi–Layer FR4 PWB With Separate Power and Ground Planes
- 178 Pin Card Edge Module
- Burndy Connector, Part Number: ELF178KSC–3Z50

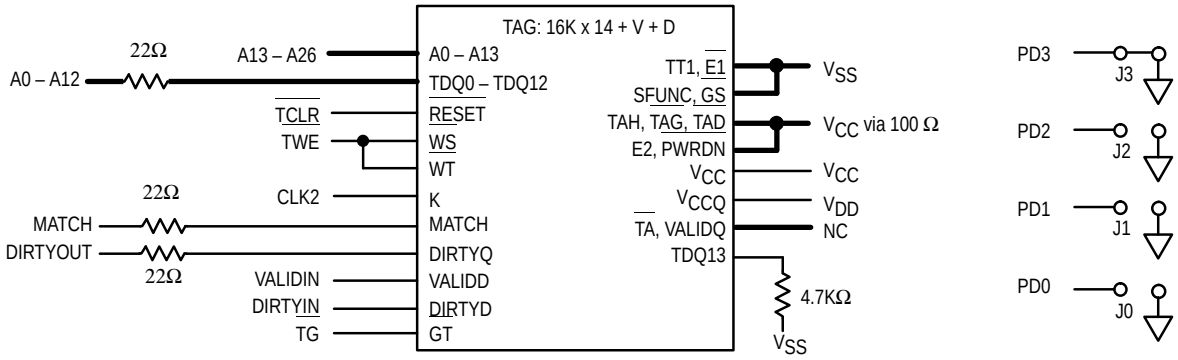
REV 2
12/20/96

MPC2104P BLOCK DIAGRAM



MPC2105P BLOCK DIAGRAM



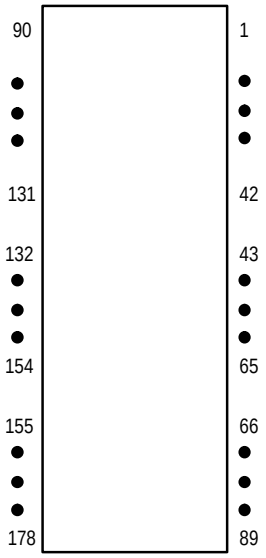


PIN ASSIGNMENT 178–LEAD DIMM

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	27	DH0	53	DL1	79	V_{SS}	105	DH14	131	DL17	157	A22
2	PD0/IDSCLK	28	NC	54	DL0	80	A7	106	DH13	132	NC	158	A20
3	PD2	29	V_{SS}	55	V_{SS}	81	A5	107	NC	133	DL15	159	V_{SS}
4	DH30	30	CLK1	56	CLK2	82	A3	108	DH10	134	DL13	160	A18
5	DH28	31	V_{SS}	57	V_{SS}	83	A0	109	DH8	135	V_{SS}	161	A16
6	DH26	32	DL28	58	NC	84	V_{CC}	110	NC	136	DL10	162	A15
7	DH24	33	DL26	59	$\overline{CG0}$	85	$\overline{TCLR}$	111	DH6	137	DL8	163	A14
8	V_{DD}	34	DL24	60	NC	86	MATCH	112	V_{DD}	138	$\overline{CWE1}$	164	V_{DD}
9	NC	35	NC	61	V_{DD}	87	$\overline{TG}$	113	DH4	139	DL6	165	A10
10	DH22	36	NC	62	NC	88	DIRTYIN	114	V_{SS}	140	V_{DD}	166	A8
11	DH20	37	DL22	63	RESERVED	89	V_{SS}	115	CLK0	141	DL5	167	A6
12	DH19	38	DL20	64	ADS0	90	V_{SS}	116	V_{SS}	142	DL2	168	V_{SS}
13	V_{SS}	39	DL18	65	NC	91	PD1/IDSDATA	117	DH1	143	V_{SS}	169	A4
14	DH17	40	DL16	66	A28	92	PD3	118	NC	144	NC	170	A2
15	NC	41	V_{SS}	67	A26	93	DH31	119	DL31	145	V_{SS}	171	A1
16	DH15	42	NC	68	A25	94	DH29	120	DL30	146	NC	172	BURSTMODE
17	DH12	43	DL14	69	A23	95	DH27	121	V_{SS}	147	V_{SS}	173	V_{CC}
18	NC	44	DL12	70	V_{SS}	96	DH25	122	DL29	148	CWE0	174	VALIDIN
19	DH11	45	DL11	71	A21	97	V_{DD}	123	DL27	149	NC	175	TWE
20	DH9	46	V_{SS}	72	A19	98	NC	124	DL25	150	V_{DD}	176	STANDBY
21	NC	47	DL9	73	A17	99	DH23	125	NC	151	NC	177	DIRTYOUT
22	DH7	48	NC	74	A13	100	DH21	126	NC	152	RESERVED	178	V_{SS}
23	V_{DD}	49	DL7	75	V_{DD}	101	DH18	127	DL23	153	CNTEN0		
24	DH5	50	DL4	76	A12	102	V_{SS}	128	DL21	154	NC		
25	DH3	51	V_{DD}	77	A11	103	DH16	129	DL19	155	A27		
26	DH2	52	DL3	78	A9	104	NC	130	V_{SS}	156	A24		

NOTE: V_{CC} and V_{DD} must be connected on all modules.

TOP VIEW – CASE TBD



PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
66, 67, 68, 69, 71, 72, 73, 74, 76, 77, 78, 80, 81, 82, 83, 155, 156, 157, 158, 160, 161, 162, 163, 165, 166, 167, 169, 170, 171	A0 – A28	Input	Address Inputs — (MSB:0, LSB:28).
64	ADS0	Input	Data RAM Address Strobe.
172	BURSTMODE	Input	Burstmode. 0 = Linear, 1 = Interleaved.
59	$\overline{CG0}$	Input	Data RAM Output Enable.
30, 56, 115	CLK0 – CLK2	Input	Clock Inputs — CLK2 is for Tag RAM, CLK0 and CLK1 are for Data RAMs only.
153	$\overline{CNTEN0}$	Input	Data RAM Count Enable.
138, 148	$\overline{CWE0}$ – $\overline{CWE1}$	Input	Data RAM Write Enables — (MSB:0, LSB:1).
4, 5, 6, 7, 10, 11, 12, 14, 6, 17, 19, 20, 22, 24, 25, 26, 27, 93, 94, 95, 96, 99, 100, 101, 103, 105, 106, 108, 109, 111, 113, 117	DH0 – DH31	I/O	High Data Bus — (MSB:0, LSB:31).
88	DIRTYIN	Input	Dirty input bit.
177	DIRTYOUT	Output	Dirty output bit.
32, 33, 34, 37, 38, 39, 40, 43, 44, 45, 47, 49, 50, 52, 53, 54, 119, 120, 122, 123, 124, 127, 128, 129, 131, 133, 134, 136, 137, 139, 141, 142	DL0 – DL31	I/O	Low Data Bus — (MSB:0, LSB:31).
86	MATCH	Output	Tag RAM active high match indication.
2	PD0/IDSCLK	Input	Presence detect bit 0/EEPROM serial clock. (EEPROM option only).
91	PD1/IDSDATA	I/O	Presence detect bit 1/EEPROM serial data. (EEPROM option only).
3, 92	PD2, PD3	Output	Presence detect bits.
63, 152	RESERVED		Reserved pin.
176	STANDBY	Input	Standby pin. Reduces standby power consumption.
85	TCLR	Input	Tag RAM clear.
87	TG	Input	Tag RAM output enable.
175	TWE	Input	Tag RAM write enable.
174	VALIDIN	Input	Tag RAM valid bit.
84, 173	V_{CC}	Input	+ 5 V power supply. Must be connected.
8, 23, 51, 61, 75, 97, 112, 140, 150, 164	V_{DD}	Input	+ 3.3 V power supply. Must be connected.
1, 13, 29, 31, 41, 46, 55, 57, 70, 79, 89, 90, 102, 114, 116, 121, 130, 135, 143, 145, 147, 159, 168, 178	V_{SS}	Input	Ground.
9, 15, 18, 21, 28, 35 – 36, 42, 48, 58, 60, 62, 65, 98, 104, 107, 110, 118, 125 – 126, 132, 144, 146, 149, 151, 154	NC	—	There is no connection to the module.

TRUTH TABLE (See Notes 1 through 4)

Next Cycle	Address Used	Standby	$\overline{ADS0}$	$\overline{CNTEN0}$	$\overline{CG0}$ [2]	DHx/DLx	$\overline{CWEx}$ [2]
Deselect	None	1	0	X	X	High–Z	X
Begin Read	External	0	0	X	X	High–Z	1[4]
Continue Read	Next	X	1	0	1	High–Z	1
Continue Read	Next	X	1	0	0	DQ	1
Suspend Read	Current	X	1	1	1	High–Z	1
Suspend Read	Current	X	1	1	0	DQ	1
Begin Write	External	0	0	X	X	High–Z	0
Continue Write	Next	X	1	0	X	High–Z	0
Suspend Write	Current	X	1	1	X	High–Z	0

NOTES:
1. X = Don't Care. 1 = logic high. 0 = logic low.
2. CG0 is an asynchronous signal and is not sampled by the clock CLK0. $\overline{CG0}$ drives the bus immediately (t_{GLQX}) following $\overline{CG0}$ going low.
3. On write cycles that follow read cycles, CG0 must be negated prior to the start of the write cycle to ensure proper write data setup times. CG0 must also remain negated at the completion of the write cycle to ensure proper write data hold times.
4. This READ assumes the RAM was previously deselected.

ASYNCHRONOUS TRUTH TABLE

Operation	$\overline{CG0}$	I/O Status
Read	L	Data Out (DHx/DLx)
Read	H	High–Z
Write	X	High–Z
Deselected	X	High–Z
Sleep	X	High–Z

LINEAR BURST ADDRESS TABLE (Burst Mode = V_{SS})

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X10	X . . . X11	X . . . X00
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X00	X . . . X01	X . . . X10

INTERLEAVED BURST ADDRESS TABLE (Burst Mode = V_{DD})

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X00	X . . . X11	X . . . X10
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X10	X . . . X01	X . . . X00

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating		Symbol	Value	Unit
Power Supply Voltage	Tag Data RAM	V_{CC} V_{DD}	– 0.5 to + 7.0 – 0.5 to + 4.6	V
Voltage Relative to V_{SS}	Tag Data RAM	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5 – 0.5 to V_{DD} + 0.5	V
Output Current (per I/O)	Tag Data RAM	I_{out}	± 20 ± 30	mA
Power Dissipation		P_D	3.86	W
Temperature Under Bias		T_{bias}	– 10 to + 85	°C
Operating Temperature		T_A	0 to +70	°C
Storage Temperature		T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, V_{DD} = 3.3 V + 10%, – 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC} V_{DD}	4.75 3.135	5.25 3.60	V
Input High Voltage	V_{IH}	2.2	V_{DD} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
**V_{IH} (max) = V_{DD} + 0.3 V dc; V_{IH} (max) = V_{DD} + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{DD})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{CG}$ = V_{IH}, V_{out} = 0 to V_{DD})	$I_{lkg(O)}$	—	± 1.0	µA
TTL Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
TTL Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter		Symbol	Max	Unit
AC Supply Current (CG = V_{IH}, E = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ 20 ns)	MPC2104P MPC2105P	I_{DDA}	410 700	mA
		I_{CCA}	320	mA
AC Standby Current (E = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH} V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ 20 ns)	MPC2104P MPC2105P	I_{SB1} (V_{DD})	210 240	mA
		I_{SB1} (V_{CC})	320	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit
Input Capacitance	(A13 – A28) (Data RAM Control Pins) (CLK0 – CLK2) (Tag Control Pins)	C_{in}	15 10 5 5	pF
Tag Output Capacitance	(MATCH, DIRTYOUT)	C_{out}	7	pF
Data RAM Input/Output Capacitance	(DH0 – DH31, DL0 – DL31)	$C_{I/O}$	8	pF
Tag Input/Output Capacitance	(A0 – A11)	$C_{I/O}$	7	pF

DATA RAMs AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, V_{DD} = 3.3 V + 10%, – 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 3 ns

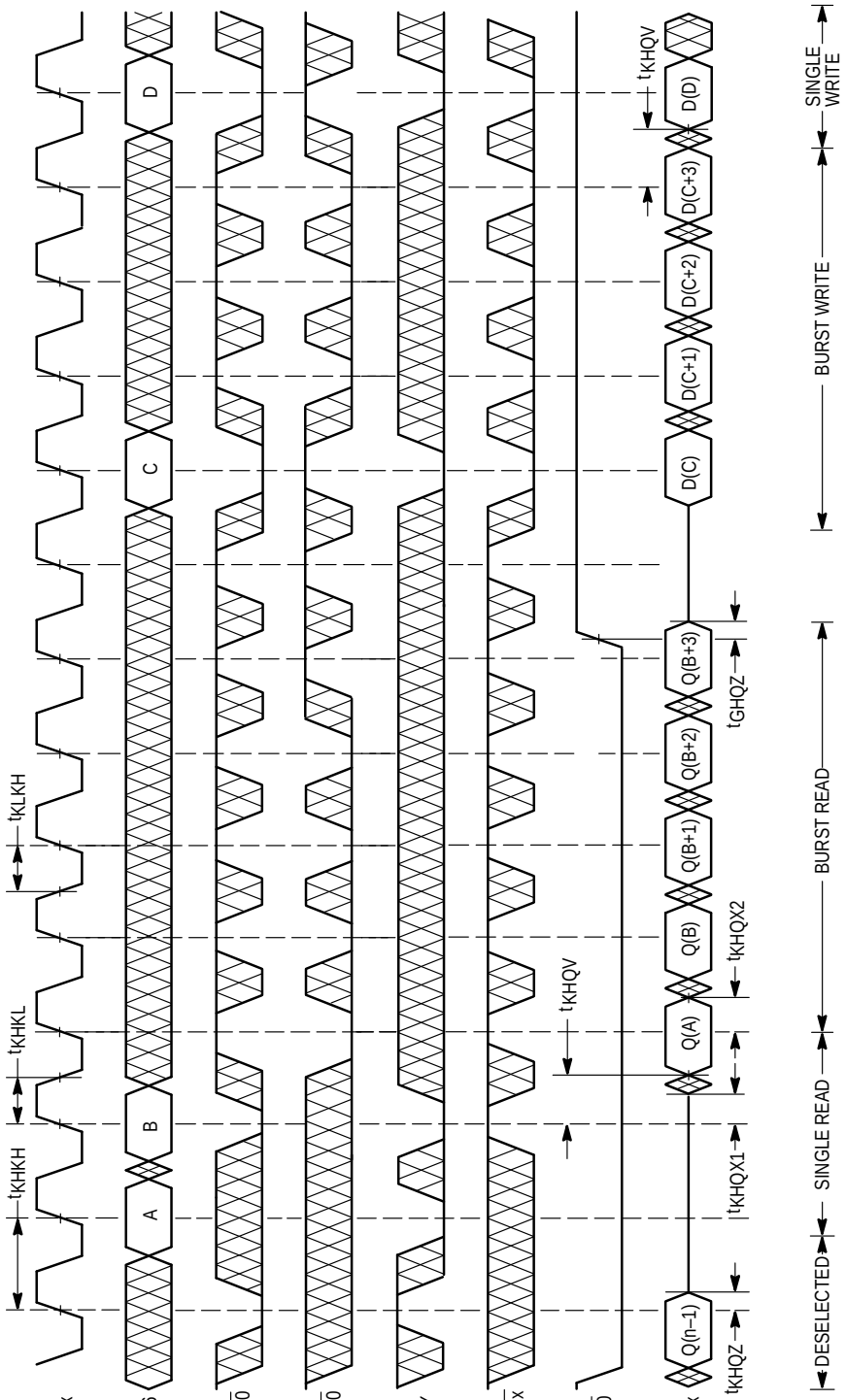
Output Timing Reference Level . . . . . 1.5 V
Output Load . . . . . See Figure 1a Unless Otherwise Noted

SYNCHRONOUS DATA RAMs READ/WRITE CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MPC2104P/5P		Unit	Notes
		Min	Max		
Cycle Time	t_{KHKH}	15	—	ns	
Clock Access Time	t_{KHQV}	—	8	ns	3
Output Enable to Output Valid	t_{GLQV}	—	6	ns	
Clock High to Output Active	t_{KHQX1}	0	—	ns	
Clock High to Output Change	t_{KHQX2}	2	—	ns	
Output Enable to Output Active	t_{GLQX}	0	—	ns	
Output Disable to Q High–Z	t_{GHQZ}	—	8	ns	
Clock High to Q High–Z	t_{KHQZ}	2	8	ns	
Clock High Pulse Width	t_{KHKL}	5	—	ns	
Clock Low Pulse Width	t_{KLKH}	5	—	ns	
Setup Times: Address Address Status Data In Write Address Advance Chip Enable	t_{AVKH} t_{SVKH} t_{DVKH} t_{WVKH} t_{BAVVKH} t_{EVKH}	2.5	—	ns	4
Hold Times: Address Address Status Data In Write Address Advance Chip Enable	t_{KHAX} t_{KHTSX} t_{KHDX} t_{KHWX} t_{KHBAX} t_{KHEX}	0.5	—	ns	4

NOTES:
1. All read and write cycle timings are referenced from CLK or $\overline{CG0}$.
2. CG is a don't care when CWE_X is sampled low.
3. Maximum access times are guaranteed for all possible PowerPC external bus cycles.
4. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of CLK whenever $\overline{ADS0}$ is low, and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of CLK when the chip is enabled. Chip enable must be valid at each rising edge of clock for the device (when ADS0 is low) to remain enabled.

READ/WRITE CYCLES



TAG RAM

RESET FUNCTION TRUTH TABLE (See Notes 1 and 2)

TCLR	CLK	TWE	TAG0 – TAG11	DIRTYOUT	MATCH	Operation	POWER
L	L – H	H	High–Z	L(3)	L(3)	Reset Status	Active
L	L – H	L	—	—	—	Not Allowed	—

NOTES:
1. H = V_{IH}, L = V_{IL}, X = don't care, — = undefined.
2. TG is X for this table.
3. These are output states.

READ FUNCTION TRUTH TABLE (See Notes 1, 2, and 3)

TG	TWE	CLK	TAG0 – TAG11	VALIDIN	DIRTYIN	DIRTYOUT	MATCH	Operation
L	H	X	D_{out}	—	—	D_{out}	D_{out}	Read Tag I/O
H	X	X	High–Z	—	—	—	—	Tag I/O Disable

WRITE FUNCTION TRUTH TABLE (See Notes 1 and 2)

TG	TWE	CLK	TAG0 – TAG11	VALIDIN	DIRTYIN	DIRTYOUT	MATCH	Operation
H	L	L – H	D_{in}	—	—	—	L	Write Tag I/O
L	L	L – H	—	—	—	—	—	Not Allowed

NOTES:
1. H = V_{IH}, L = V_{IL}, X = don't care, — = undefined.
2. This table applies when RESET and PWRDN are high.
3. D_{out} in this case is the same as D_{in}. The input data is written through to the outputs during the write operation.

MATCH FUNCTION TRUTH TABLE (See Notes 1 through 4)

$\overline{TG}$	$\overline{TWE}$	TAG0 – TAG11	VALIDIN(4)	DIRTYIN(4)	MATCH	Operation
X	X	—	—	—	D_{out}	Selected
L	H	D_{out}	—	—	L	Read Tag I/O
H	L	D_{in}	D_{in}	D_{in}	L	Write Tag I/O, Status Bits
H	H	TAG_{in}	L	—	L	Invalid Data — Dedicated Status Bits
H	H	TAG_{in}	H	—	H	Match — Dedicated Status Bits

NOTES:
1. H = V_{IH}, L = V_{IL}, X = don't care, — = undefined.
2. M = high if TAG_{in} equals the memory contents at the address; M = low if TAG_{in} does not equal the contents at that address.
3. PWRDN and RESET are high for this table. GS and CLK are X.
4. This column represents the stored memory cell data for the given status bit at the selected address.

TAG RAM AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 3 ns

Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1a Unless Otherwise Noted

TAG RAM READ CYCLE (See Notes 1 through 4)

Parameter	Symbol	Tag RAM		Unit
		Min	Max	
Clock Access Time	t_{KHQV}	—	10	ns
Output Enable to Output Valid	t_{GLQV}	—	8	ns
Output Enable to Output Active	t_{GLQX}	0	—	ns
Output Disable to Q High–Z	t_{GHQZ}	1	6	ns
Status Bit Hold from Address Change	t_{AXSX}	3	—	ns
Address Access Time Status Bits	t_{AVSV}	—	10	ns
Tag Bit Hold from Address Change	t_{AVQX}	3	—	ns
Address Access Time Tag Bits	t_{AVQV}	—	12	ns

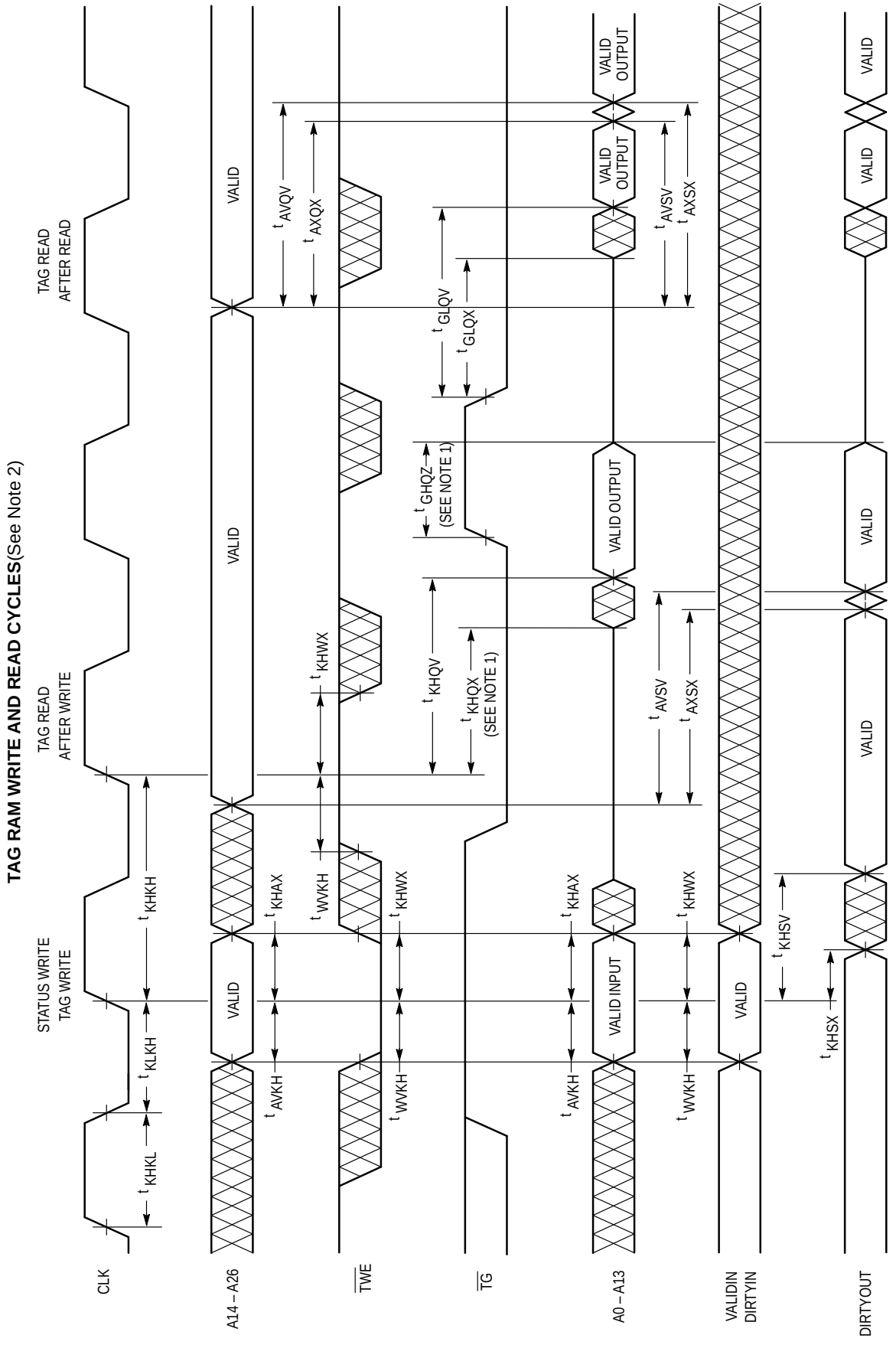
NOTES:
1. Setup and hold times, W (write) refers to $\overline{TWE}$.
2. A read cycle is defined by $\overline{TWE}$ high. A write cycle is defined by $\overline{TWE}$ low.
3. Maximum access times are guaranteed for all possible MC68040 and PowerPC external bus cycles.
4. Tag reads are asynchronous.

TAG RAM WRITE CYCLE (See Notes 1 through 4)

Parameter	Symbol	Tag RAM		Unit
		Min	Max	
Cycle Time	t_{KHKH}	15	—	ns
Clock High Pulse Width	t_{KHKL}	4.5	—	ns
Clock Low Pulse Width	t_{KLKH}	4.5	—	ns
Clock High to Output Active	t_{KHQX}	1.5	—	ns
Setup Times Address Write	t_{AVKH} t_{WVKH}	3	—	ns
Hold Times Address Write	t_{KHAX} t_{KHWX}	1.5	—	ns
Status Output Hold	t_{KHSX}	0	—	ns
Clock High to Status Bits Valid	t_{KHSV}	—	9	ns

NOTES:
1. Setup and hold times, W (write) refers to $\overline{TWE}$.
2. A read cycle is defined by $\overline{TWE}$ high. A write cycle is defined by $\overline{TWE}$ low.
3. Maximum access times are guaranteed for all possible MC68040 and PowerPC external bus cycles.
4. Tag writes are synchronous.

TAG RAM WRITE AND READ CYCLES(See Note 2)



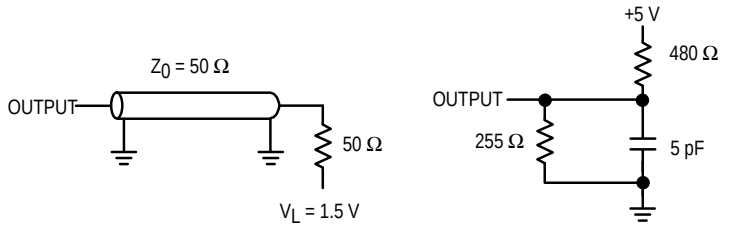
NOTES:
1. Transition is measured plus or minus 200 mV from steady state.
2. $\overline{TCLR}$ = High.

TAG RAM MATCH CYCLE

Parameter	Symbol	Tag RAM		Unit
		Min	Max	
Clock High Write to MATCH Invalid	t_{KHML}	—	7	ns
Clock High Read to MATCH Valid	t_{KHMV}	—	10	ns
Address Valid to MATCH Valid	t_{AVMV}	—	10	ns
MATCH Valid Hold from Address Change	t_{AXMX}	2	—	ns
TG Low to MATCH Invalid	t_{GLML}	—	7	ns
TG High to MATCH Valid	t_{GHMX}	—	8	ns

TAG RAM RESET ($\overline{\text{TCLR}}$) CYCLE

Parameter	Symbol	Tag RAM		Unit
		Min	Max	
$\overline{\text{TCLR}}$ Setup Time	t_{STC}	4	—	ns
$\overline{\text{TCLR}}$ Hold Time	t_{HTC}	1	—	ns
Status Bit Reset Time	t_{SRST}	—	60	ns
Status Bit Hold from $\overline{\text{TCLR}}$ Low	t_{SHRS}	2	—	ns
$\overline{\text{TCLR}}$ Low to MATCH Invalid	t_{RSML}	—	10	ns
$\overline{\text{TCLR}}$ High to MATCH Valid	t_{RSMV}	—	100	ns
$\overline{\text{TCLR}}$ Low to TAG High–Z	t_{RSQZ}	—	10	ns
$\overline{\text{TCLR}}$ High to TAG Active	t_{RSQX}	—	100	ns
STANDBY Setup to $\overline{\text{TCLR}}$ Low	t_{PDSR}	30	—	ns
$\overline{\text{TCLR}}$ High to TWE Low	t_{RHWX}	80	—	ns



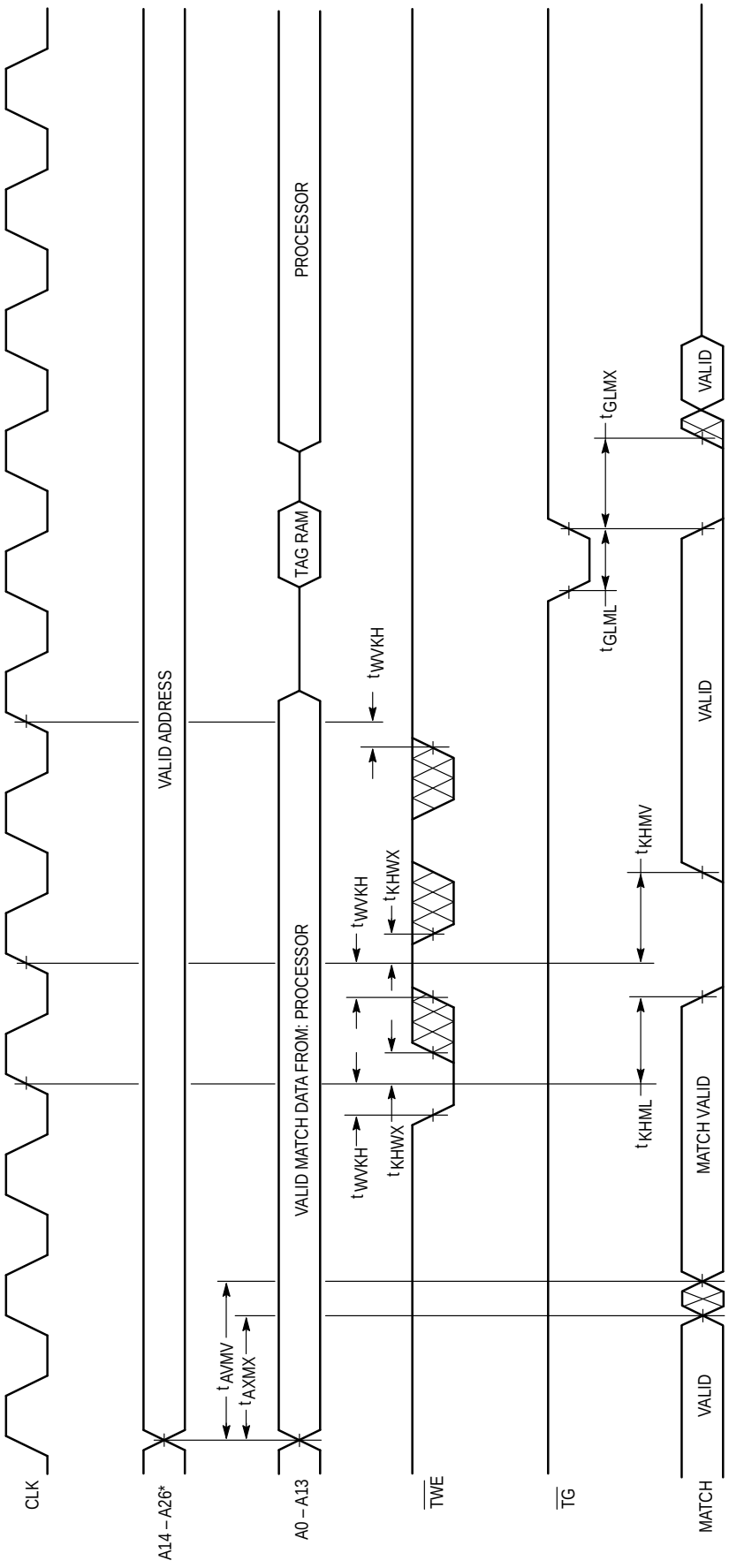
(a) **(b)**

Figure 1. Test Loads

TIMING LIMITS

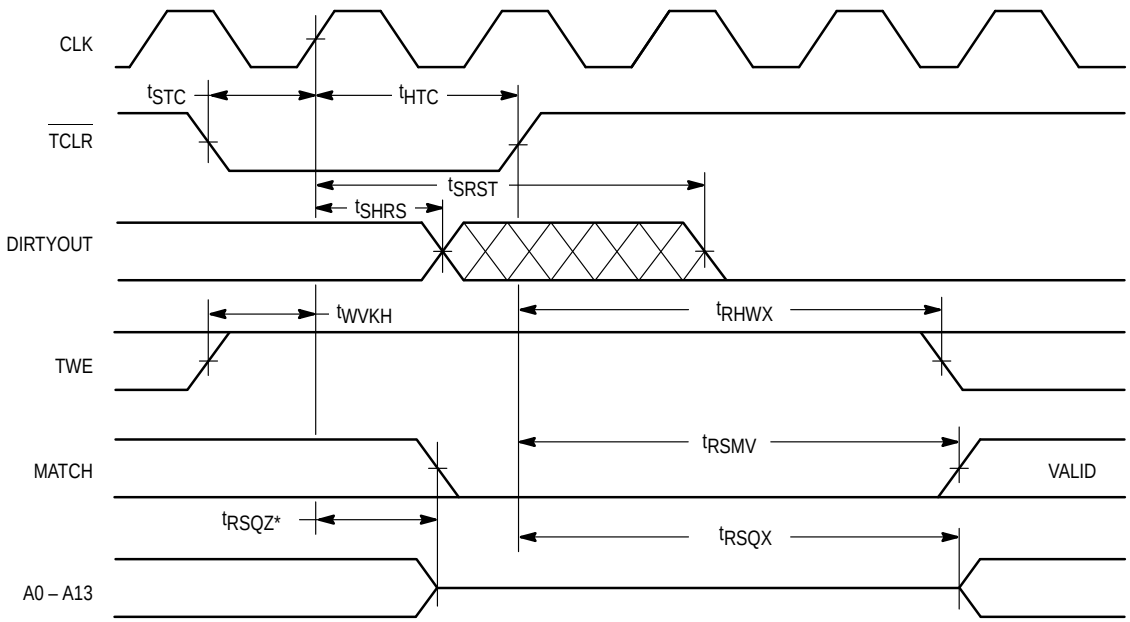
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

TAG RAM MATCH CYCLE



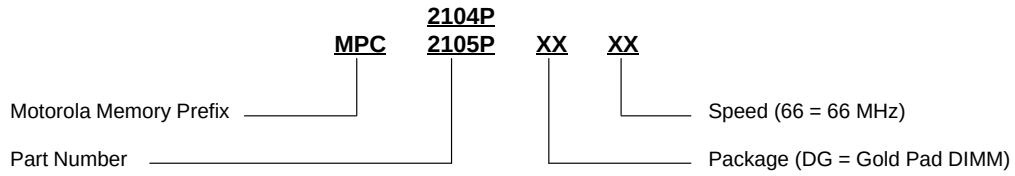
*Cache addresses used are: A14 – A26 for MPC2104P.

TAG RAM $\overline{\text{TCLR}}$ FUNCTION



* Transition is measured plus or minus 200 mV from steady state.

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MPC2104PDG66 MPC2104P = 256KB, synchronous pipelined
MPC2105PDG66 MPC2105P = 512KB, synchronous pipelined

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