

Low Voltage 1:12 Clock Distribution Chip

The MPC948 is a 1:12 low voltage clock distribution chip. The device features the capability to select either a differential LVPECL or a LVTTTL compatible input. The 12 outputs are LVCMOS or LVTTTL compatible and feature the drive strength to drive 50Ω series terminated transmission lines. With output-to-output skews of 350ps, the MPC948 is ideal as a clock distribution chip for the most demanding of synchronous systems. For a similar product targeted at a lower price/performance point, please consult the MPC947 data sheet.

- Clock Distribution for PowerPC™ 620 L2 Cache
- LVPECL or LVCMOS/LVTTTL Clock Input
- 350ps Maximum Output-to-Output Skew
- Drives Up to 24 Independent Clock Lines
- Maximum Output Frequency of 150MHz
- Synchronous Output Enable
- Tristatable Outputs
- 32-Lead TQFP Packaging
- 3.3V V_{CC} Supply Voltage

With an output impedance of approximately 7Ω, in both the HIGH and LOW logic states, the output buffers of the MPC948 are ideal for driving series terminated transmission lines. More specifically, each of the 12 MPC948 outputs can drive two series terminated 50Ω transmission lines. With this capability, the MPC948 has an effective fanout of 1:24 in applications where each line drives a single load. With this level of fanout, the MPC948 provides enough copies of low skew clocks for high performance synchronous systems, including use as a clock distribution chip for the L2 cache of a PowerPC 620 based system.

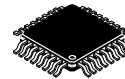
The differential LVPECL inputs of the MPC948 allow the device to interface directly with a LVPECL fanout buffer like the MC100LVE111 to build very wide clock fanout trees or to couple to a high frequency clock source. The LVCMOS/LVTTTL input provides a more standard interface for applications requiring only a single clock distribution chip at relatively low frequencies. In addition, the two clock sources can be used to provide for a test clock interface as well as the primary system clock. A logic HIGH on the TTL_CLK_Sel pin will select the TTL level clock input.

All of the control inputs are LVCMOS/LVTTTL compatible. The MPC948 provides a synchronous output enable control to allow for starting and stopping of the output clocks. A logic high on the Sync_OE pin will enable all of the outputs. Because this control is synchronized to the input clock, potential output glitching or runt pulse generation is eliminated. In addition, for board level test, the outputs can be tristated via the tristate control pin. A logic LOW applied to the Tristate input will force all of the outputs into high impedance. Note that all of the MPC948 inputs have internal pullup resistors.

The MPC948 is fully 3.3V compatible. The 32-lead TQFP package was chosen to optimize performance, board space and cost of the device. The 32-lead TQFP has a 7x7mm body size with a conservative 0.8mm pin spacing.

MPC948

**LOW VOLTAGE
1:12 CLOCK
DISTRIBUTION CHIP**



FA SUFFIX
32-LEAD TQFP PACKAGE
CASE 873A-02

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MPC948

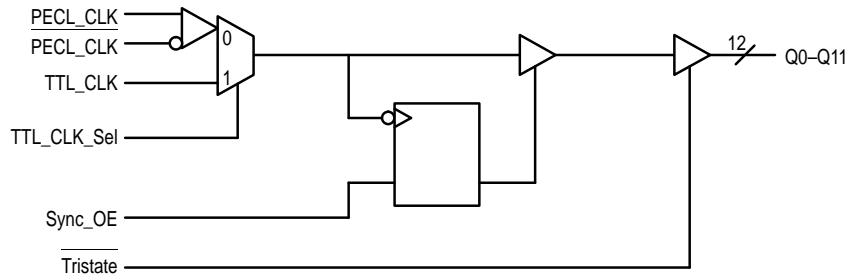
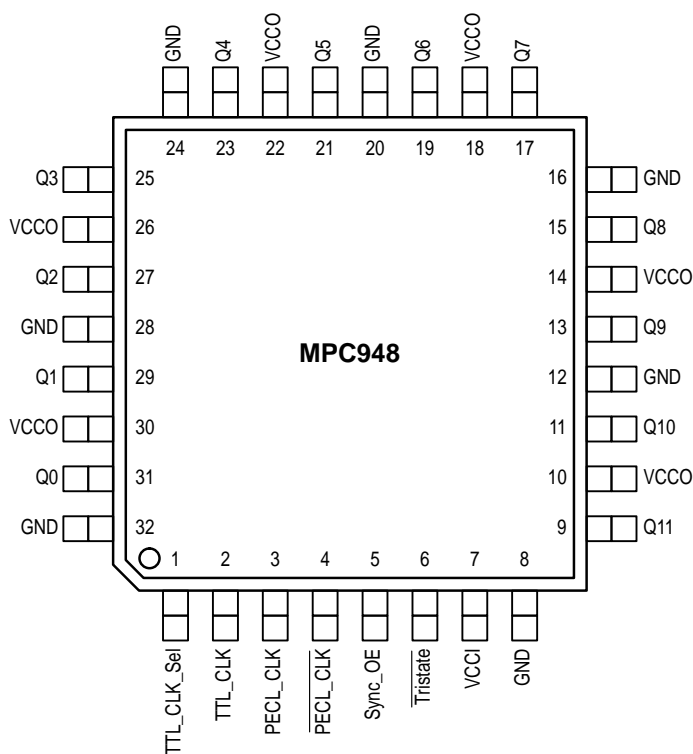


Figure 1. Logic Diagram



FUNCTION TABLES

TTL_CLK_Sel	Input
0	PECL_CLK
1	TTL_CLK
Sync_OE	Outputs
0	Disabled
1	Enabled
Tristate	Outputs
0	Tristate
1	Enabled

Figure 2. 32-Lead Pinout (Top View)

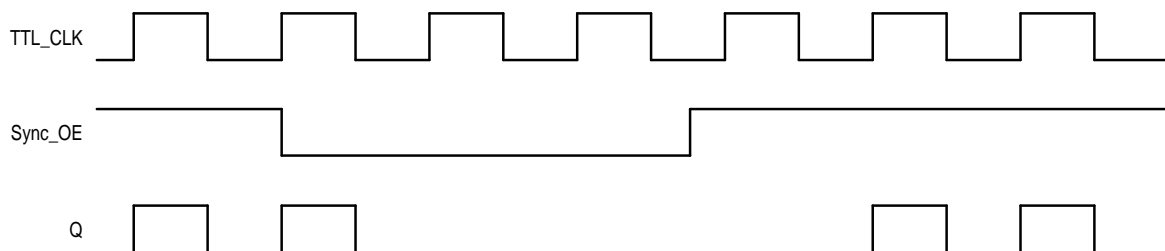


Figure 3. Sync_OE Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply Voltage	-0.3	4.6	V
V _I	Input Voltage	-0.3	V _{DD} + 0.3	V
I _{IN}	Input Current		±20	mA
T _{Stor}	Storage Temperature Range	-40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±0.3V)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V _{IH}	Input HIGH Voltage PECL_CLK Other	2.135 2.0		2.42 3.60	V	Single Ended Spec
V _{IL}	Input LOW Voltage PECL_CLK Other	1.49		1.825 0.8	V	Single Ended Spec
V _{PP}	Peak-to-Peak Input Voltage PECL_CLK	300		1000	mV	
V _{CMR}	Common Mode Range PECL_CLK	V _{CC} - 2.0		V _{CC} - 0.6	V	Note NO TAG
V _{OH}	Output HIGH Voltage	2.5			V	I _{OH} = -20mA (Note NO TAG)
V _{OL}	Output LOW Voltage			0.4	V	I _{OL} = 20mA (Note NO TAG)
I _{IN}	Input Current			±100	μA	Note NO TAG
C _{IN}	Input Capacitance			4	pF	
C _{pd}	Power Dissipation Capacitance		25		pF	Per Output
I _{CC}	Maximum Quiescent Supply Current		22	30	mA	

- V_{CMR} is the difference from the most positive side of the differential input signal. Normal operation is obtained when the "HIGH" input is within the V_{CMR} range and the input swing lies within the V_{PP} specification.
- The MPC948 outputs can drive series or parallel terminated 50Ω (or 50Ω to V_{CC}/2) transmission lines on the incident edge (see Applications Info section).
- Inputs have pull-up resistors which affect input current, PECL_CLK has a pull-down resistor.

AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±0.3V)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
F _{max}	Maximum Input Frequency	150			MHz	Note NO TAG
t _{pd}	Propagation Delay PECL_CLK to Q TTL_CLK to Q	4.0 4.4		8.0 8.9	ns	Note NO TAG
t _{sk(o)}	Output-to-Output Skew			350	ps	Note NO TAG
t _{sk(pr)}	Part-to-Part Skew PECL_CLK to Q TTL_CLK to Q			1.5 2.0	ns	Notes NO TAG, NO TAG
t _{pwo}	Output Pulse Width	t _{CYCLE} /2- 800		t _{CYCLE} /2+ 800	ps	Notes NO TAG, NO TAG Measured at V _{CC} /2
t _s	Setup Time Sync_OE to PECL_CLK Sync_OE to TTL_CLK	1.0 0.0			ns	Notes NO TAG, NO TAG
t _h	Hold Time PECL_CLK to Sync_OE TTL_CLK to Sync_OE	0.0 1.0			ns	Notes NO TAG, NO TAG
t _{PZL} , t _{PZH}	Output Enable Time	3		11	ns	
t _{PLZ} , t _{PHZ}	Output Disable Time	3		11	ns	
t _r , t _f	Output Rise/Fall Time	0.20		1.0	ns	0.8V to 2.0V

- Driving 50Ω transmission lines
- Part-to-part skew at a given temperature and voltage
- Assumes 50% input duty cycle.
- Setup and Hold times are relative to the falling edge of the input clock

APPLICATIONS INFORMATION

Driving Transmission Lines

The MPC948 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions brochure (BR1333/D).

In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to VCC/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC948 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. NO TAG illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC948 clock driver is effectively doubled due to its capability to drive multiple lines.

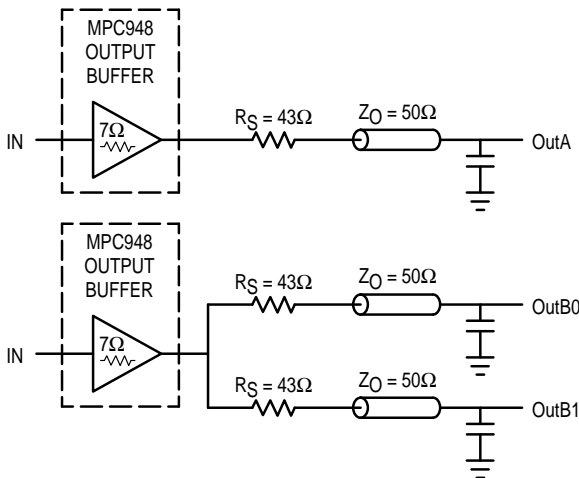


Figure 4. Single versus Dual Transmission Lines

The waveform plots of NO TAG show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC948 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC948. The output waveform in NO TAG shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the

line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_0 / R_s + R_o + Z_0) = 3.0 (25 / 53.5) = 1.40V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

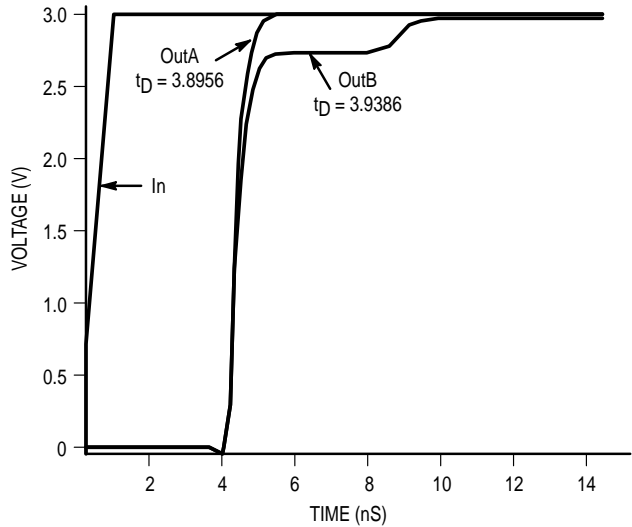


Figure 5. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in NO TAG should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

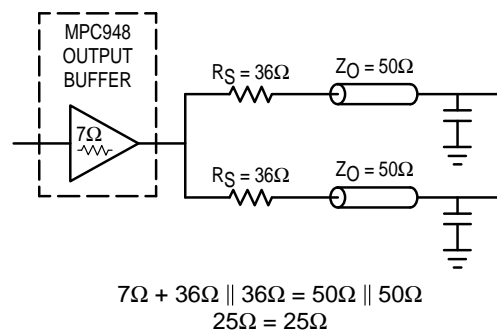
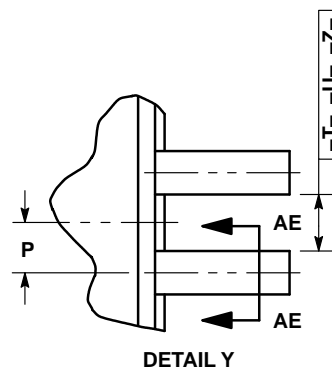
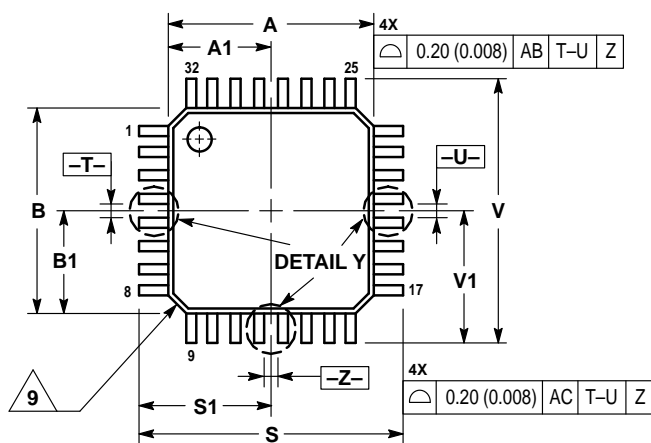


Figure 6. Optimized Dual Line Termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

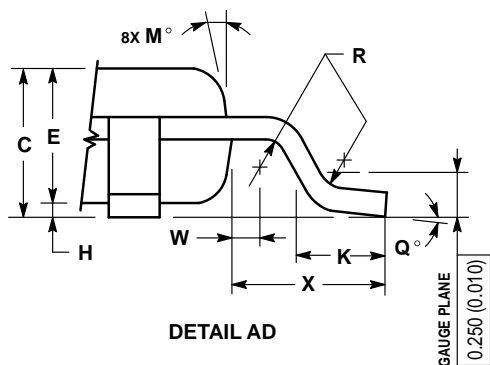
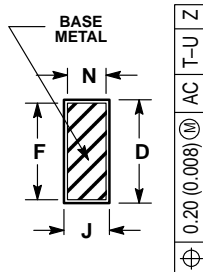
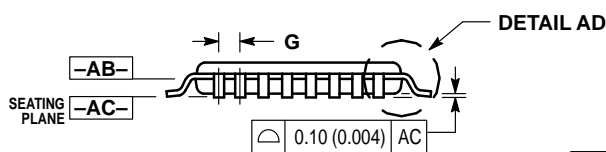
OUTLINE DIMENSIONS

FA SUFFIX
TQFP PACKAGE
CASE 873A-02
ISSUE A




NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -AB- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -T-, -U-, AND -Z- TO BE DETERMINED AT DATUM PLANE -AB-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -AC-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -AB-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.



SECTION AE-AE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

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