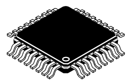
Advance Information

Low Voltage 1:12 Clock Distribution Chip

MPC948L

**LOW VOLTAGE
1:12 CLOCK
DISTRIBUTION CHIP**



FA SUFFIX
32–LEAD TQFP PACKAGE
CASE 873A–02

The MPC948L is a 1:12 low voltage clock distribution chip. The device is pin and function compatible with the MPC948 with the added feature of 2.5V output capabilities. The device features the capability to select either a differential LVPECL or a LVTTL compatible input. The 12 outputs are 2.5V LVCMOS or LVTTL compatible and feature the drive strength to drive 50Ω series terminated transmission lines. With output–to–output skews of 350ps, the MPC948L is ideal as a clock distribution chip for the most demanding of synchronous systems.

- Clock Distribution for Intel Microprocessors
- LVPECL or LVCMOS/LVTTL Clock Input
- 350ps Maximum Output–to–Output Skew
- Drives Up to 24 Independent Clock Lines
- Maximum Output Frequency of 150MHz
- Synchronous Output Enable
- Tristatable Outputs
- 32–Lead TQFP Packaging
- 2.5V Output Capability

With an output impedance of approximately 7Ω, in both the HIGH and LOW logic states, the output buffers of the MPC948L are ideal for driving series terminated transmission lines. More specifically, each of the 12 MPC948L outputs can drive two series terminated 50Ω transmission lines. With this capability, the MPC948L has an effective fanout of 1:24 in applications where each line drives a single load.

The differential LVPECL inputs of the MPC948L allow the device to interface directly with a LVPECL fanout buffer like the MC100LVE111 to build very wide clock fanout trees or to couple to a high frequency clock source. The LVCMOS/LVTTL input provides a more standard interface for applications requiring only a single clock distribution chip at relatively low frequencies. In addition, the two clock sources can be used to provide for a test clock interface as well as the primary system clock. A logic HIGH on the TTL_CLK_Sel pin will select the TTL level clock input.

All of the control inputs are LVCMOS/LVTTL compatible. The MPC948L provides a synchronous output enable control to allow for starting and stopping of the output clocks. A logic high on the Sync_OE pin will enable all of the outputs. Because this control is synchronized to the input clock, potential output glitching or runt pulse generation is eliminated. In addition, for board level test, the outputs can be tristated via the tristate control pin. A logic LOW applied to the Tristate input will force all of the outputs into high impedance. Note that all of the MPC948L inputs have internal pullup resistors.

The 32–lead TQFP package was chosen to optimize performance, board space and cost of the device. The 32–lead TQFP has a 7x7mm body size with a conservative 0.8mm pin spacing.

The MPC948L features two independent power supplies; VCCI and VCCO. The VCCI pin powers the internal core logic and must be tied to 3.3V. The VCCO pin powers the output buffer and can be tied to either 2.5V or 3.3V.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

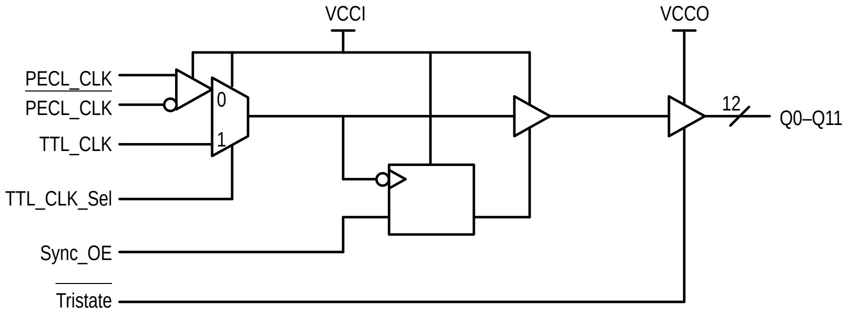


Figure 1. Logic Diagram

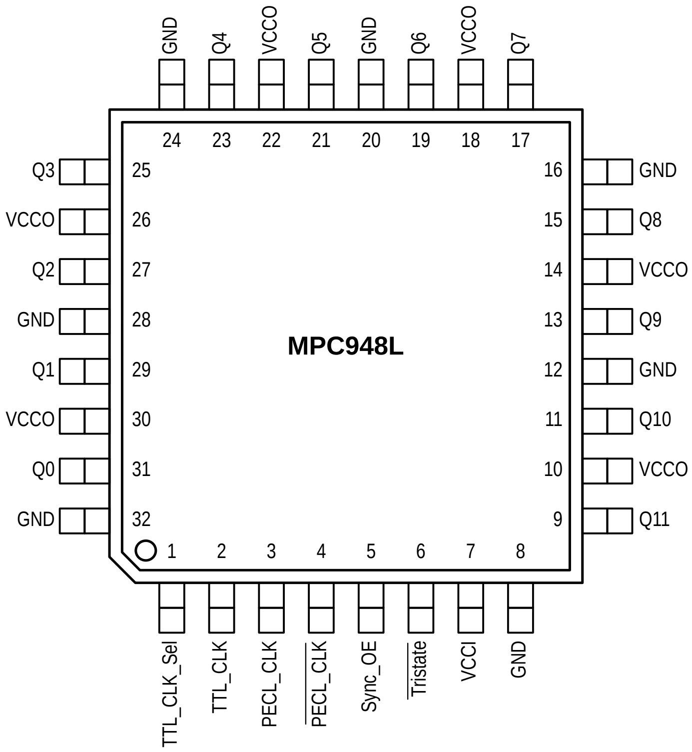


Figure 2. 32–Lead Pinout (Top View)

FUNCTION TABLES

TTL_CLK_Sel	Input
0 1	PECL_CLK TTL_CLK

Sync_OE	Outputs
0 1	Disabled Enabled

Tristate	Outputs
0 1	Tristate Enabled

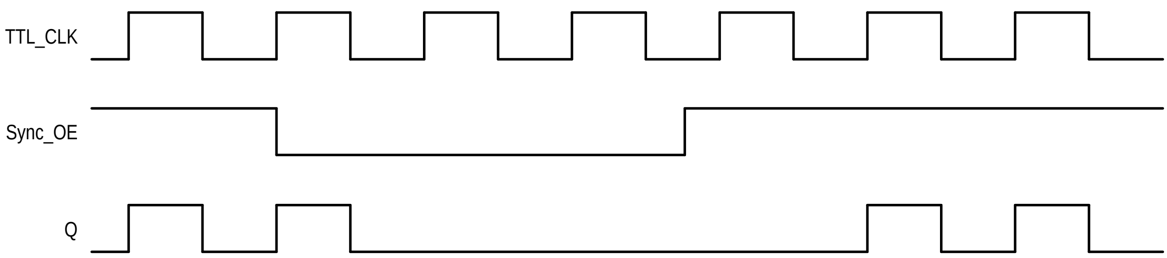


Figure 3. Sync_OE Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	4.6	V
V_I	Input Voltage	–0.3	V_{DD} + 0.3	V
I_{IN}	Input Current		±20	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CCI} = 3.3V ±5%; V_{CCO} = 2.5V ±5% or 3.3V ±5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	PECL_CLK Other	2.135 2.0		2.42 3.60	V	Single Ended Spec
V_{IL}	Input LOW Voltage	PECL_CLK Other	1.49		1.825 0.8	V	Single Ended Spec
V_{PP}	Peak–to–Peak Input Voltage	PECL_CLK	300		1000	mV	
V_{CMR}	Common Mode Range	PECL_CLK	V_{CC} – 2.0		V_{CC} – 0.6	V	Note 1.
V_{OH}	Output HIGH Voltage	VCCO = 3.3V VCCO = 2.5V	2.5 2.0			V	I_{OH} = –20mA (Note 2.)
V_{OL}	Output LOW Voltage				0.4	V	I_{OL} = 20mA (Note 2.)
I_{IN}	Input Current				±100	μA	Note 3.
C_{IN}	Input Capacitance				4	pF	
C_{pd}	Power Dissipation Capacitance			25		pF	Per Output
I_{CC}	Maximum Quiescent Supply Current			22	30	mA	

1. V_{CMR} is the difference from the most positive side of the differential input signal. Normal operation is obtained when the "HIGH" input is within the V_{CMR} range and the input swing lies within the V_{PP} specification.
2. The MPC948L outputs can drive series or parallel terminated 50Ω (or 50Ω to V_{CC}/2) transmission lines on the incident edge (see Applications Info section).
3. Inputs have pull–up resistors which affect input current, $\overline{\text{PECL\_CLK}}$ has a pull–down resistor.

AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CCI} = 3.3V ±5%; V_{CCO} = 2.5V ±5% or 3.3V ±5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
F_{max}	Maximum Input Frequency		150			MHz	Note 4.
t_{pd}	Propagation Delay	PECL_CLK to Q TTL_CLK to Q		7.0 7.9		ns	Note 4.
$t_{sk(o)}$	Output–to–Output Skew				350	ps	Note 4.
$t_{sk(pr)}$	Part–to–Part Skew	PECL_CLK to Q TTL_CLK to Q		1.5 2.0		ns	Notes 4., 5.
t_{pwo}	Output Pulse Width		t_{CYCLE}/2– 800		t_{CYCLE}/2+ 800	ps	Notes 4., 6. Measured at V_{CC}/2
t_s	Setup Time	Sync_OE to PECL_CLK Sync_OE to TTL_CLK	1.0 0.0			ns	Notes 4., 7.
t_h	Hold Time	PECL_CLK to Sync_OE TTL_CLK to Sync_OE	0.0 1.0			ns	Notes 4., 7.
t_{PZL},t_{PZH}	Output Enable Time		3		11	ns	
t_{PLZ},t_{PHZ}	Output Disable Time		3		11	ns	
t_r, t_f	Output Rise/Fall Time		0.20		1.0	ns	0.8V to 2.0V

4. Driving 50Ω transmission lines
5. Part–to–part skew at a given temperature and voltage
6. Assumes 50% input duty cycle.
7. Setup and Hold times are relative to the falling edge of the input clock

APPLICATIONS INFORMATION

Driving Transmission Lines

The MPC948L clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions brochure (BR1333/D).

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to VCC/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC948L clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC948L clock driver is effectively doubled due to its capability to drive multiple lines.

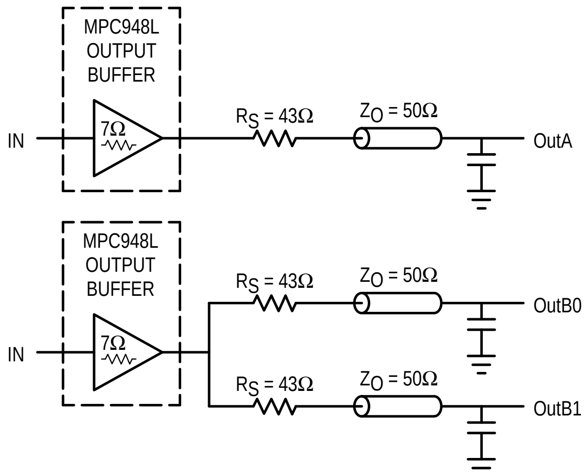


Figure 4. Single versus Dual Transmission Lines

The waveform plots of Figure 5 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC948L output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC948L. The output waveform in Figure 5 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$VL = VS (Zo / Rs + Ro +Zo) = 3.0 (25/53.5) = 1.40V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

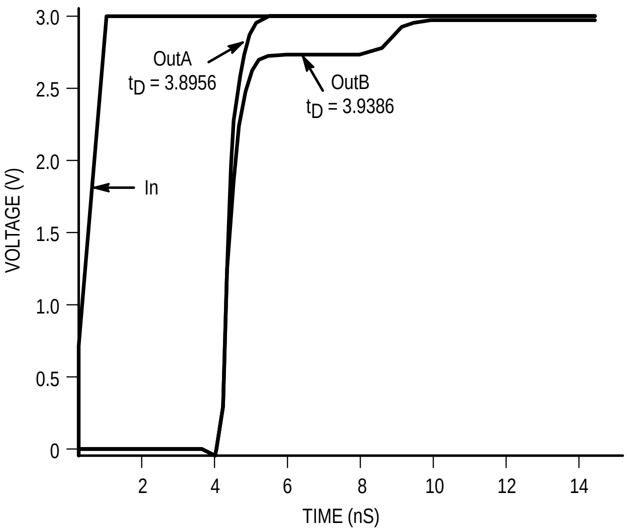
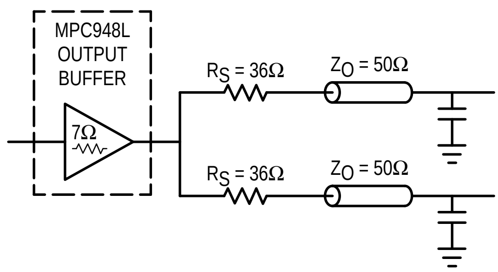


Figure 5. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 6 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



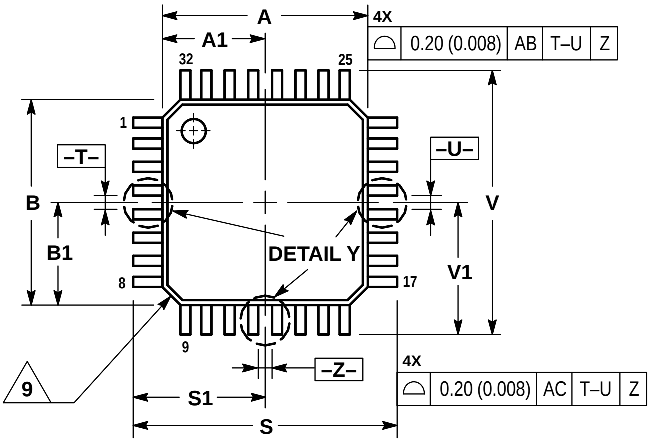
$$7\Omega + 36\Omega \parallel 36\Omega = 50\Omega \parallel 50\Omega$$
$$25\Omega = 25\Omega$$

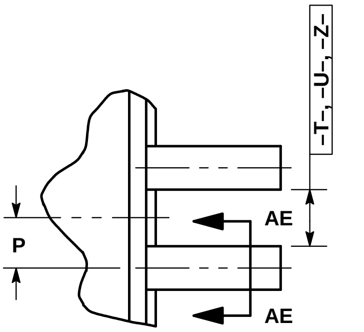
Figure 6. Optimized Dual Line Termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

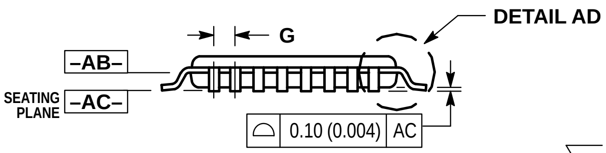
OUTLINE DIMENSIONS

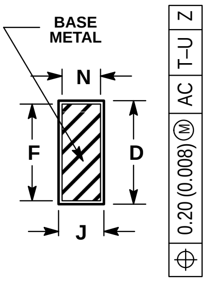
FA SUFFIX
TQFP PACKAGE
CASE 873A–02
ISSUE A



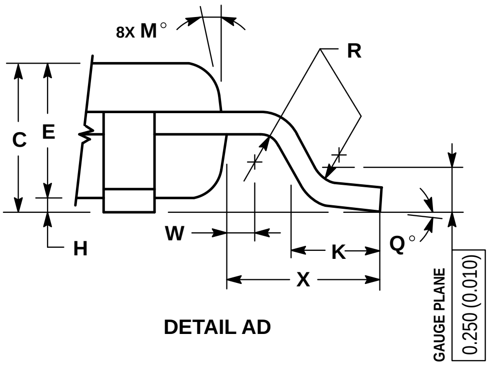


DETAIL Y





SECTION AE–AE



DETAIL AD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

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ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298