Product Preview

Low Voltage PLL Clock Driver

MPC953

LOW VOLTAGE PLL CLOCK DRIVER

FA SUFFIX
32–LEAD TQFP PACKAGE
CASE 873A–02

The MPC953 is a 3.3V compatible, PLL based clock driver device targeted for high performance clock tree designs. With output frequencies of up to 87.5MHz and output skews of 150ps the MPC953 is ideal for the most demanding clock tree designs. The devices employ a fully differential PLL design to minimize cycle–to–cycle and phase jitter.

- Fully Integrated PLL
- Output Frequency up to 87.5MHz
- Outputs Disable in High Impedance
- TQFP Packaging
- 100ps Cycle–to–Cycle Jitter

The MPC953 has a differential LVPECL reference input along with an external feedback input. These features make the MPC953 ideal for use as a zero delay, low skew fanout buffer. The device performance has been tuned and optimized for zero delay performance. The MR/OE input pin will reset the internal counters and tristate the output buffers when driven “high”.

If the reference clock (PECL_CLK) is lost or shut down when the MPC953 is in phase–lock, the output frquency will slew slowly downward. The final VCO frequency will be around TBDMHz.

The MPC953 is fully 3.3V compatible and requires no external loop filter components. All control inputs accept LVCMOS or LVTTL compatible levels while the outputs provide LVCMOS levels with the ability to drive terminated 50Ω transmission lines. For series terminated 50Ω lines, each of the MPC953 outputs can drive two traces giving the device an effective fanout of 1:18. The device is packaged in a 7x7mm 32–lead TQFP package to provide the optimum combination of board density and performance.

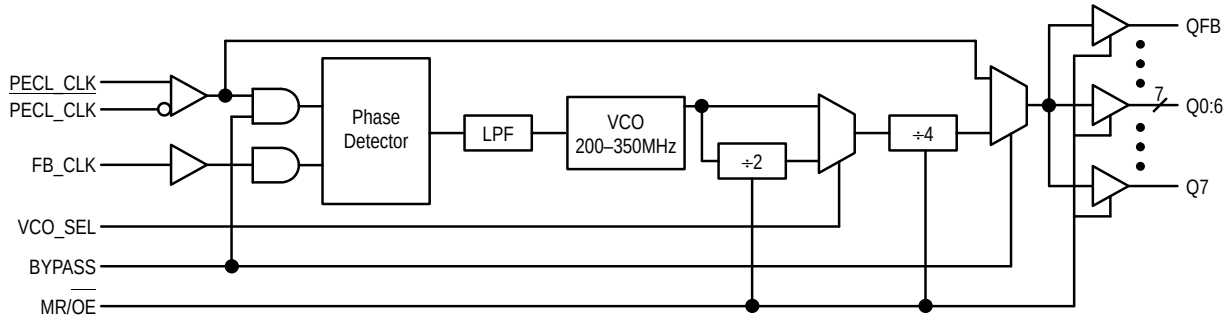

Figure 1. Logic Diagram

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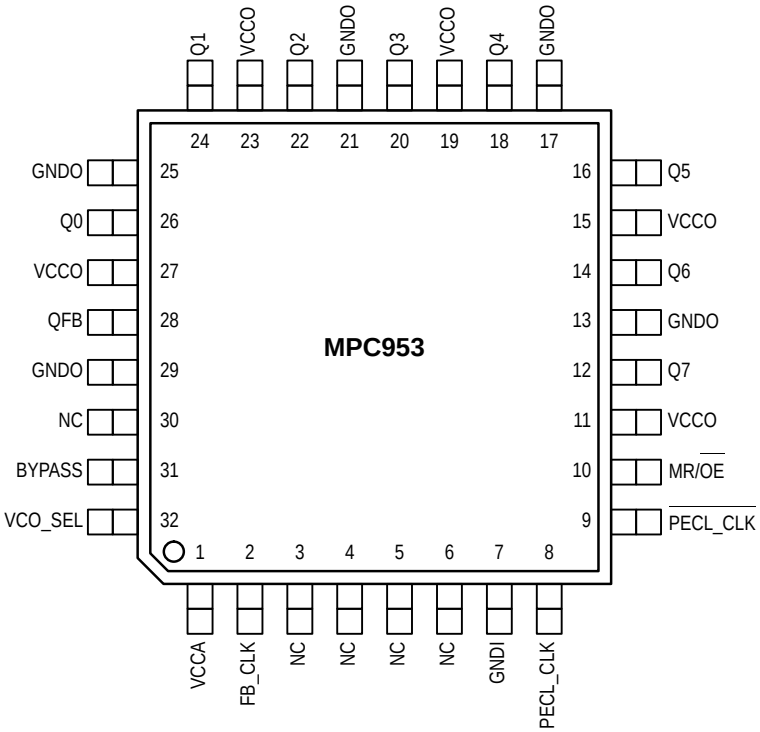


Figure 2. 32–Lead Pinout (Top View)

FUNCTION TABLES

BYPASS	**Function**
1	PLL Enabled
0	PLL Bypass
MR/$\overline{OE}$	**Function**
1	Outputs Disabled
0	Outputs Enabled
VCO_SEL	**Function**
1	÷2
0	÷1

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	4.6	V
V_I	Input Voltage	–0.3	V_{DD} + 0.3	V
I_{IN}	Input Current		±20	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage LVCMOS Inputs	2.0		3.6	V	
V_{IL}	Input LOW Voltage LVCMOS Inputs			0.8	V	
V_{PP}	Peak–to–Peak Input Voltage PECL_CLK	300		1000	mV	
V_{CMR}	Common Mode Range PECL_CLK	V_{CC}–1.5		V_{CC}–0.6	mV	Note 1.
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = –40mA, Note 2.
V_{OL}	Output LOW Voltage			0.5	V	I_{OL} = 40mA, Note 2.
I_{IN}	Input Current			±120	µA	
C_{IN}	Input Capacitance			4	pF	
C_{pd}	Power Dissipation Capacitance		25		pF	Per Output
I_{CC}	Maximum Quiescent Supply Current			75	mA	All VCC Pins
I_{CCPLL}	Maximum PLL Supply Current		15	20	mA	VCCA Pin Only

1. V_{CMR} is the difference from the most positive side of the differential input signal. Normal operation is obtained when the “HIGH” input is within the V_{CMR} range and the input swing lies within the V_{PP} specification.
2. The MPC953 outputs can drive series or parallel terminated 50Ω (or 50Ω to V_{CC}/2) transmission lines on the incident edge (see Applications Info section).

PLL INPUT REFERENCE CHARACTERISTICS (T_A = 0 to 70°C)

Symbol	Characteristic	Min	Max	Unit	Condition
f_{ref}	Reference Input Frequency	Note 3.	Note 3.	MHz	
f_{refDC}	Reference Input Duty Cycle	25	75	%	

3. Maximum and minimum input reference is limited by the VCO lock range and the feedback divider.

AC CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 3.3V ±5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
t_r, t_f	Output Rise/Fall Time	0.10		1.0	ns	0.8 to 2.0V
t_{pw}	Output Duty Cycle	45	50	55	%	
$t_{sk(O)}$	Output–to–Output Skews (Relative to QFB)			±75	ps	
f_{VCO}	PLL VCO Lock Range	200		350	MHz	
f_{max}	Maximum Output Frequency	50		87.5	MHz	VCO_SEL = ‘0’
t_{pd}(lock)	Input to Ext_FB Delay (with PLL Locked)	X–100	X (Note 4.)	X+100	ps	f_{ref} = 75MHz
t_{pd}(bypass)	Input to Q Delay (with PLL Bypassed)	5		10	ns	
$t_{PLZ,HZ}$	Output Disable Time			7	ns	
t_{PZL}	Output Enable Time			6	ns	
t_{jitter}	Cycle–to–Cycle Jitter (Peak–to–Peak)			100	ps	
t_{lock}	Maximum PLL Lock Time			10	ms	

4. X will be targeted for 0ns, but may vary from target by ±150ps based on characterization of silicon.

Power Supply Filtering

The MPC953 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC953 provides separate power supplies for the output buffers (VCCO) and the phase–locked loop (VCCA) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the VCCA pin for the MPC953.

Figure 3 illustrates a typical power supply filter scheme. The MPC953 is most susceptible to noise with spectral content in the 1KHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the VCCA pin of the MPC953. From the data sheet the I_{VCCA} current (the current sourced through the VCCA pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the VCCA pin very little DC voltage drop can be tolerated when a 3.3V V_{CC} supply is used. The resistor shown in Figure 3 must have a resistance of 10–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. It is recommended that the user start with an 8–10Ω resistor to avoid potential V_{CC} drop problems and only move to the higher value resistors when a higher level of attenuation is shown to be needed.

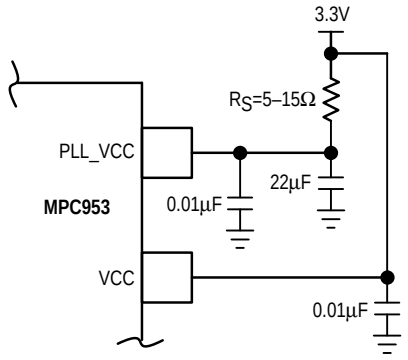


Figure 3. Power Supply Filter

Although the MPC953 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The MPC953 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions brochure (BR1333/D).

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to VCC/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC953 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC953 clock driver is effectively doubled due to its capability to drive multiple lines.

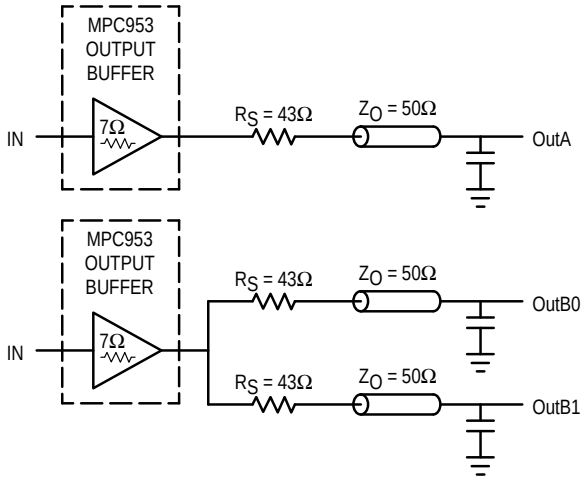


Figure 4. Single versus Dual Transmission Lines

The waveform plots of Figure 5 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC953 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC953. The output waveform in Figure 5 shows a step in the waveform, this step is caused

by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

VL = VS (Zo / (Rs + Ro +Zo))

Zo = 50Ω || 50Ω
Rs = 43Ω || 43Ω
Ro = 7Ω

VL = 3.0 (25 / (21.5 + 7 + 25) = 3.0 (25 / 53.5)
= 1.40V

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

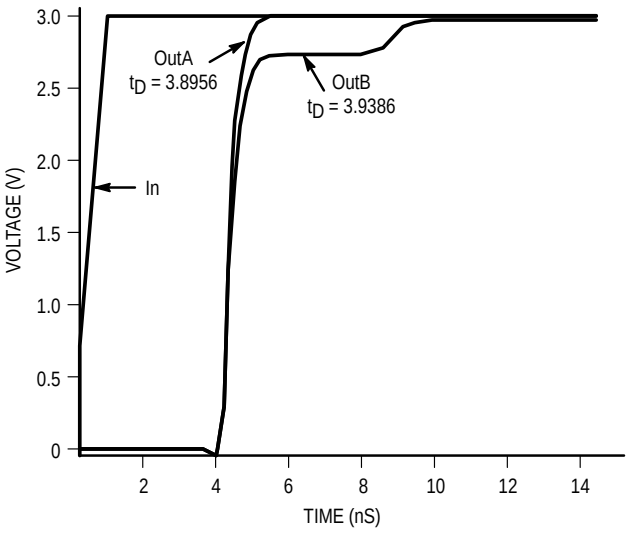
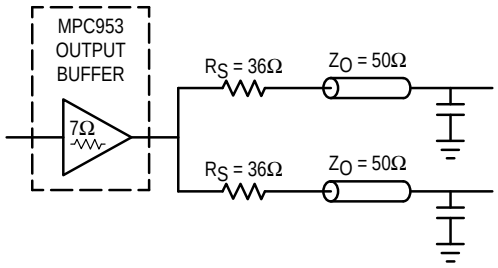


Figure 5. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 6 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



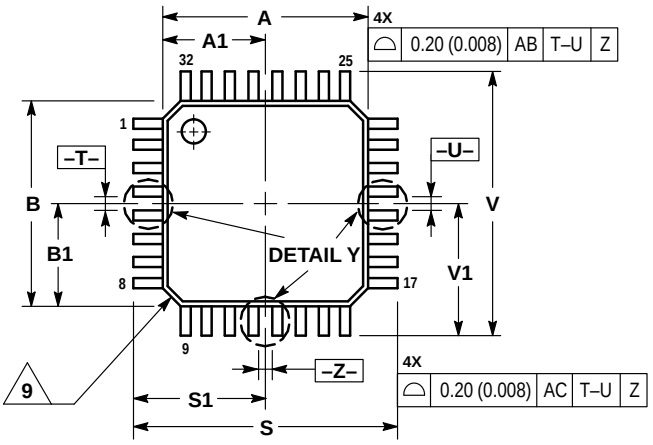
7Ω + 36Ω || 36Ω = 50Ω || 50Ω
25Ω = 25Ω

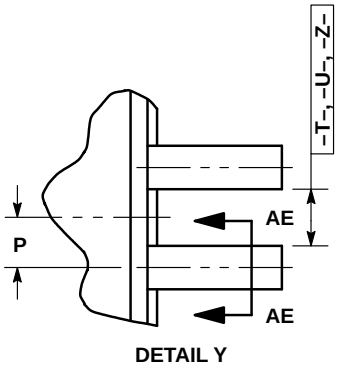
Figure 6. Optimized Dual Line Termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

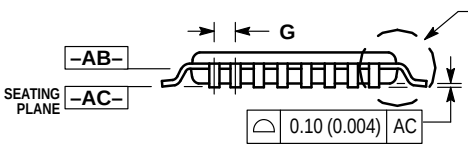
OUTLINE DIMENSIONS

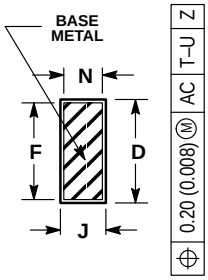
FA SUFFIX
TQFP PACKAGE
CASE 873A–02
ISSUE A



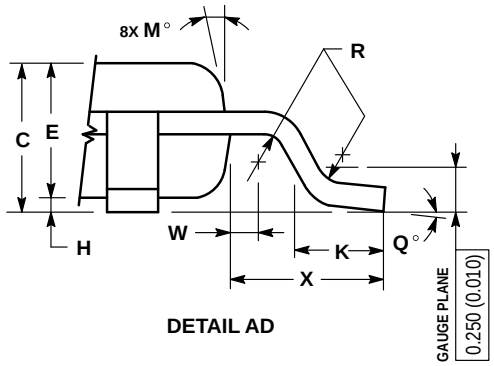


DETAIL Y





SECTION AE–AE



DETAIL AD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

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